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IDENTIFICATION

PRODUCT CODE:	MAINDEC-Ø8-DITCA-A-D REPLACES MAINDEC-Ø8-D3BD
PRODUCT NAME:	TC08* BASIC EXERCISER TC08 BE
DATE:	MAY 31, 1972
MAINTAINER:	DIAGNOSTIC GROUP
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1. ABSTRACT

The TC01 Basic Exerciser is a series of test programs that may be used to gain a high degree of confidence in the data handling ability of a TC01 DECtape Control and one to eight TU55 DECtape Transports. The Basic Exerciser consists of several basic routines that may be individually selected; each routine will operate on any configuration of one to eight drives. These routines include a Basic Motion Routine, Search Find All Blocks Test, Basic Search Routine, Start/Stop/Turnaround Test, Basic Write/Read Data Test with eight selectable patterns, and a Parity Generation and Checking Test. The operation of the Basic Motion Routine and the Baisc Search Routine are controlled by keyboard input. Also, a Write Data Scope Loop, Read Data Scope Loop, and a Search Scope Loop are provided to keep the tape moving from end zone to end zone.

2. REQUIREMENTS

2.1 Equipment

PDP-8 (standard)
TC01 *DECtape Control
One to eight TU55 DECtape Transports

2.2 Storage

The program occupies most of memory from address 0000 to 6377 and utilizes three buffer areas as follows:

Address	Function
6774-7174	Output buffer Program storage for Motion Test (0200) Block Number storage for Basic Search (0202)
7175-7375	INPUT buffer 1
7376-7576	INPUT buffer 2

2.3 Preliminary Programs (None)

3. LOADING PROCEDURE

3.1 Method

Use normal binary loading procedures from paper tape.

*This program can also be used on the TCØ8 DECtape control.
All tests are applicable, merely substitue "TCØ8" for "TCØ1 in text.

4. STARTING PROCEDURE

4.1 Control Switch Settings

Any configuration of one to eight drives may be selected in SWITCH REGISTER bits 0 to 7. Each bit is a master bit for selection of a drive. When the switch is a 1 the drive is selected; when a 0 the drive is not selected.

Switch	Drive
0	8
1	1
2	2
3	3
4	4
5	5
6	6
7	7

4.2 Starting Addresses of Routines

Address	Routine	Paragraph
0200	Basic Motion Routine	9.1
0201	Search Find All Blocks	9.2
0202	Basic Search Routine	9.3
0203	Start/Stop/Turnaround	9.4
0204	Write/Read Data Test	9.5
0205	Parity Generation Test	9.6
0206	Write Data Scope Loop	9.7
0207	Read Data Scope Loop	9.8
0210	Search Scope Loop	9.9

- CAUSE AC to COUNT FROM 0 to 2701 (BLOCKS) BACK AND FORTH.

4.3 Program and/or Operator Action

a. Place the select address for the routine desired in the SWITCH REGISTER and press LOAD ADDRESS.

b. Set SWITCH REGISTER bits 0 to 7 to select drives. (Any configuration except all 0s is valid.)

c. Press Start. The static register test will be run on status register A. and B. The processor should halt at address 0223 with bits 0 to 7 of the switch register displayed in the AC. For all error halts other than mentioned in 4.3 section D, consult the listing.

d. A halt at address 0311 indicates bits 0 to 7 were all 0s. Select drives and press CONTINUE to recover.

e. Set all SWITCH REGISTER bits to 0, or as desired according to paragraph 5.1, and press CONTINUE.

A detailed description of how the routines can be used to initially check out the control and drives can be found in paragraph 5.3.

5. OPERATING PROCEDURE

5.1 Operational Switch Settings

5.1.1 Routines with no Switch Settings - Four of the routines require different switch settings to control program flow. The routines that have no switch settings are:

0200	Basic Motion Routine
0202	Basic Search Routine
0205	Parity Generation
0207	Read Scope Loop
0210	Search Scope Loop

5.1.2 Search Find All Blocks - The Search Find All Blocks Routine (0201) has one switch setting. Setting SW11 to 1 deletes the halt at the end of test.

5.1.3 Write/Read Data Test - The Write/Read Data Test (0204) utilizes switches 3 to 11 to control pattern selection and program flow as follows:

Switch	Operation
3	Delete all error detection where the motion bit in status A remains 1 (parity, data compare errors, and WC (word count register) not equal to 0).
4	Run patterns sequentially; i.e., After making one complete pass the length of tape with pattern 5, the next pass is made with pattern 6.
5	Read data only (after the first write pass).
6	Write data only (SW5 overrides SW6).
7	Write and read sequence, one block at a time.
8	Write and read sequence, 32 blocks at a time. (SW7 overrides SW8, when both switches = 0, the write and read sequence occurs for the length of the tape).