CHAPTER 3
PRINCIPLES OF OPERATION

3.1 INTRODUCTION

This chapter presents three levels of PDP-8/E System operation. First, a simplified block diagram presenting the primary parts of the processor is discussed. Second, a flow chart relating the processor instructions to time states is presented and discussed with appropriate references to the corresponding third-level discussion. The third-level discussion presents the logic theory and is divided into functional groups of logic. A reference to the modules is provided so that continuity between the principles of operation and the engineering drawings exists throughout the discussion.

NOTE

The component designations are for reference only and do not necessarily correspond to those designations on engineering drawings.

Chapter 3 is divided into eight functional sections:

Section 1 – System Introduction

Section 2 – System Flow Diagrams

Section 3 – Timing Generator

Section 4 – Memory System

Section 5 – Central Processor

Section 6 – I/O Transfer Logic

Section 7 – Teletype Control

Section 8 – Power Supply

This format is provided to aid the user in understanding the principles of operation and to distinguish the individual parts of the basic PDP-8/E processor.

3.2 PDP-8/E BASIC SYSTEM

The PDP-8/E processor contains eight functional areas and can accommodate as many as 60 options. A simplified block diagram, Figure 3-1, relates the OMNIBUS to the major signals and the eight functional areas. Each of the functional areas is contained on a single quad-size module with the exception of the MM8-E (three modules are provided).

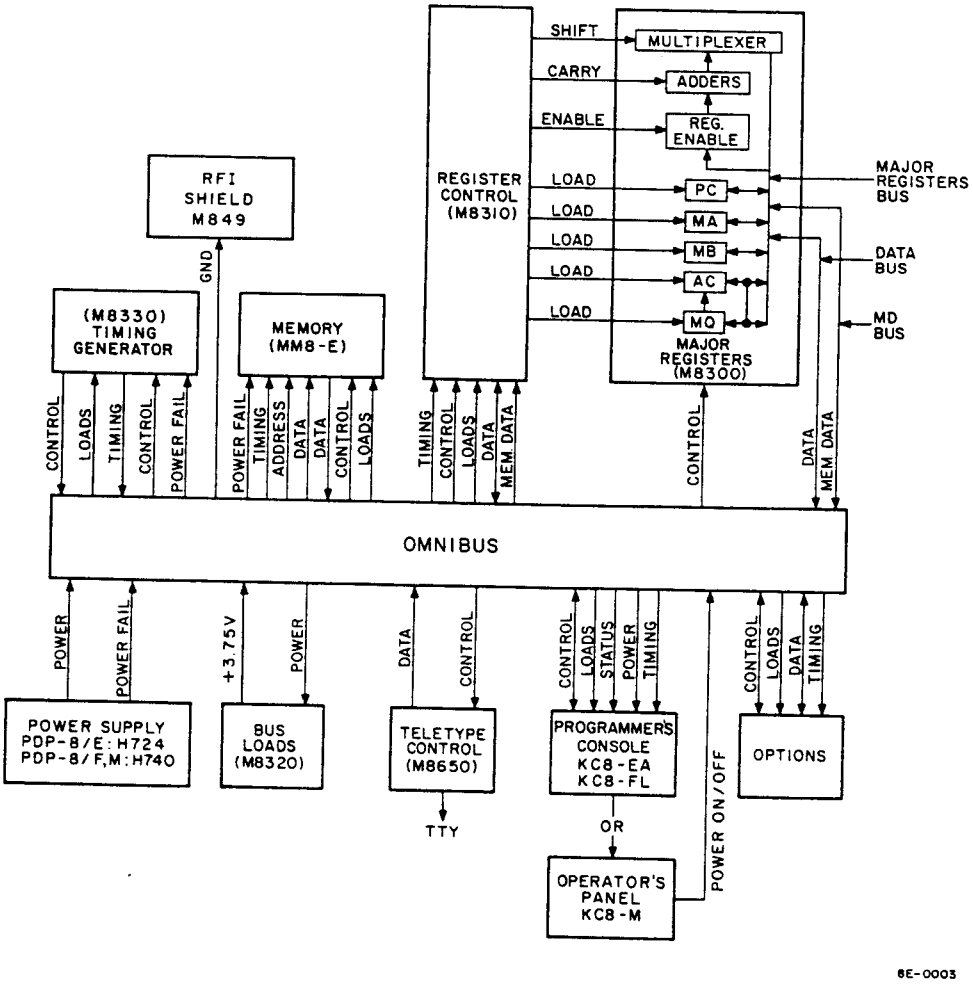

Figure 3-1 PDP-8/E Simplified Block Diagram

3.2.1 OMNIBUS

The OMNIBUS provides a two-way path between the corresponding connector pins of the modules that plug into it. To accommodate 96 signal lines plus ground and power at the module connectors, 144 pins are provided. In general, each signal line is kept at a +3.75 Vdc level and pulled to ground when the signal is asserted. However, exceptions occur, with respect to power levels and some timing and control signals. Bus loads provide this capability by applying +3.75 Vdc to the bus lines via load resistors. When a signal line is asserted, the output driver of that signal pulls the line to ground, the corresponding input circuits (on the same module or a different

module) are activated due to the low signal. This technique facilitates the interaction between modules and makes it possible to connect many modules to the same bus. Some signals do not use the OMNIBUS. The connection of the M8310 Register Control module and the M8300 Major Registers module is partially accomplished using an H851 Edge Connector for all of the control signals. Data is exchanged through the OMNIBUS.

3.2.2 Timing Generator (M8330)

The timing generator provides four time states (TS1 through TS4), four time pulses (TP1 through TP4) and memory timing signals. One memory cycle is accomplished between TS1 and TS4. A choice of two memory cycles is provided: a slow (1.4 μs) and a fast (1.2 μs) cycle. Control inputs are provided by the register control module and the power supply.

3.2.3 Memory (MM8-E)

Three memory modules are provided: the G619 Memory Stack, the G227 X/Y Driver and Current Source, and the G104 Sense/Inhibit.

The memory stack contains 12 core mats, each consisting of 4096 cores and selection diodes to provide a 12 bit-per-word, 4096 word storage capability.

The X/Y driver and current source module contains the selection switches, drivers, and current source required to fully select any one of the 4096 memory locations.

The sense/inhibit module is used to sense (read) any one of the 4096 memory locations and to write into any memory location.

3.2.4 Register Control (M8310)

The register control has many functional logic circuits that generate the major states of the processor, determine the instruction to be performed, and control the operation of the major registers (M8300). The register control receives a word from memory, decodes the word, and determines the operation to be performed. Functional logic is provided to gate bits into the major register adder circuit, shift right, or shift left. The M8310 develops register transfer signals and register load signals. The timing generator determines when these signals are generated.

3.2.5 Major Registers (M8300)

The major registers module provides the Program Counter (PC) Register, the Central Processor Memory Address (CPMA) Register, the Memory Buffer (MB) Register, the Accumulator (AC) Register, and the Multiply-Quotient (MQ) Register. Transfer of information in the AC to the MQ is accomplished directly through enabling logic. Transfer of all other registers is accomplished through the register enable logic, through the adders, and through the output multiplexers, where the information is placed onto the MAJOR REGISTERS BUS. Information can be brought into the MAJOR REGISTERS BUS from the DATA BUS and the MD BUS or transferred out to the same lines. Transfer of MB data to the MD lines is accomplished by MD DIR (H).

3.2.6 Power Supply (H724)

The power supply receives an input of 95 to 130 Vac, 47 to 63 Hz and provides 28 Vac, +8 Vdc, +5 Vdc, -15 Vdc, and +15 Vdc to the PDP-8/E System. The power system is interlocked with the front panel key switch. Power fail and overload detection are provided to ensure the protection of system components and system performance.

3.2.7 Bus Loads (M8320)

The bus loads receive +5 Vdc and +15 Vdc inputs from the power supply and provide a +3.75 Vdc output to the signal lines on the OMNIBUS.

3.2.8 Teletype Control (M8650)

The Teletype control module contains a receive register and transmit register, decoders, and interprets two flags. It performs the conversion of parallel computer words to serial Teletype words, assembles serial Teletype characters into data words for the computer and commands from the computer.

3.2.9 Programmer's Console (KC8-EA)

The programmer's console is a plug-in module, containing logic, lamps, and switches. The face panel, which contains openings for the switch levers and a silk-screened switch/indicator identification, is mounted in front of the programmer's console module. The panel OFF/POWER/PANEL LOCK switch is controlled by a key. The programmer's console enables the operator to deposit a 12-bit word into memory, read any memory location, observe the content of important registers, read the instruction currently being processed, and observe every primary activity the processor is currently performing.

3.2.10 RFI Shield (M849)

The RFI shield module ensures no interference of memory circuits with nonmemory options (those options not synchronized with memory).

3.2.11 Options

More than 60 options are available to the PDP-8/E user. The one option described in this volume is the Teletype control option. All other internal bus options are described in Volume 2. External bus options are described in Volume 3.

3.2.12 Signal Finder

The basic PDP-8/E signals and their descriptions are given in Table 3-1. If the reader desires to study the detailed logic as he is progressing through the flow diagrams, a corresponding paragraph reference to the detailed logic is provided. Refer to Appendix B for source-destination module designations.

Table 3-1
Signal Finder

Signal Name	Logic Reference	Signal Description
DATA T DATA F	3.35.3	Data Control GATE ENABLING signals – DATA BUS TO ADDERS: DATA T, DATA F COMPLEMENT OF DATA BUS TO ADDERS: DATA T, DATA F ZERO TO ADDERS: DATA T, DATA F*
AC → BUS L	3.35.2	Enables the Data Line MUX to allow the contents of the AC to be applied to the DATA BUS.
MQ → BUS L	3.35.2	Enables the Data Line MUX to allow the contents of the MQ to be applied to the DATA BUS.
SHL + LD ENA L AC → MQ ENA L	3.40	Enable signals applied to the MQ MUX to output either the MQ (one place to the left) or the contents of the AC. SHL + LD ENA L / AC → MQ ENA L / Output: L / L / MQ (left) L / H / MQ (left) H / L / AC H / H / 0
F SET L D SET L E SET L	3.34.1	Indicates the next major state. For example, F SET L means that the next major state is FETCH.
F L, D L, E L	3.34.1	Indicates the current major state.
DMA	3.8	Direct Memory Access State – asserted when MS, IR DISABLE is grounded.
INT IN PROG	3.42.1	Interrupt in Progress – this signal acknowledges an interrupt request and forces a JMS to the IR and EXECUTE to the Major State Register.
INT REQUEST L	3.42.1	Interrupt Request – when asserted (low) means that a device has set a flag and is requesting an Interrupt.
USER MODE	3.42.1	Used with the time-sharing option to prevent programmed halt, I/O PAUSE, OSR, or LAS.

*This condition cannot exist during OPERATE and TS3.