CHAPTER 4
MAINTENANCE

This chapter contains information pertinent to preventive maintenance, corrective maintenance, and troubleshooting techniques of the PDP-8/E.

SECTION 1 - PREPARATION FOR MAINTENANCE

4.1 EQUIPMENT

Table 4-1 lists the equipment and relevant specifications needed for maintenance of the basic PDP-8/E. Also included in the list is the equivalent equipment used by DEC Field Service personnel.

4.2 PROGRAMS

Table 2-4 in Chapter 2 lists the maintenance programs supplied by DEC for ascertaining proper PDP-8/E operation. To supplement these programs, there are eight short test routines detailed in the following paragraphs. These routines can be used, as needed, to perform the required maintenance.

NOTE
All diagnostics require a Programmer's Console, a working Teletype and at least 4K memory with the basic system.

4.2.1 TTY Receiver Test

Perform the following test to display a character (any character depressed on keyboard or read from paper tape) in the ac. Load address 0000 and deposit the following test routine in sequence:

Location	Contents
0000	6032
0001	6031
0002	5001
0003	6036
0004	5001

Load address 0000 and press CONT.

Table 4-1
Maintenance Equipment

Equipment	Specifications	Equivalent
Multimeter	10kΩ/V minimum	Triplett Model 310
Oscilloscope	dc to 50 Hz with calibrated deflection factors from 5 mV to 10V/div. Maximum horizontal sweep rate of 0.1 μs/div. Delaying sweep is desirable and dual trace is a necessity.	Tektronix Type 453
Probes	X10 with response characteristics matched to oscilloscope.	Tektronix Type P6010
Recessed Probe Tip (2)		Tektronix
Ground Leads (for each probe)		Tektronix
Integrated Circuit Pin Extender	AP Inc	DEC 29-10246
Double-Height Extender (2)		W984
Edge Connector Extender Cables (2)		BC08M-OM
Light Bulb Extractor		DEC 12-9151
Tool Kit		DEC Type 142
Black Spray Paint		DEC 120-68
White Spray Paint		DEC 120-94
Jumper Wire		30-Gauge with TERMI POINT Connections
Silicone Grease		Dow Corning Compound
1/16 in. Allen Wrench		Hunter 4Z 035
Single-Height Extender Module (1)		W980

4.2.2 TTY Transmitter Test

Perform the following test to print the character in the Switch Register (bits 04–11). Load address 0000 and deposit the following test routine in sequence:

Location	Contents
0000	7604
0001	6046
0002	6041
0003	5002
0004	5000

Load address 0000 and press CONT. To print a different character, change the contents of the Switch Register.

4.2.3 Echo Test

Perform the following test to type a character on the keyboard. Load address 0000 and deposit the following test routine in sequence:

Location	Contents
0000	6032
0001	6031
0002	5001
0003	6036
0004	6046
0005	6041
0006	5005
0007	5001

Load address 0000 and press CONT. Type any character on the keyboard and observe a corresponding echo return on the printer.

4.2.4 Print Test

Perform the following test to print all characters. Load address 0000 and deposit the following test routine in sequence:

Location	Contents	
0000	7001	/Increment ac
0001	6046	/Load buffer and print
0002	6041	/Skip if flag is set
0003	5002	/JMP .-1
0004	5000	/JMP 0

Load address 0000 and press CONT.

4.2.5 Deposit SR into Corresponding Address

Perform the following test to deposit the contents of the Switch Register into the corresponding address. Load address 0000 and deposit the following test routine in sequence:

Location	Contents
0000	7604
0001	3005
0002	1005
0003	3405
0004	5000

Load address 0000, change SR to any number equal to or greater than 5, and press CONT.

4.2.6 4K Core Transfer (8K or more systems only)

Perform the following test to test the relocation process. Load address 7600 and deposit the following routine in sequence:

Location	Contents	
7600	6201	/Change data field to 0 (specifies source field)
7601	1670	/TAD I 7670
7602	6211	/Change data field to 1 (specifies destination field)
7603	3670	/DCA I 7670
7604	2270	/Increment LOC 7670
7605	5300	/JMP .-5
7606	7402	/Halt when transfer complete
7670	0000	

Load address 7600 and press CONT. This routine can also be used to relocate diagnostic programs from one field to the other.

4.2.7 Write All Zeros

Perform the following test to write 0s in all address locations except some locations already occupied by the program. Load address 0004 and deposit the following test routine in sequence:

Location	Contents
0004	1007
0005	3410
0006	5004
0007	0000
0010	0011

Load address 0004 and press CONT. Computer will hang-up and all addresses will contain 0s, except locations occupied by the program. Note: addresses 0004 and 0005 will contain 0s after one program pass.

To write any other word, repeat the same procedures but change address 0007 to the desired word.

SECTION 2 - PREVENTIVE MAINTENANCE

4.3 PREVENTIVE MAINTENANCE INSPECTIONS

This section provides information for performing preventive maintenance inspections. This information consists of visual, static, and dynamic tests that provide better equipment reliability. Preventive maintenance consists of procedures that are performed prior to the initial operation of the computer and periodically during its operating life. These procedures include visual inspections, cleaning, mechanical checks, and operational testing. A log should be kept to record specific data that indicates the performance history and rate of deterioration; such a record can be used to determine the need and time for performing corrective maintenance on the system.

Scheduling of computer usage should always include specific time intervals that are set aside for scheduled maintenance purposes. Careful diagnostic testing programs can then reveal problems which may only occur intermittently during on-line operation.

4.4 SCHEDULED MAINTENANCE

The PDP-8/E must receive certain routine maintenance attention to ensure maximum life and reliability. Digital Equipment Corporation suggests the maintenance schedule defined in Table 4-2.

Table 4-2
Processor Preventive Maintenance Schedule
(3 months or 500 hours)

Type	Action
Cleaning	a. Clean the exterior and interior of the computer cabinet, using a vacuum cleaner and/or clean cloths moistened in nonflammable solvent.
	b. Clean the air filter. Use a vacuum cleaner to remove accumulated dirt and dust, or wash with clean hot water and thoroughly dry before using.
Lubricate	a. Lubricate slide mechanisms and casters with a light machine oil or powdered graphite. Wipe off excess oil.
Inspect	a. Visually inspect equipment for general condition. Repaint any scratched areas.
	b. Inspect all wiring and cables for cuts, breaks, fraying, wear, deterioration, kinks, strains, and mechanical security. Tape, solder, or replace any defective wiring or cable covering.
	c. Inspect the following for mechanical security: key switches, control knobs, lamps, connectors, transformers, fans, capacitors, etc. Tighten or replace as required.
	d. Inspect all module mounting panels to ensure that each module is securely seated in its connector. Remove and clean any module that may have collected excess dirt or dust.

Table 4-2 (Cont)
Processor Preventive Maintenance Schedule
3 months or 500 hours

Type	Action
	e. Inspect power supply components for leaky capacitors, overheated resistors, etc. Replace any defective components.
	f. Check the output of the H724(A) power supply as specified in Table 4-8. Use a multimeter to make these measurements without disconnecting the load. If any output voltage is not within tolerance, the supply is considered defective, and corrective maintenance should be performed.
Perform	a. Run all MAINDEC programs to verify proper computer operation in Table 2-4. Each program should be allowed to run for at least three minutes or two passes, whichever is longer.
	b. Perform all preventive maintenance operations for each peripheral device included in the PDP-8/E System as directed in the individual maintenance instructions supplied with each peripheral device.
	c. Enter preventive maintenance results in log book.

4.4.1 Weekly Preventive Maintenance Schedule

Under weekly maintenance, time should be scheduled each week to operate the MAINDEC programs as listed in Table 2-4. Run each program for a minimum of three minutes. Take any corrective action necessary at this time and log the results. External cleanliness of the system should also be maintained on a weekly basis.

4.4.2 The Importance of a Preventive Maintenance Schedule

Computer downtime can be minimized by rigid adherence to a preventive maintenance schedule. A dirty air filter can cause machine failure through overheating. All filters should be cleaned periodically. The procedure for filter cleaning is described in Table 4-2.

SECTION 3 - CORRECTIVE MAINTENANCE

4.5 MAINTENANCE PROCEDURES

The PDP-8/E is constructed of highly reliable MSI IC logic modules. Use of these circuits and a minimum amount of preventive maintenance ensures relatively little equipment downtime due to failure. If a malfunction occurs, maintenance personnel should analyze the condition and correct it as indicated in the following procedures. Neither special test equipment nor special tools are required for corrective maintenance other than a broad-bandwidth oscilloscope and a multimeter. The best corrective maintenance tool is a thorough understanding of the physical and electrical characteristics of the equipment. Persons responsible for maintenance should become thoroughly familiar with the system concept, logic drawings, operation of specific IC circuits, and location of mechanical and electrical components.

It is virtually impossible to outline any specific procedures for locating faults within complex digital systems such as the PDP-8/E. However, diagnosis and remedial action for a fault condition can be undertaken logically and systematically in the following phases:

a. Preliminary Investigation
b. System Troubleshooting
c. Logic Troubleshooting
d. Circuit Troubleshooting
e. Repairs and Replacement
f. Validation Tests
g. Log Entry

4.5.1 Preliminary Investigation

Before beginning troubleshooting procedures, explore every possible source of information. Gather all available information from those users who have encountered the problem and check the system log book for any previous references to the problem. The troubleshooting flowchart (Figure 4-1) should be used to localize the problem. This flowchart is not a complete guide to determining system fault; it is intended to give the user some thoughts on where a problem could be, a possible solution, and how to describe it to the DEC representative before he arrives on site.

Do not attempt to troubleshoot by use of complex system programs alone. Run the MAINDEC programs and select the shortest, simplest program available that exhibits the error conditions. MAINDEC programs are carefully written to include program loops for assistance in system and logic troubleshooting.

4.5.2 System Troubleshooting

When the problem is understood and the proper program is selected, the logical section of the system at fault should be determined. Obviously, the program that has been selected gives a reasonable idea of what section of the system is failing. However, faults in equipment that transmit or receive information, or improper connection of the system, frequently give indications similar to those caused by computer malfunctions.

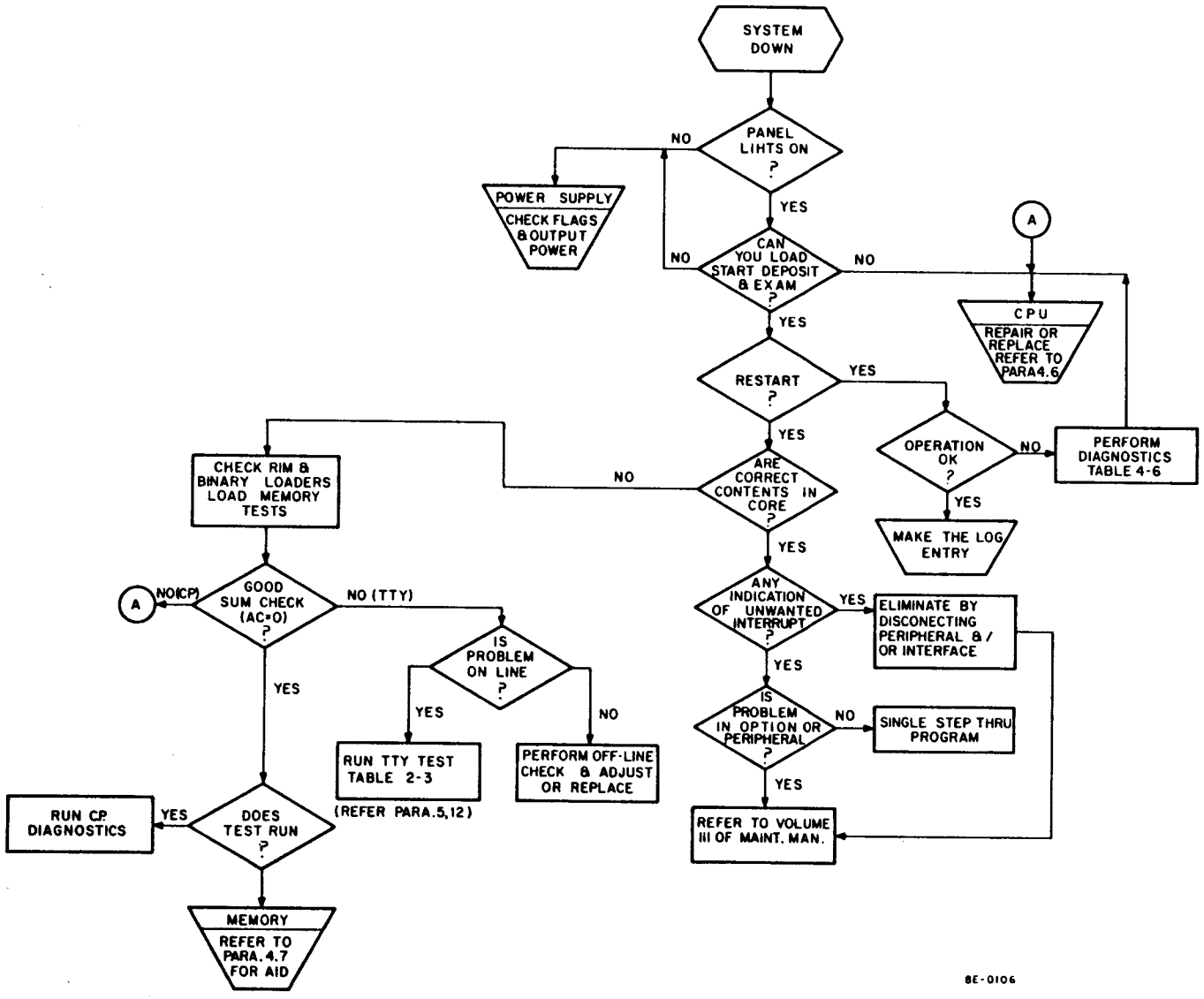


Figure 4-1 System Troubleshooting Flow Chart

Disconnect any peripheral devices that are not necessary to operate the failing program. At this time, reduce the program to its simplest scope loop and duplicate this loop in a dissimilar portion of memory to verify, for instance, that an operation failure is not dependent on memory location. This process can aid in distinguishing memory failures from processor failures. Use of the techniques described above often pinpoints the problem to a module or several ICs.

4.5.3 Logic Troubleshooting

Before attempting to troubleshoot the logic, make certain that proper and calibrated test equipment is available. Always calibrate the vertical preamp and probes of an oscilloscope before using. Make sure the oscilloscope has a good ground via the ac line cord, and keep the ground to the probe as short as possible with the aid of probe ground leads.

To extend the suspected module in the OMNIBUS perform the following procedure:

1 Turn off power.

2 Remove the H851 Edge Connector, if applicable, from the module.

3 Remove the module.

4 Insert two double-extender boards into the same slot.

5 Insert the suspected module into the extender board.

6 If applicable, connect the two edge-connector extender cables (BC08M-OM). This method should be used only with short program loops.

7 Turn power on.

8 Use IC pin extender for signal tracing and for grounding of scope.

NOTE

Test points on individual modules can be observed by connecting the oscilloscope to available pins on the extender.

Use the oscilloscope and IC pin extender to trace signal flow through the suspected logic elements. Oscilloscope sweep can be synchronized by control pulses or by level transitions that are available on individual IC pins at the component side of the module. Exercise care when probing the logic, to prevent shorting between pins. Shorting of signal pins to power supply pins can result in damaged components. Within modules, unused gate inputs are held at +3V.

NOTE

If vibration of the PDP-8/E is desired during troubleshooting, ensure that the vibration is of low enough amplitude that intermodule shorts will not occur.

4.5.4 Circuit Troubleshooting

Engineering schematic diagrams of each module are supplied with each PDP-8/E System and should be referred to for detailed circuit information.

Visually inspect the module on both the component side and the printed wiring side to check for overheated or broken components or etch. If this inspection fails to reveal the cause of trouble or confirm an observed fault condition, use the multimeter to measure resistance of suspected components.

CAUTION

Do not use the lowest or highest resistance ranges of the multimeter when checking semiconductor devices. The X10 range is suggested. Failure to heed this warning may result in damage to components.

Measure the forward and reverse resistances of diodes. Diodes should measure approximately 20Ω forward and more than 1000Ω reverse. If readings in each direction are the same and no parallel paths exist, replace the diode.

Measure the emitter-collector, collector-base, and emitter-base resistances of transistors in both directions. Short circuits between collector and emitter or an open circuit in the base-emitter path cause most failures. A good transistor indicates an open circuit in both directions between collector and emitter. Normally 50Ω to 100Ω exist between the emitter and the base, or between the collector and the base in the forward direction, and an open circuit condition exists in the reverse direction. To determine forward and reverse directions, consider a transistor as two diodes connected back to back. In this analogy, PNP transistors would have both cathodes connected together to form the base, and both the emitter and collector would assume the function of an anode. In NPN transistors, the base would be a common-anode connection; and both the emitter and collector, the cathode.

Multimeter polarity must be checked before measuring resistance, because many meters apply a positive voltage to the common lead when in the resistance mode.

ICs contain complex integrated circuits with only the input, output, and power terminals available; thus, static multimeter testing is limited to continuity checks for shorts between terminals. IC checking is best done under dynamic conditions using a module extender to make terminals readily accessible. Using PDP-8/E logic diagrams and M-series module schematics, locate an IC on a circuit board as follows:

1 Hold the module with the handle in your left hand; component side facing you.

2 ICs are numbered starting at the contact side of the board; upper right-hand corner.

3 The numbers increase toward the handle.

4 When a row is complete, the next IC is located in the next row at the contact end of the board (Figure 4-2).

5 The pins on each IC are located as Figure 4-3 illustrates.

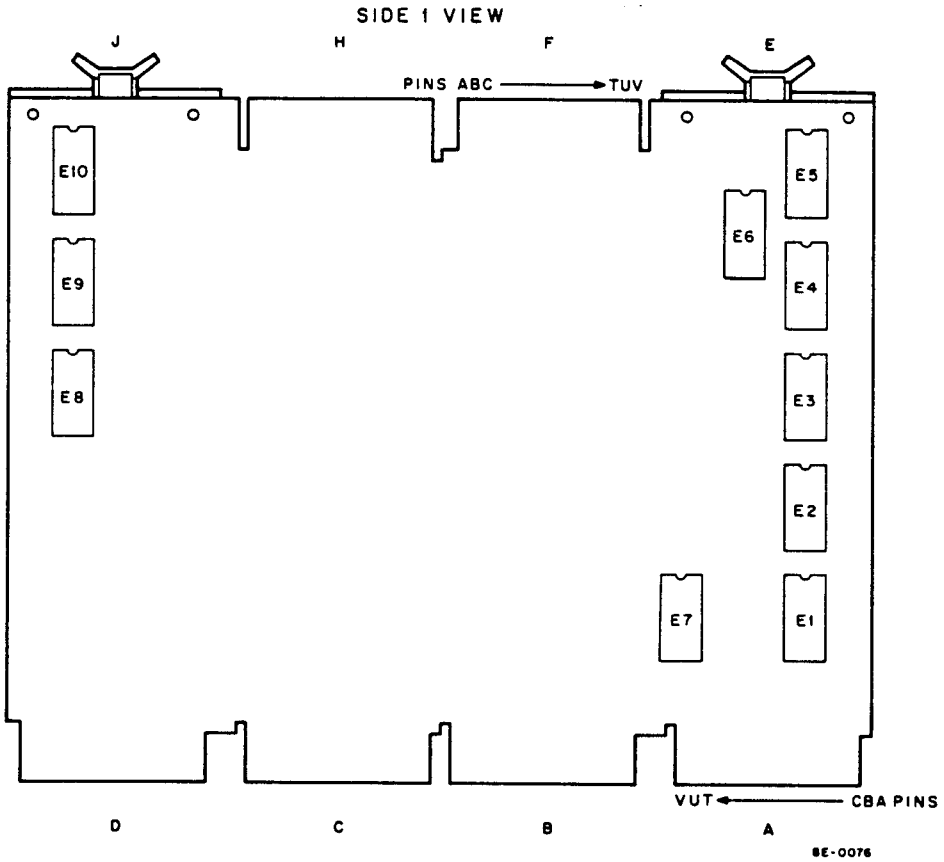


Figure 4-2 IC Location

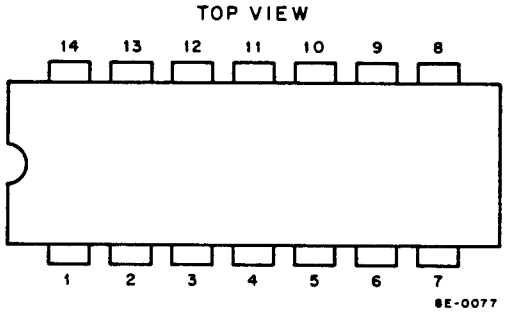


Figure 4-3 IC Pin Location

4.5.5 Repairs and Replacements

When soldering semiconductor devices (transistor, diodes, rectifiers, or integrated circuits) that can be damaged by heat, physical shock, or excessive electrical current, take the following special precautions:

1 Use a heat sink, such as a pair of pliers, to grip the lead between the joint and device being soldered.

2 Use a 6V iron with an isolation transformer. Use the smallest iron adequate for the work. Use of an iron without an isolation transformer can result in excessive voltages presented at the iron tip. Use only pencil-pointed tip soldering irons on PC boards.

3 Perform the soldering operation in the shortest possible time to prevent damage to the component and delamination of the module etched wiring.

4 ICs can be removed by using a solder puller to remove all excessive solder from contacts. Then, by straightening the leads, lift the IC from its terminal points. If it is not desired to save the defective IC for test purposes, perform Steps 5 through 12. If the IC is to be saved, perform Steps 8 through 12 (remove IC following Step 8).

5 Clip IC leads at top of lead at the connection to chip.

6 Remove chip portion of IC.

7 Apply heat to individual leads from siside #1 and remove leads slowly from side #1, using a pair of needle nose pliers. Do not hold lead with pliers while applying heat; the pliers will act as a heat sink.

8 Turn board over to side #2 and heat each hole individually, removing excess solder with desoldering tool.

9 Insert new component, bending appropriate leads. (Only leads with tear drop lands should be bent. They should be bent in the direction of the point.)

10 Clip protruding component leads from side #2. Do not cut flush with the board. (Leads and solder joints cannot exceed 1/16 in. from bottom of board.)

11 Solder all leads on side #2.

12 Clean flux from both sides of board with TRICHLORETHYLENE, FREON, or equivalent. *Be careful – both substances will damage the plastic handle.*

In all soldering and unsoldering operations in the repair and replacement of parts, avoid placing excessive solder or flux on adjacent parts or service lines. When repair has been completed, remove all excess flux by washing junctions with a solvent such as trichlorethylene. Be very careful not to expose paint or plastic surfaces to this solvent.

CAUTION

Never attempt to remove solder from terminal points by heating and rapping module against another surface. This practive can result in module or component damage. Remove solder with a solder-sucking tool or solderwick.

When removing any part of the equipment for repair and replacement, make certain that all leads or wires that are unsoldered, or otherwise disconnected, are legibly tagged or marked for identification with their respective terminals. Replace defective component only with parts of equal or better quality and equal tolerance.

To remove a switch on the Programmer's Console, follow the procedure below:

1 Turn power off.

2 Loosen Allen screw and remove knob from rotary switch.

3 Remove four screws from Bezel.

4 Carefully remove the face plate.

5 Remove two screws retaining aluminum mounting bracket.

6 Remove two wires from tab terminals on the left-hand side of the console.

7 Remove Programmer's Console board.

8 Remove faulty switch.

9 When replacing the panel, the yellow wire goes to the top tab terminal and blue wire to the bottom.

To remove the power supply heat sink assembly (Paragraph 4.8), follow the procedure below:

1 Remove ac power by turning off CB1 and disconnecting the ac plug.

NOTE

If the PDP-8/E is rack-mounted, remove carefully and place on table.

2 Remove the power supply assembly from the chassis as follows:

a. Remove five Phillips-head screws. Two are located on the front side of the chassis, one on the rear side, and two are located on the back side.

NOTE

If the PDP-8/E is rack-mounted, the chassis tracks and the five mounting screws must be removed.

b. Unplug the OMNIBUS power and switch power harness.

c. Lift up the power supply and slide it back just far enough to remove the blue and the yellow power wires from the front panel.

d. Lift out the power supply.

3 Remove the protective screen from the side of the power supply by removing the 12 countersunk screws on the screen.

4 Remove the heat sink assembly as follows:

a. Remove the nylon plug from the heat sink assembly bracket.
b. Remove the six screws from the heat sink assembly bracket.
c. Lift out the heat sink assembly.

5 During replacement, the yellow wire goes to the top tab terminal of the front panel.

4.5.6 Validation Tests

If a defective module is replaced by a new one while repairs are being made, tag the defective module noting the nature of the failure. When repairs are completed, ascertain that the repairs have resolved the problem.

To confirm that repairs have been completed, run all tests that originally exhibited the problem. If modules have been moved during the troubleshooting period, return all modules to their original positions before running the validation tests.

4.5.7 Log Entry

A log book is supplied with each PDP-8/E System. Corrective maintenance is not complete until all activities are recorded in the log book. Record all data indicating the symptoms given by the fault, the method of fault detection, the component at fault, and any comments that would be helpful in maintaining the equipment in the future.

The log book should be maintained on a daily basis, recording all operator usage and preventive maintenance results.

4.6 CPU TROUBLESHOOTING

After it is established that the CPU is causing the problem (Figure 4-1), Table 4-3 can be used as a troubleshooting aid to isolate the problem. The symptoms and causes are examples that may help the computer technician to find the area in which to look, once an abnormal indication is noted on the Programmer's Console.

When troubleshooting the PDP-8/E, remember that the OMNIBUS is designed so that all pins that are lettered the same are connected to each other, and that a signal can be provided from more than one place. An example is MD6, which is on pins BM1 of all slots of the OMNIBUS. The source of MD06 can come from either the Major Register module (M8300) or the Sense/Inhibit module (G104) and is used by five of the nine modules in the basic computer. To find the source and destination of all the signals used in the basic computer, refer to Appendix B.

4.7 MEMORY TROUBLESHOOTING

After it is established that the memory is the source of the problem through symptom analysis using the system troubleshooting flowchart (Figure 4-1), the memory troubleshooting flowchart (Figure 4-4) and associated troubleshooting Tables 4-4 and 4-5 and waveforms in Figure 4-5 may be used to isolate the problem.

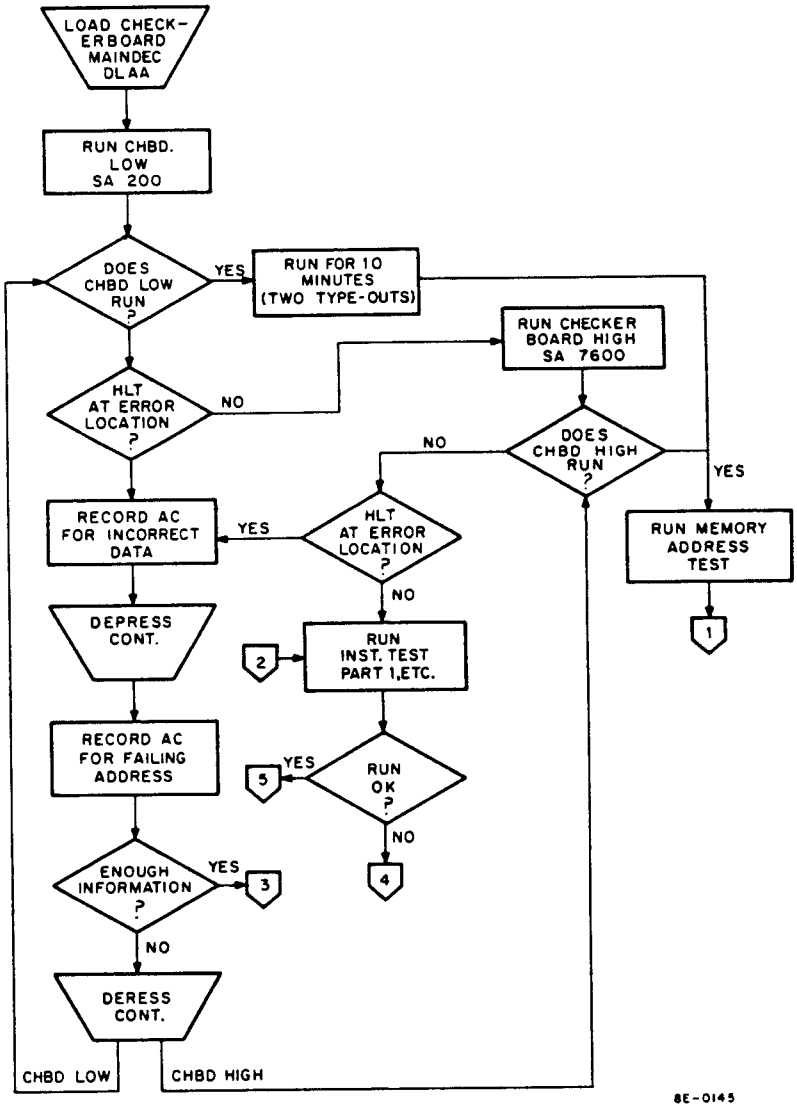


Figure 4-4 Memory Troubleshooting Flowchart (Sheet 1 of 2)

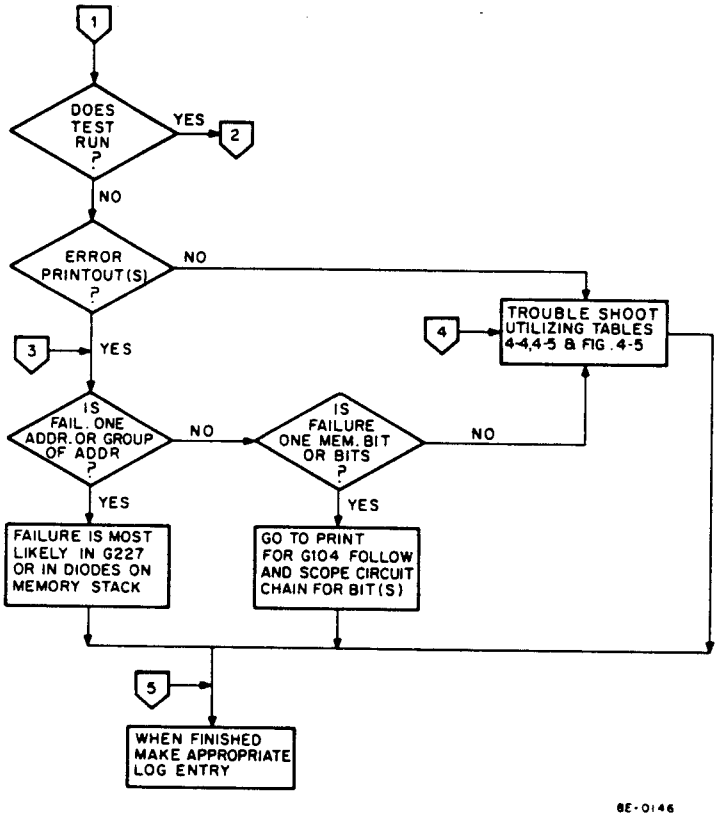


Figure 4-4 Memory Troubleshooting Flowchart (Sheet 2 of 2)

4.7.1 Memory Resistance Checks

There are also some resistance checks that can be performed to aid in isolating a trouble in the memory. These resistance checks are summarized below:

1 Turn power off.

2 Remove memory stack module.

3 Resistance of thermistor network is approximately 150Ω.

4 Resistance of individual thermistor when out of the circuit is approximately 56Ω.

5 Resistance of winding for one bit is approximately 3Ω (for example, between pins FA and FB for bit 6).

6 Resistance of diodes FSA2501 is as follows: Forward – approximately 24Ω; Reverse – approximately greater than 1MΩ.

CAUTION

Metal can transistors have their casing connected to the collector. Care should be exercised to prevent a ground lead or the back of another module from touching the metal can during troubleshooting.

Table 4-3
Processor Troubleshooting

Item	Symptom	Likely Cause	Module
1	A signal on the OMNIBUS is always low.	Bus loads, diode from GND to the OMNIBUS is shorted.	M8320
2	Unable to start automatic operations (run light always off).	a. Missing MEM START L, which is a 300 to 500 ns pulse for everytime CONT, DEP, or EXAM key is depressed. b. Power OK "delayed" or Power OK is true.	M8330 and KC8-E
3	Unable to change Major States.	Missing CPMA LOAD L. MA, MS LOAD CONT L grounded.	M8310
4	Unable to modify any memory locations.	a. MB LOAD b. Memory direction always low c. INHIBIT always low d. WRITE L stays low e. SOURCE stays low f. FIELD L is high (Refer to Table 4-4, Memory Data Errors.)	M8310 M8330 M8330 M8330 M8330 G104
5	Data from memory is not getting to the MB.	a. Memory direction always high b. No MB LOAD L c. No TIME STROBE d. WRITE L staying high (Refer to Table 4-4, Memory Data Errors.)	M8330 M8310 G104 M8330
6	When loading an address, the word in the MA is not the same as the Switch Register.	LA ENABLE is always high (this causes the switch register to be ORed with AC, MQ, or STATUS if the rotary switch is in one of these positions).	KC8-E
7	When using LOAD ADDR, DEPOSIT, or EXAM, the MA changes to an incorrect value (EX:0020 → 0634).	EN0, EN1, EN2 or LEFT L, RIGHT L, TWICE L are an incorrect level. Refer to truth table on M8310 logic print, sheet 3 of 3.	M8310
8	Depressing ADDR LOAD key will enter all 1s in the MA. By examining and observing the MD, it will be noted that the register will change when the key is released.	DATA T always high.	M8310

Table 4-3 (Cont)
Processor Troubleshooting

Item	Symptom	Likely Cause	Module
9	The MA decrements when doing an EXAM or DEPOSIT.	DATA F is always low. Refer to truth table on M8310 logic print, sheet 3 of 3.	M8310
10	When doing an EXAM, DEPOSIT, CONTINUE, or a JUMP instruction, the MA bits 0 – 4 are zeroed.	PAGE Z L is high. (If just one of MA 0 → 4 check PAGE Z circuit on M8300.)	M8310 M8300
11	CPMA, MB, PC, or AC do not increment.	CAR IN L is always high to the adder. It should be generated for: a. During TS1 with DEPOSIT, EXAM, or EX TO LOAD depressed. b. TS1 of FETCH state. c. TS2 of DEFER state. d. EXECUTE state and TS2 of an ISZ, or TS3 of a JMS. e. TS3 of a Group 2 OPR instruction. f. If SKIP is set: TS2 of EXECUTE doing a JMS, or TS4 of a MRI.	M8310
12	Unable to SKIP on an ISZ instruction.	a. SKIP F/F will not clear. b. No "carryout". c. No "overflow".	M8310
13	Information being read from Teletype is loading into MA and PC.	C2 L is always low, which causes PC LOAD at BUS STROBE (TP3) time instead of AC loading.	M8320 M8310 M8330

Table 4-4

Memory Data Errors – Possible Causes

Symptom	Cause	Module	Check
One Bit = 1 OR 0	Inhibit Driver	G104	Collector of 2007 transistors
One Bit = 1 OR 0	Sense Amplifier	G104	E31-42 Pin 8
Random = 1 OR 0	Time Strobe	G104	E9-3
Random/All = 0	XY current/voltage is low	G227	≈5.3V across +5V and Pin JU2
Random/All = 1	XY current/voltage is high	G227	Same as above
Random/All = 1	Slice voltage low	G104	≈5.3V across GND and test point DA1
Random/All = 0	Slice voltage high	G104	≈5.3V across GND and test point DA1
Random/All = 1	Inhibit current/voltage low	G227	-15 Vdc power
Random = 0	Inhibit current/voltage high	G227	-15 Vdc power

Table 4-5

Memory Module Test Point Voltage Levels

Signal	Pin	Module	Approximate Readings
Current Control	HA1	G104	1.2V
	HV2	G104	2.3V
Current Source	JU2	G227	1.4V
	FU2	G104	0.25V
Test Point	DA1	G104	-5.3V
Test Point	CB1	G104	6V
Test Point	DB1	G104	-6V
Current Source	HU2	G104	4V
	FA1	G104	2.3V
	FB1	G104	-4V
	Q17 Emitter	G104	-4.8V
Memory Stack	Top of Thermistor		2.5V
Test Points	Q18 Collector	G104	-6V
	Q15, 16 Emitter	G104	+3V
	Q13 Base	G104	+1.3V

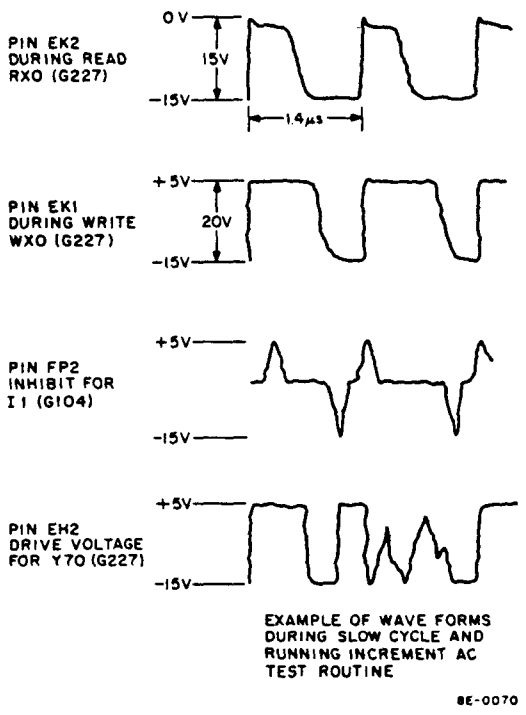


Figure 4-5 Memory Waveforms

4.7.2 Memory Circuit Variables

There are a number of variables in the MM8-E memory system such as current, slice, and field, that have to be set properly. Although some of the settings are permanent for a particular board, interchangeability in the field is assured. These variables are summarized in Table 4-6 and detailed in the following paragraphs.

Table 4-6
Memory Circuit Variables

Variables on MM8-E Memory System	Means for Settings	Location	Who Makes the Settings
Field Select	3 Jumpers EMA0, EMA1, EMA2	G104	Factory or Field Service
Strobe	6-position rotary switch	G104	Factory or Field Service
Slice	2 Jumpers – SLA, SLB	G104	Factory only
X/Y Current Control	2 Jumpers – CCA, CCB	G227	Factory only
Temperature Tracking	Thermistor-Resistor Combination RT, R1, R2, R3	G619	Factory only

4.7.3 Field Select Jumpers

The octal combination of the appropriate *cut* jumpers represents the selected field; therefore, for the basic system (no extended memory), all jumpers must be in place.

4.7.4 Strobe Adjustment

A 6-position rotary switch optimizes the strobe positioning in discrete steps of 10 ns. For detailed setting procedures, refer to Paragraph 4.7.9.

4.7.5 Slice Level

Any variation on the +5V power supply will cause a proportional change of the absolute value of the slice level.

The slice level can be set to four different levels according to the following truth table:

Jumpers		Slice Level (Testpoint DA1 on G104)
SLA	SLB	
In	In	-4.3V
Cut	In	-4.8V
In	Cut	-5.3V
Cut	Cut	-6.0V

NOTE
Do not field-adjust the slice level under any circumstances.

4.7.6 X/Y Current Control (G227)

On the G227 module there are two jumpers in the upper center of the module. These jumpers can be removed and a 24 AWG wire loop soldered in their place if it is necessary to measure currents with a current probe.

The X/Y current control can be set to four discrete levels to calibrate the current source. The nominal voltage varies with temperature and its corresponding X/Y current is 370 mA measured on a loop between the X/Y drive and the stack board. The pertinent truth table follows:

Jumpers		Current Control Voltage (Voltage across +5V and Pin JU2 on G227)
CCA	CCB	
In	In	+3.7%
In	Cut	+2.2%
Cut	In	Nominal (~3.5V at 25°C)
Cut	Cut	-1.7%

NOTE
Do not field-adjust current control voltage under any circumstances.

4.7.7 Temperature Tracking

A thermistor-resistor combination on the memory stack board provides a temperature-sensitive voltage divider, which is connected to the current control circuit.

4.7.8 Inhibit Current

The inhibit current is fixed; however, it varies proportionally to the -15V supply; its corresponding nominal value is 340 mA.

4.7.9 Strobe Setting Procedure

Setting the strobe properly is very important and must be done carefully. The chosen setting scheme makes this procedure relatively simple. Figure 4-6 illustrates the relation between X/Y current sense amplifier output and strobe.

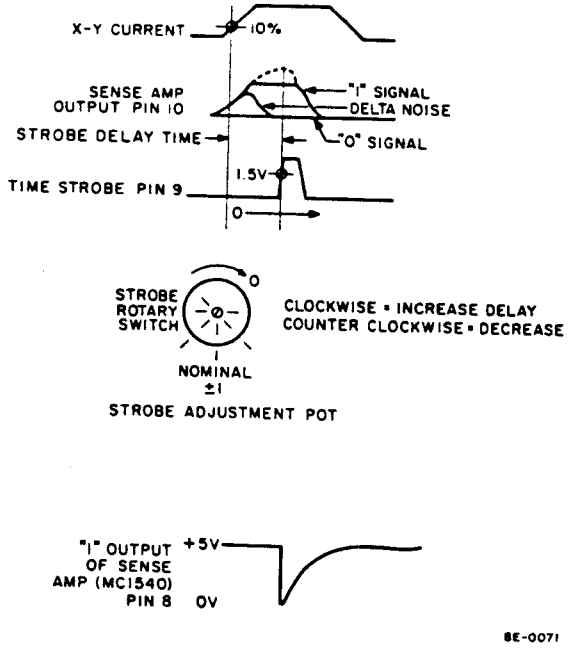


Figure 4-6 Setting of Strobe

It is not advisable to set the strobe timing using an oscilloscope and a current probe. Because of the length of the current probe cables, the bandwidth of the probe and scope may vary in each case.

The resulting correlation error can exceed the tolerance allowed, resulting in a misadjusted memory. To set the strobe accurately, perform the following procedure at room temperature:

1 The switch has to be set to one of the three possible nominal positions (Figure 4-6).

2 Load "Memory Checkerboard" maintenance program and run it.

3 Program should run without error.

4 Halt program and delay strobe 10 ns (1 position clockwise), then restart.

5 If program still runs without error, proceed to the next position. When errors occur, stop and memorize this strobe position.

6 Repeat the same procedure advancing the strobe (counterclockwise) until errors occur, then stop and memorize this position.

7 A reliable system has to have a minimum of three working consecutive positions.

8 Finally set strobe to the middle working position. If there is an even number of working positions, favor the most delayed (clockwise) of the two center positions.

9 In checkout, "Checkerboard" should always run in the middle position and, for at least 15 minutes, in the positions to the left and right of middle with no errors.

10 Acceptance is to be run only in the final strobe position.

11 Setting strobe for extended memories, load basic memory checkerboard (MAINDEC-8E-D1AA-D) into extended fields and proceed to set strobe position according to Steps 1 through 10.

4.8 H724 POWER SUPPLY TROUBLESHOOTING PROCEDURES

The H724 Power Supply provides power for CPU logic, the memory, bus loads, and the lamps on the Programmer's Console. If the power supply is established to be the source of the problem through symptom analysis with the aid of the system troubleshooting chart (Figure 4-1), voltage checks should be performed. Voltages and tolerances are given in Table 4-7. A component troubleshooting aid, Table 4-8, and parts location, Figure 4-7, are included as aids to isolating and correcting the malfunction.

The following paragraphs describe some of the power supply features and characteristics that can aid in isolating the malfunction.

Table 4-7
H724 Power Supply Parameters

Output Voltage	Wire Color	Minimum Voltage	Maximum Voltage	Tolerance	Current Rating	Maximum Ripple
+5V	Red	4.85V	5.15V	± 3%	20A	50 mV p-p
-15V	Blue	-14.25V	-15.75V	± 5%	8A	50 mV p-p
+15V	Orange	13.5V	16.5V	± 10%	1A	75 mV p-p
+8V	Yellow	6V	10V	± 26%	2A	
dc Volts OK	Grey	3.75V	5V			
Overvoltage Protection			6.5V			
14 Vac				± 26%	0.2A	
AC INTLK					0.12A	

Table 4-8

Component Troubleshooting Aid for H724 Power Supply

Output Volts	Wire Color	Jack & Pin	Fuse (amps)	Module	Transistors	Adjustment	Use
+5 Vdc	Red	J3-3 J4-3	25	A2	Q200 Q201-6	R21	CPU Logic
-15 Vdc	Blue	J3-4 J4-4 J6-3	10	A1	Q300 Q301 Q304	R5	Memory
+15 Vdc	Orange	J3-5 J4-5	1	A1	Q100	R5	Bus Loads
+8 Vdc	Yellow	J6-4	25				Lights
14 Vac	-	J5-1 J5-3	.5				Options
Overvoltage Protect	-			A2			Power Surge
dc Volts OK (3.75)	Grey	J3-6 J4-6		A2		R29 (Factory Adjustable Only)	Power Loss

Static ohmeter reading of thermistor is approximately 23Ω.

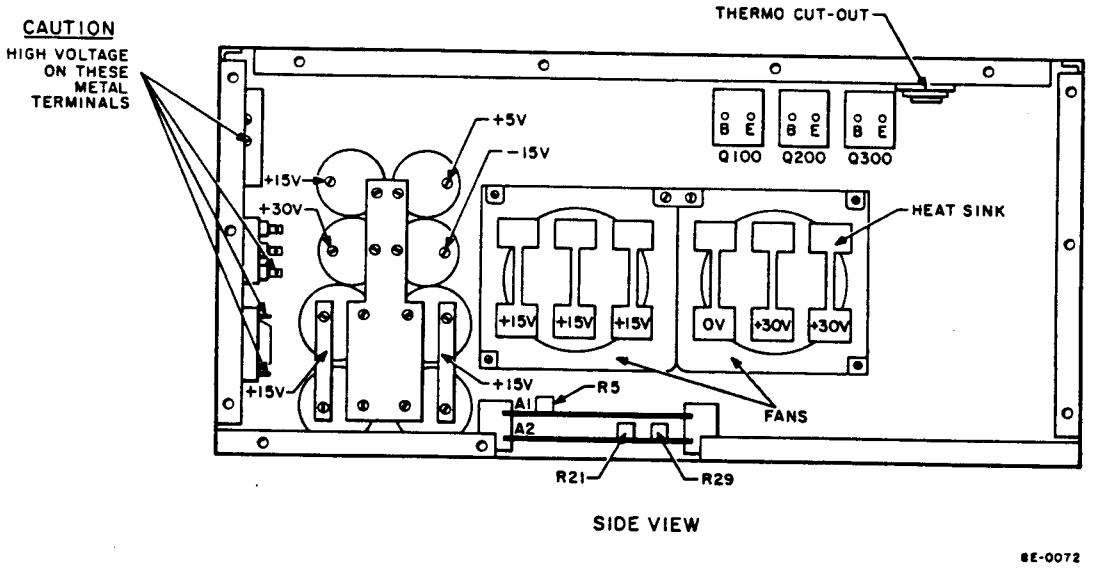


Figure 4-7 H724 Power Supply

4.8.1 Overcurrent Protection

The power supply should not be loaded by more than 175 percent of the rated output current (Table 4-7).

4.8.2 Hold-Up Time

The regulated output voltages under maximum load conditions should remain stable for a minimum of 2 ms after loss of line voltage.

4.8.3 Thermal Protection

A thermal switch is in series with the interlock circuit. This switch is located in the forward top section of the power supply (Figure 4-6). It will disconnect primary power at 90°C ±5°. The thermal switch must be reset manually if it is tripped.

4.8.4 Contact Protection

Contact protection is provided to limit the primary power at the input to the convenience outlet to twice the nominal peak voltage. In addition, protection is provided against a rate of change in the voltage exceeding 10V/second as the solenoid or circuit breaker is opened.

4.8.5 Input Switching

The primary power is switched by a 24 Vdc relay, controlled by an interlock circuit. Grounding pin A on the interlock panel will operate the solenoid and apply power to the computer. The solenoid will break both sides of the line.

4.8.6 Power ON-OFF Switch Adjustment

The Power ON-OFF switch is cam-adjusted according to Table 4-9.

Table 4-9
Power ON-OFF Switch Adjustment

Power Switch Position	Three Cam-Operated Switches Switch Position	
	Back 2 Switches	Front Switch
OFF	ON	OFF
ON	ON	ON
Panel Lock	OFF	ON

4.8.7 Parallel Operation

Two or more power supplies must not be wired in parallel to extend the current driving capability.

4.8.8 Large Configuration

When more than one box is in the sytem, the interlock panel is wired so that the front panel power switch of the first box and the thermal cut-out switch of each additional box are in series and will control power to all boxes, though they may be connected to independent primary power sources.

4.9 H740 POWER SUPPLY TROUBLESHOOTING PROCEDURES

4.9.1 Troubleshooting Rules and Precautions

Observe the following rules and precautions when maintaining the power supply.

1 Do not adjust voltages beyond their 105 percent rating; adjust slowly to avoid overvoltage crowbar that blows dc output fuses.

2 Use a calibrated voltmeter, preferably a digital voltmeter. Voltages should be adjusted to their center values: +15.0, +5.0, and - 15.0, all under load at the dc cable termination.

3 Ensure that power is turned off and unplugged before servicing the power supply.

4 Ensure that input capacitors C1 and C2 are discharged before servicing the power supply. A 10Ω to 100Ω, 10W resistor can be used to hasten the discharge of the capacitors. (Ensure power is off.)

5 The dc regulator module is not internally grounded to the chassis. Therefore, shorts to ground can be located after disconnecting the dc output cable.

6 The dc output fuses, F1 and F2, can be replaced without removing the dc regulator module. Before unsoldering fuses, observe cautions described in 3 and 4.

7 For proper operation, all hardware must be secured tightly to about 12 inch pounds (i.e., capacitors, chokes, semiconductors). All hardware should be replaced with identical hardware replacement parts.

8 The dc regulator module can be removed from the top of the power chassis assembly while the latter is still bolted to the computer chassis. The dc regulator module is held in place by six screws.

9 When replacing power semiconductor components that are secured to the heat sink, apply a thin coat of Wakefield #128 compound or Dow silicone grease to heat sink contact side (bottom) of the semiconductor. Insulating wafers are not required.

4.9.2 Troubleshooting Chart

The most likely source of a power supply malfunction is the dc regulator. A quick remedy for a malfunction is to replace this entire module. The problem, however, could be a short in the system unit or possibly a defective component or other problem in the ac input circuit. Table 4-10 applies to the regulator module and helps to isolate problems in this area.

Table 4-10
Regulator Module Troubleshooting Chart

Problem	Cause
No +5V and +15V output	F1 opened D14 or transformer opened +5V adjusted too high (1)
+5V output too low	Q5, D9, Q10, Q9, Q11, D12, or D10 shorted C5 or C7 shorted R49, R50, R46, or R44 opened Q6, Q7, Q8, or D11 shorted A9, Q10, or D9 opened (1) R51 or R50 opened
+15V output too high	Q1 shorted D8 opened R35 or R36 opened
+15V output too low	Q3, Q4, Q5, or D8 shorted R56, R35, or R34 opened C19 shorted
-15V output too low	F2 opened D14 or transformer opened Q25, D4, Q26, Q21, Q27, D7 or D5 shorted C14 or C12 shorted R22, R26, R25, or R29 opened Q22, Q23, Q24, or D6 shorted Q25, Q26, or D4 opened R26 or R27 opened (1) -15V adjusted too high (1)
AC LO L will not go high	Q13, Q14, or Q15 shorted Q16 or D3 opened R7, R3, R6, or R8 opened C9 shorted
AC LO L will not go low and/or acts erratically on power-on/power-off	Q13, Q14, or Q16 opened Q15 or D3 shorted R12, R13, R7, or R10 opened

SECTION 4 - TELETYPE MAINTENANCE

This section contains information pertinent to the maintenance of the TTY and associated control logic. Perform the test routines described in Paragraph 4.2 to localize trouble in the Teletype.

4.10 SPECIAL TOOLS

Table 4-11 lists the special tools needed to maintain the 33 ASR Teletype. All of these items can be obtained from Digital Equipment Corporation or from Teletype Corporation.

4.11 PROGRAMS

The Teletype control test referenced in Table 2-4 serves as an aid in maintaining the 33 ASR Teletype and associated control logic.

Table 4-11
Teletype Maintenance Tools

Item	Part No.
Set of gauges	117781
Offset screwdriver	94644
Offset screwdriver	94645
Handwheel	161430
Handwheel adapter	181465
Contact adjustment tool	172060
Gauge	180587
Gauge	180588
Gauge	183103
Bending Tool	180993
Extractor	182697
Tweezer	151392
Spring hook (push)	142555
Spring hook (pull)	142554
Screw holder	151384

SECTION 5 - PREVENTIVE MAINTENANCE PROCEDURES

4.12 PREVENTIVE MAINTENANCE

Teletype preventive maintenance should be scheduled every 3 months.

CAUTION

Do not use alcohol, mineral spirits, or other solvents to clean plastic parts with protective decorative finishes. Normally, a soft, dry cloth should be used to remove dust, oil, grease, or otherwise clean parts or subassemblies.

To clean plastic surfaces, we recommend using any of several household cleaner-waxer liquids. To clean the printer platen, we recommend a lacquer thinner.

During an overhaul, subassemblies and metal parts can be cleaned in a bath of trichlorethylene. Proper lubrication should be performed often.

4.12.1 Weekly Tasks

The following procedures should be followed on a weekly basis.

1 Inspect platen and paper guides. Wipe clean, using a soft, dry cloth.

2 Clean external areas of paper-tape punch and reader, using a soft brush or cloth.

3 Remove and empty the paper-tape punch chad box.

4 Run the Teletype control test for approximately 15 minutes.

4.12.2 Preventive Maintenance Tasks

Follow the procedure outlined below.

1 Inspect platen and paper guides. Clean platen, using a lacquer thinner to remove shiny surface.

2 Clean ribbon guides and replace ribbon, if necessary.

3 Remove cover and check for vibration effects, loose nuts, screws, retaining clips, etc.

4 Clear distributor rotor and clean disk surface, using cotton swab moistened in freon or trichlorethylene.

5 Clean between selector magnet-pole piece and armature with bond paper to remove any lubricant or dirt.

6 Clean and lubricate the Teletype, per Teletype Bulletin 273B. Follow instructions literally; do not over lubricate.

7 The following adjustments should be checked. Pages indicated are in Bulletin 273B, Volume 2.

Trip Shaft	574-122-700 Page 13
Trip Lever	574-122-700 Page 14
Brush Holder (Distributor)	574-122-700 Page 15
Clutches	574-122-700 Pages 16-24
Code Bar Reset	574-122-700 Pages 30-34
Print Suppression	574-122-700 Page 35
Blocking Levers	574-122-700 Page 37
Print Suppression	574-122-700 Page 43
Carriage Drive Bail	574-122-700 Page 44
Print Trip Lever	574-122-700 Pages 61-62
Dashpot	574-122-700 Page 78
Final Printing Alignment	574-122-700 Page 85
Line Feed	574-122-700 Pages 89-95
Keyboard Trip Lever	574-122-700 Page 141
Reader Trip Lever	574-124-700 Pages 6-9
Detent Lever	574-124-700 Page 10
Sensing Pin	574-124-700 Page 15
Tape Lid Latch Handle	574-124-700 Page 18
Feed Pawl	574-125-700 Page 11
Registration	574-125-700 Page 12

8 Run each of the Teletype MAINDEC Programs; at least two passes each.

9 Check that tape holes are being punched cleanly.

4.13 CORRECTIVE MAINTENANCE PROCEDURES

Details of the cable connector fusing and test points are included in Tables 4-12 and 4-13. During off-line operation, the keyboard distributor effectively drives the printer selector magnet; thus, any character received from the keyboard or paper-tape reader is automatically reproduced on the printer and paper-tape punch. During on-line operation, this continuity is broken and a Teletype receiver (M8650) is used to accept the input from the reader or keyboard while a Teletype transmitter (M8650) is used to drive the printer and paper-tape punch.

Table 4-12
Connections of TTY Cable

33 ASR Connections	W076D Split Lug	Mate-N-Lok Pin No.	M8650 Split Lug	Keyboard	Printer	Reader Advance
		1 (N/C)	0 (N/C)			
T.B. Pin #6	6	2	2		X	
T.B. Pin #3	3	3	3	X		
*-15	-Relay	4	4			X
T.B. Pin #7	7	5	5		X	
*To CP (F)	+Relay	6	6			X
T.B. Pin #4	4	7	7	X		
	-30V (N/C)	8 (N/C)	0 (N/C)			

*Wheelock Relay Card

Table 4-13
TTY Cabling, Fusing and Test Points

Check	Reader	Receiver	Transmitter
Fuses	.1/2A		3, 3/8, 2.5, 3A
Terminal No.	6 and 4	7 and 3	5 and 2
Test Points	DA1 Reader Run	AB1 Receiver Active '1'	

A crystal clock is used to shift the bits through the transmitter and receiver buffers; therefore, no clock adjustments are required. Most Teletype problems can be traced to one of three areas:

a. 33 ASR keyboard or reader
b. 33 ASR printer or punch
c. M8650 receiver/transmitter

Isolation of bit-related problems is relatively simple. Off-line duplication can usually determine whether the problem is in the teleprinter or the control logic. Steps may be taken to isolate the problem to subassemblies within the teleprinter. Picking up bits during a read operation can be caused by a defect in any of three sets of contacts that are tied in parallel. Reader, keyboard, and answer-back contacts provide parallel inputs to the distributor contact disk. Bit pick-up problems can be isolated to one of these three areas by disengaging the related contact from the suspected contact set.

Printer/punch problems can sometimes be isolated by comparing the printed character with the output of the paper-tape punch. If the printed character agrees with the punch output, and both are incorrect, then the problem lies in the selector mechanism or in the TTY receiver/transmitter module (M8650). If the printed character and the paper-tape punch output disagree, and the paper-tape punch output is correct, then the problem lies within the printer assembly. Figure 4-8 shows the Teletype signal relationship between the computer and the Teletype.

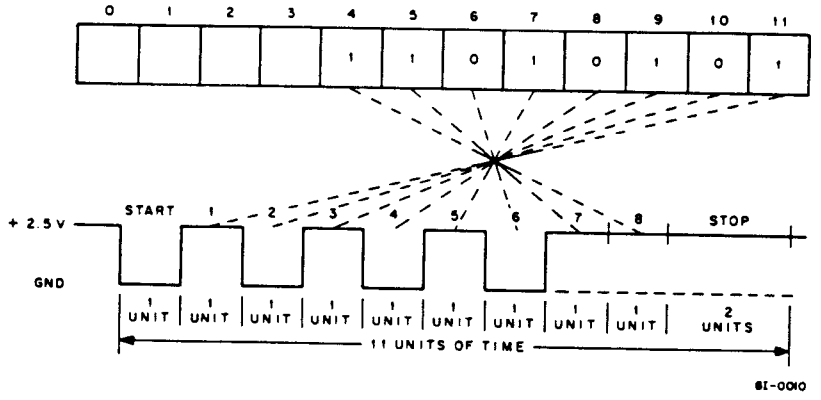


Figure 4-8 Teletype Signal Waveform
and Bit Relationship for the Character "U"

SECTION 7 - I/O CABLE TROUBLESHOOTING

4.14 I/O AND BREAK CABLES

Pin assignments for the positive I/O adapter module and break are provided in Figure 9-20 of the *PDP-8/E & PDP-8/M Small Computer Handbook*. The figure provides a source and destination in the event that cable troubleshooting is necessary.

SECTION 8 - SPECIAL TROUBLESHOOTING PROCEDURES

4.15 TEST CLOCK (M499)

The test clock module serves as a troubleshooting tool for the PDP-8/E when problems with memory prevent the use of troubleshooting programs. The M499 module provides a MEM START signal of 100—500 ns width every 15 μs with the DEP or EXAM key depressed. This procedure makes signals available for associated troubleshooting at a continuous rate. Troubleshooting procedures using the M499 Test Clock are as follows:

1 Insert M499 into any slot in row A of PDP-8/E OMNIBUS.

2 Depress the SING STEP key on the Programmer's Console.

3 The Switch Register may now be used in conjunction with the EXAM or DEP key to scope manual functions.

4 The EXAM or DEP key may be taped into the depressed position (thus leaving the operator free).

SECTION 9 - PREPARATION FOR RESHIPMENT

4.16 RESHIPMENT

If the computer must be moved to a location far removed from the original installation, good packaging procedures should be followed. If the original packing materials have been retained, the instructions given below will ensure that the computer is transported safely.

1 Disconnect the computer and remove it from its enclosure.

2 If the computer is a PDP-8/F or PDP-8/M, remove the chassis tracks and ship them separately; remove the filter from the side of the computer. If the computer is a PDP-8/E table-top model, remove the air filter from both sides of the super cover and ship them with cables, software, manuals, etc.

3 Roll the power cord and tape it to the rear of the computer.

4 Place the computer in a polyethylene bag and seal the bag with tape.

5 Use the original packing materials to pack computer and accessories snugly in an inner carton.

6 Seal the inner carton, place the inner carton in an outer carton, and seal the outer carton.

CHAPTER 5
SPARE PARTS

5.1 INTRODUCTION

This chapter lists the recommended spares for the PDP-8/E, PDP-8/F, and PDP-8/M basic computers and for the 33 ASR Teletype. Two levels of spares are recommended, viz., "Remove and Replace at the Module Level" and "Remove and Replace at the Component Level".

5.2 PDP-8/E SPARES

5.2.1 PDP-8/E First-Level Spares

First-level spares for the PDP-8/E basic computer, which are included in spare parts option kit SP8-EA, are listed in Table 5-1. Table 5-2 lists those parts that are not recommended as spares. Additional spares may be purchased separately.

Table 5-1
PDP-8/E Recommended First-Level Spares

Part No.	Description	Quantity
M8300	Major Registers Module	1
M8310	Major Register Control Module	1
M8330	Timing Generator Module	1
G104	Sense Inhibit Module	1
G227	X/Y Drive Module	1
1205941	Slide Switch	2
1205375	Slide Switch, Momentary	2
125849-13	Switch Handle, Terra Cotta	2
125849-12	Switch Handle, Amber	2
1209219	Indicator Bulb	6
7006994	Key Switch Assembly	1
5409264	Power Supply Control Module A1	1
5409262	Power Supply Control Module A2	1

Table 5-2
Not Recommended as Spare Parts for PDP-8/E

Part No.	Description
M8320	Timing Loads
H220	Memory Stack
M8650	Teletype Control
54-9057	Programmer's Console (includes printed circuit board, switches, indicators, etc.)
H724	Power Supply
BE8-E	OMNIBUS Expander

5.2.2 PDP-8/E Second-Level Spares

Second-level spares for the PDP-8/E basic computer, which are included in spare parts option kit SP8-EB, are listed in Table 5-3.

Table 5-3
PDP-8/E Recommended Second-Level Spares

DEC Part No.	Description			Quantity
12-05317	Switch			2
12-09219	Lamp			6
12-05375	Switch			1
12-05941	Switch			2
12-10043	Switch Rotary			1
12-05849-12	Switch Handle			2
12-05849-13	Handle			2
13-02871	Resistor	1.21K	1/8W	2
13-04833	Resistor	1.96K	1/8W	2
13-04868	Resistor	2.74K	1/8W	2
13-05128	Resistor	5.62K	1/8W	2
13-05252	Resistor	68.1K	1/8W	2
13-10032	Resistor	16.9Ω	6W 1%	2
13-02941	Resistor	14.7K	1/8W	2
13-03156	Resistor	34.8K	1/8W	2
13-01420	Resistor	27Ω	1/4W	2
13-00317	Resistor	470Ω	1/4W	2
13-00439	Resistor	3.3K	1/4W	2
13-00229	Resistor	100Ω	1/4W	2
15-09649	Transistor	2N3762		3
15-100150	Transistor	DEC 4008		4
15-05321	Transistor	DEC 2007		3
15-09632	Transistor	DEC 2007		4
15-09854	Transistor	8251		2
10-03053	Capacitor	0.47 MFD		2

Table 5-3 (Cont)
PDP-8/E Recommended Second-Level Spares

DEC Part No.	Description	Quantity
10-00004	Capacitor 0.02 MFD	2
10-00016	Capacitor 100 pF	2
10-09678	Capacitor 0.047 MFD	2
10-05306	Capacitor 6.8 MFD	2
19-09004	IC DEC 7402	2
19-09686	IC DEC 7404	2
19-09930	IC DEC 7405	1
19-09955	IC DEC 7412	1
19-09928	IC DEC 7416	2
19-09929	IC DEC 7417	1
19-09056	IC DEC 74H00	1
19-09931	IC DEC 74H04	1
19-09057	IC DEC 74H10	1
19-09267	IC DEC 74H11	1
19-05586	IC DEC 74H40	2
19-05547	IC DEC 7474	3
19-09667	IC DEC 74H74	1
19-09594	IC DEC 8251	2
19-09932	IC DEC 7483	1
19-09927	IC DEC 74H87	1
19-010011	IC DEC 7486	1
19-09055	IC DEC 7495	2
19-09971	IC DEC 6380A	3
19-09972	IC DEC 6314A	1
19-09973	IC DEC 97401	5
19-09936	IC DEC 74151	2
19-09937	IC DEC 74153	1
19-09935	IC DEC 8235	1
19-09934	IC DEC 8266	2
19-09373	DEC ML-9601	1
19-09867	DEC ML-4007	1
19-05521	DEC ML-1540	2
16-09996	Transformer 6501	1
16-09651	Transformer 8010	2
16-09478	Transformer 17Z5	2
18-09880-01	Crystal 14.418 MHz	1
18-09880	Crystal 19.661 MHz	1
12-10089	Berg Socket	2
12-10090	Berg Housing	2
13-02955	Resistor 750Ω 1/8W	2
13-02956	Resistor 196Ω 1/8W	2
13-04855	Resistor 9.09K 1/8W	2

Table 5-3 (Cont)
PDP-8/E Recommended Second-Level Spares

DEC Part No.	Description	Quantity
91-07722		2
12-10073	Terminal	2
12-10072	Connector Socket	2
FSA 2501	Diode Pack	4
13-10071	Thermistor	2
BC08J	BC08J	1
12-09340	AMP Pin Housing (Mate-N-Lok)	1
12-09379-01	Pin Connector Terminal	1
12-09340-01	AMP Socket Housing	1
12-09378-01	Socket Connector Terminal	1
12-9350-6	AMP Socket Housing	1
12-9351-6	AMP Pin Housing	1
12-9378-1	Pin Connector Terminal	1
12-9379-1	Socket Connector Terminal	1

5.2.3 H724 Power Supply Recommended Spare Components

Recommended spares for the H724 Power Supply are listed in Table 5-4.

Table 5-4
H724 Power Supply Recommended Spare Parts

DEC Part No.	Description	Quantity
11-10181-0	CR500 Thyractor 6RS05P5B5	1
11-05314	CR400 IN645	1
11-09979	CR200 IN1185A	1
11-10006	CR300 IN1201A	1
11-09977	VR7 IN749A	1
11-00114	CR1,2,3 IN914 or 644	4
12-09403	Fan (Super)	1
13-10170	Thermistor	1
13-09143-8	R29 Pot. 2K, 3/4W, 10%	1
13-09143-6	R5, 21 Pot. 500, 3/4W, 10%	1
15-09338	Q2-7, 13, 14 MPS6531 or 2N1613	1
15-10151	Q1, 10 RCA 40372	2
15-03409	Q8, 9, 12, 15 MPS6534 or 2N3133	2
15-5819	Q100, 200, -206, 300 2N3055 (to-41 Case)	2
12-10198-0	Relay K1	1

Table 5-4 (Cont)
H724 Power Supply Recommended Spare Parts

DEC Part No.	Description			Quantity
11-10182-0	CR100 IN4721			2
11-10183-0	Q207 SCR			1
54-09262	A1 Control Module			1
54-09264	A2 Control Module			1
12-10199-0	Thermal Relay			1
19-09981	VR1, 5 VA 723C			1
90-07208	0.5A	250V	AGC 1/2	2
90-083890-0	0.125	250V	AGC 1/8	2
90-08390-0	10A	250V	ABC 10	2
90-08388-0	1.5A	250V	AGC 1-1/2	2
90-08387-0	2.5A	250V	AGC 2-1/2	2
90-08386-0	25A	125V	ABC 25	2

5.3 PDP-8/F AND PDP-8/M SPARES

5.3.1 PDP-8/F First-Level Spares

First-level spares for the PDP-8/F basic computer, which are included in spare parts option kit SP8-FA, are listed in Table 5-5.

Table 5-5
PDP-8/F Recommended First-Level Spares

DEC Part No.	Description	Quantity
M8300	Major Registers Module	1
M8310	Registers Control Module	1
M8330	Timing Module	1
G104	Sense/Inhibit Module	1
G227	X/Y Drive Module	1
11-10625	Light Emitting Diode	2
12-10626	Slide Switch	2
12-05375	Slide Switch, Momentary	2
12-5849-12	Handle, Amber	2
12-5849-13	Handle, Terra Cotta	2
54-09728	Regulator Board Assembly	1

5.3.2 PDP-8/M First-Level Spares

First-level spares for the PDP-8/M basic computer, which are included in spare parts option kit SP8-MA, are listed in Table 5-6.

Table 5-6
PDP-8/M Recommended First-Level Spares

DEC Part No.	Description	Quantity
M8300	Major Registers Module	1
M8310	Registers Control Module	1
M8330	Timing Module	1
G104	Sense/Inhibit Module	1
G227	X/Y Drive Module	1
11-10625	Light Emitting Diode	2
12-10626	Slide Switch	2
12-05375	Slide Switch, Momentary	2
12-05849-06	Handle, Russett Orange	2
12-05849-13	Handle, Terra Cotta	2
54-09728	Regulator Board Assembly	1

5.3.3 PDP-8/F and PDP-8/M Second-Level Spares

Second-level spares for the PDP-8/F and PDP-8/M basic computers, which are included in spare parts option kits SP8-FB and SP8-MB, respectively, are listed in Table 5-7.

Table 5-7
PDP-8/F and PDP-8/M Recommended Second-Level Spares

DEC Part No.	Description	Quantity
10-00004	Capacitor, 0.02 MFD	2
10-00016	Capacitor, 100 pF	2
10-03053	Capacitor, 0.47 MFD	2
10-05306	Capacitor, 06.8 MFD	2
10-09678	Capacitor, 0.047 MFD	2
11-10324	Solid State Lamp	1
11-10714	12A Diode Bridge NSS3514	1
12-09355	Switch, Micro	1
12-05033	Fan, Boxer	1
12-10043	Switch, Miniature Rotary	1
12-10073	Connector, 40 Terminal	2
12-10627	Rotary Switch	1
12-10790	Switch, DPSTN.O.	1
12-10824	Thermostat	1
12-10830-5	Circuit breaker, 5 AMP	1
12-10830-7	Circuit Breaker, 7 AMP	1
13-00229	Resistor 100Ω 1/4W	2
13-00317	Resistor 470Ω 1/4W	2
13-00439	Resistor 3.3K 1/4W	2
13-01420	Resistor 27Ω 1/4W	2

Table 5-7 (Cont)

PDP-8/F and PDP-8/M Recommended Second-Level Spares

DEC Part No.	Description	Quantity
13-02871	Resistor 1.21K 1/8W	2
13-02941	Resistor 14.7K 1/8W	2
13-02955	Resistor 750Ω 1/8W	2
13-02956	Resistor 196Ω 1/8W	2
13-03156	Resistor 34.8K 1/8W	2
13-04833	Resistor 1.96K 1/8W	2
13-04855	Resistor 9.09K 1/8W	2
13-04868	Resistor 2.74K 1/8W	2
13-05128	Resistor 5.62K 1/8W	2
13-05252	Resistor 68.1K 1/8W	2
13-05872	Resistor	2
13-10032	Resistor 16.9Ω 6W	2
13-10071	Resistor	2
13-10709	Resistor	2
15-03409-01	MPS6534B or 2N3133	2
15-05321	2N4258	3
15-09338	MPS6531 or 2N1613	1
15-09632	DEC 2007	4
15-09649	2N3762	3
19-09594	DEC 8251	2
15-10015	DEC 4008	4
15-10151	RCA 40372 (2N3054)	2
15-10196	2N5302	2
15-10706	GPS–A55 or MPS–A55	2
15-10765	TRIACMAC 11-3	2
16-09478	Transformer 1725	2
16-09651	Transformer 8010	2
16-09996	Transformer 6501	1
18-09880	Crystal, 19.661 MHz	1
18-09880-01	Crystal 14.418 MHz	1
19-05521	IC DEC 1540	2
19-05547	IC DEC 7474	3
19-05586	IC DEC 74H40	2
19-09004	IC DEC 7402	2
19-09055	IC DEC 7495	2
19-09056	IC DEC 74H00	1
19-09057	IC DEC 74H10	1
19-09267	IC DEC 74H11	1
19-09373	IC DEC ML-9601	1
19-09594	IC DEC 82513-930	2
19-09667	IC DEC 74H74	1
19-09686	IC DEC 7404	2
19-09705	IC DEC 8881	1
19-09867	IC DEC 4007	1
19-09927	IC DEC 74H87	1
19-09928	IC DEC 7416	2
19-09929	IC DEC 7417	1

Table 5-7 (Cont)
PDP-8/F and PDP-8/M Recommended Second-Level Spares

DEC Part No.	Description	Quantity
19-09930	IC DEC 7405	1
19-09931	IC DEC 74H04	1
19-09932	IC DEC 7483	1
19-09934	IC DEC 8266	2
19-09935	IC DEC 8235	1
19-09936	IC DEC 74151	2
19-09937	IC DEC 74153	1
19-09955	IC DEC 7412	1
19-09971	IC DEC 6380A	3
19-09972	IC DEC 6314A	1
19-09973	IC DEC 97401	5
19-10010	IC DEC FSA2501	4
19-10011	IC DEC 7486	1
90-7221	Fuse	5
90-07226	Fuse	5
90-08389	Fuse	5

5.3.4 H740 Power Supply Recommended Spares

Recommended spares for the H740 power supply are listed in Table 5-8.

Table 5-8
H740 Power Supply Recommended Spare Parts

DEC Part No.	Description	Quantity
1510712	Transistor, MJ900	1
1510706	Transistor, GPS855	2
1510705	Transistor, GPS A05	2
1510928	Transistor, C32A X 135	1
1510708-2	Transistor, D45 H8/B	1
1510196	Transistor, 2N5302	1
1501311	Transistor, 2N1309	1
1500583	Transistor, 2N1308	1
1510765	Transistor, MAC 11-3	1
1110766	Zener Diode, IN5248B	1
1110715	Diode, 20A Fast Recovery Rectifier	1
1110714	Diode, Bridge Rectifier	1
1110925	Zener Diode, 5.1V	1
1110420	Diode, A15B	1
1105796	Diode, IN4004	1
1102421	Zener Diode, IN753A	1
1101938	Zener Diode, AZ5, 2.4V	1
1100122	Zener Diode, IN748A	1

Table 5-8 (Cont)
H740 Power Supply Recommended Spare Parts

DEC Part No.	Description	Quantity
1102802	Zener Diode, IN752A	1
1309150-05	Resistor, Variable, 100Ω, 1/2W, 20%	1
1310927	Thermistor, 100Ω, 3%	1
1610717	Choke, 100 μH, 20A, MMC 4289	1
1610849	Choke, 200 μH, 7A, MMC 4340	1
1210824	Thermostat, SPST	1
1205747	Fuse, 5A Pico	1
1210929	Fuse, 15A Pico	1

5.4 33 ASR TELETYPE SPARES

The recommended Teletype spare parts are listed in Table 5-9.

Table 5-9
Spare Parts for Keyboard-Model 33 ASR Teletype

DEC Part No.	Description	Quantity
181821	Circuit Board	1
183071	Tape Feed Sprocket	2
182240	Lever, Universal	2
90-07208	Fuse, 1/2A	1
90-07207	Fuse, 3/8A	1
90-08387-0	Fuse, 2.5A	1
120167	Fuse, 3.2A	1
180979	Distributor Brush	2
181420	Belt Driven Gear	1
181411	Drive Gear	1
181409	Belt	2
181007	Shaft	1
181002	Bearing	2

Users who do not have maintenance personnel trained in the maintenance and repair of Teletype units should keep a complete Model 33 Automatic Send Receive Teletype near the computer. If the on-line unit becomes defective, substitute the spare to avoid computer down time. Many users have facilities for the maintenance of Teletype units, in which case it is suggested that spare parts be stocked as listed in Table 5-9 and that one of each Teletype maintenance tool listed in Table 4-10 be stocked. All of these items can be obtained from Digital Equipment Corporation or from Teletype Corporation.

APPENDIX A
IC DESCRIPTIONS

A.1 DEC 7474 and 74H74 ICs

The 7474 and 74H74 ICs are dual D-type, edge-triggered flip-flops. The 74H74 has a smaller propagation delay and a higher maximum clock frequency, but can be represented by the same illustrations as the 7474. These are shown in Figure A-1.

The dc-set and dc-reset inputs are independent of the clock. A low input on either one of these lines holds the flip-flop in the specified state for as long as the low level is maintained. Data on the D-input line is transferred to the outputs on the positive-going edge of the clock pulse. If the clock is at either a high or a low level, the D-input signal has no effect.

The functional logic symbol shows the flip-flop as it normally appears in the manual. Thus, a high level at the D-input causes the flip-flop to be set (the 1 side goes high) by the positive-going edge of the clock pulse. However, many control signals in the PDP-8/E are asserted at ground, rather than at a high level; consequently, if the D input is asserted (is active) at ground, the flip-flop is reset by the clock pulse, and an active signal causes the flip-flop to go to its inactive state. To rectify this inconsistency, DEC redefines flip-flops with D inputs that are asserted at ground. The redefined 7474 flip-flop appears as shown in Figure A-2. If the D input is active (at ground), the clock pulse sets the flip-flop. Note that redefinition involves only the defining of pin numbers in a different manner. Pin 5 is redefined as the 0 side of the flip-flop, pin 6 is redefined as the 1 side, pin 4 becomes dc-reset, and pin 1 becomes dc-set.

A.2 DEC 74H87 IC

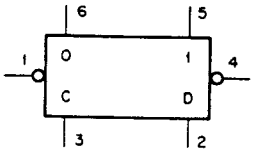
The 74H87 IC is a 4-bit true-false/0-1 element. The logic diagram, the truth table, and the pin locator are shown in Figure A-3.

If control input B is low, control input C determines if an output bit represents the true or the false state of the respective input. However, if B is high, C forces the output to be either high or low, regardless of the respective input. The 74H87 is used in major register gating, where it is designated Data Control Gate.

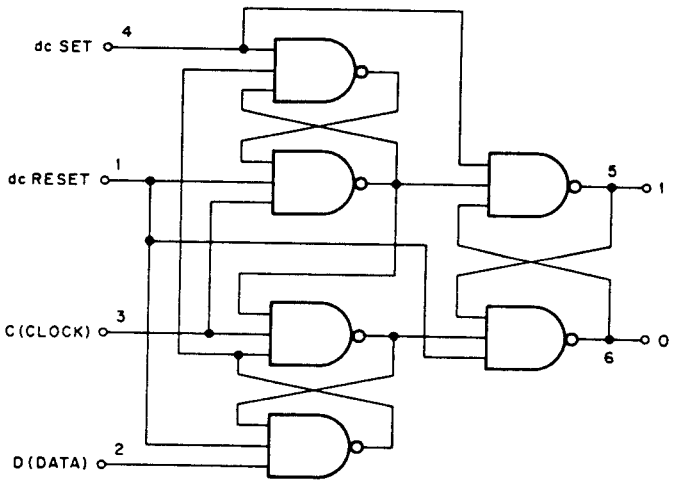
A.3 DEC 7483 IC

The 7483 IC is a 4-bit binary full-adder. The logic diagram and the pin locator are shown in Figure A-4.

The 7483 is used for parallel-add/serial-carry applications. It adds two 4-bit binary numbers (A and B) and provides a sum (S) output for each bit. The resultant carry (CARRY OUT) is taken from the last bit of each adder. This IC is used in the adder network of major register gating.



FUNCTIONAL LOGIC
SYMBOL (EACH F/F)

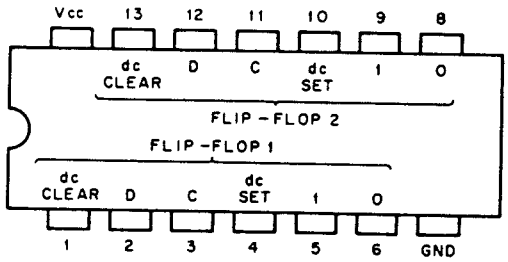


LOGIC DIAGRAM (EACH F/F)

t_n	t_{n+1}	
D - INPUT	1-OUTPUT	0-OUTPUT
LOW	LOW	HIGH
HIGH	HIGH	LOW

t_n = BIT TIME BEFORE CLOCK PULSE
t_{n+1} = BIT TIME AFTER CLOCK PULSE

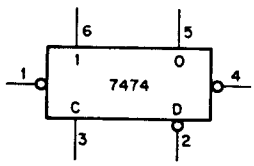
TRUTH TABLE (EACH F/F)



PIN LOCATOR
(TOP VIEW OF IC)

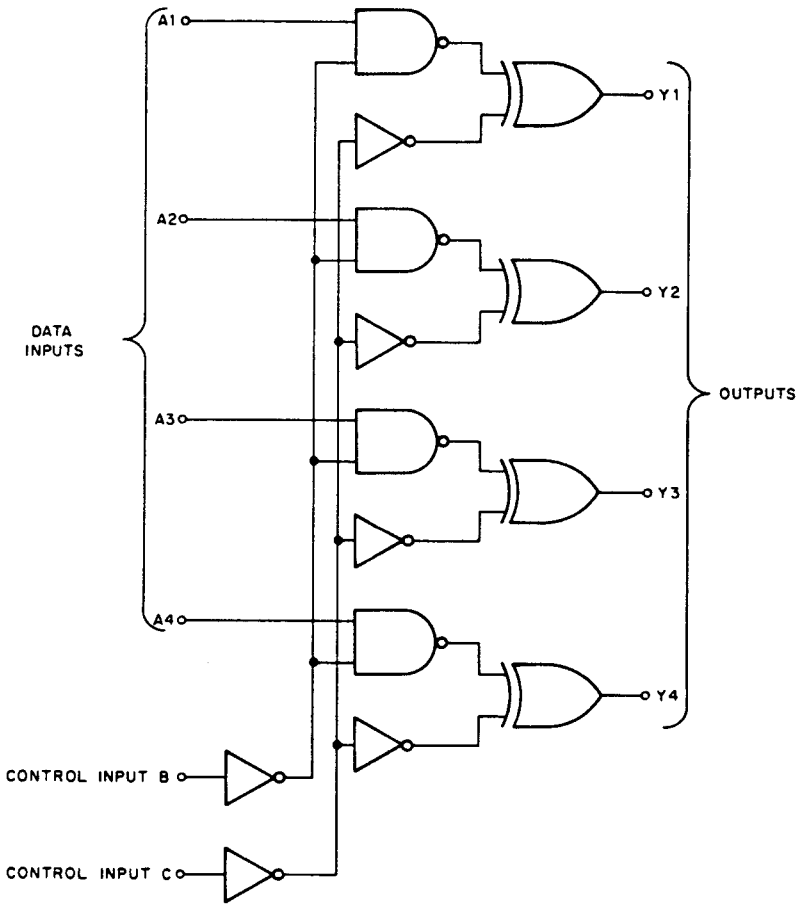
8E-0135

Figure A-1 DEC 7474 and 74H74 IC Illustrations



8E-0132

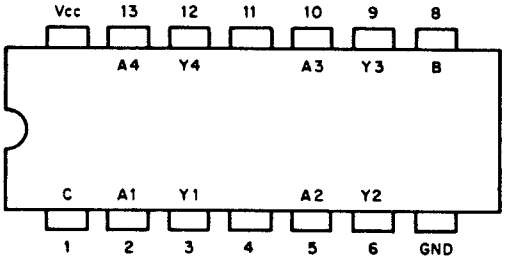
Figure A-2 DEC 7474 IC; Redefined Functional Logic Symbol



LOGIC DIAGRAM

CONTROL INPUTS		OUTPUTS			
B	C	Y1	Y2	Y3	Y4
LOW	LOW	$\overline{A1}$	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$
LOW	HIGH	A1	A2	A3	A4
HIGH	LOW	HIGH	HIGH	HIGH	HIGH
HIGH	HIGH	LOW	LOW	LOW	LOW

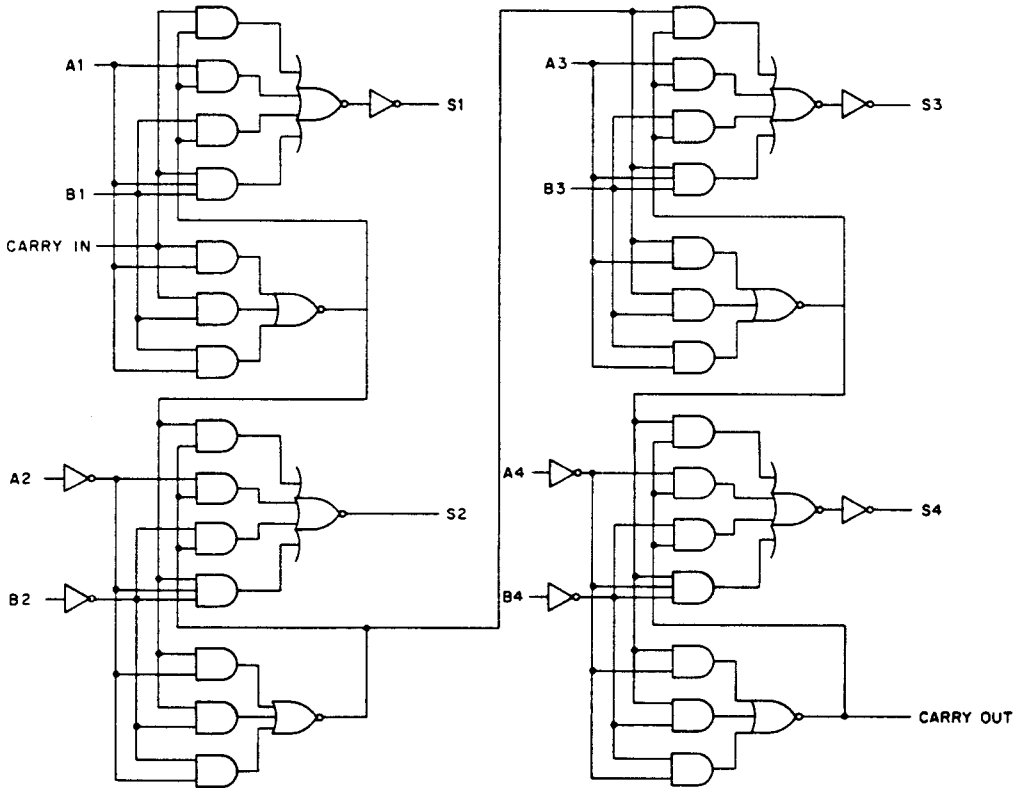
TRUTH TABLE



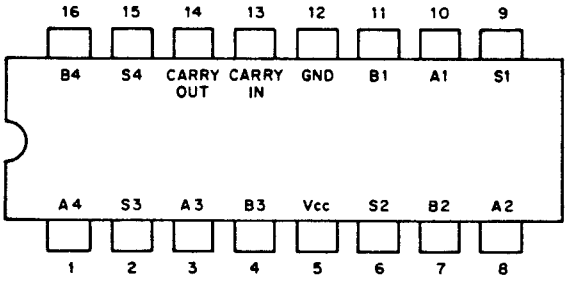
PIN LOCATOR
(TOP VIEW OF IC)

8E-0131

Figure A-3 DEC 74H87 IC Illustrations



LOGIC DIAGRAM



PIN LOCATOR
(TOP VIEW OF IC)

8E-0130

Figure A-4 DEC 7483 IC Illustrations

A.4 DEC 7495 IC

The 7495 IC is a 4-bit shift register. The logic diagram and the pin locator are shown in Figure A-5.

This IC can be used for both parallel-loading operations and shifting operations, depending on the state of the mode control (M) input. If the M-input is high, data can be placed on the parallel input lines, A1 through D1, and loaded into the R/S master-slave flip-flops by a clock pulse at the Clock 2 input. If the M-input is low, the output of each flip-flop is coupled to the R/S input of the succeeding flip-flop. Data is placed on the Serial Input line, and a clock pulse at the Clock 1 input shifts the data into the first R/S flip-flop. Each succeeding pulse does likewise, at the same time right-shifting the register. The outputs of the flip-flops, A2 through D2, are available during both shifting and parallel-loading operations. The 7495 is used in the Timing Generator, where a number of them are connected in series to form the Timing Shift Register.

A.5 DEC 8235 IC

The 8235 is a 4-bit, dual data input logic element. The logic diagram, the truth table, and the pin locator are shown in Figure A-6.

If both control inputs are low, a bit output can be either high or low, depending on the state of both A_n and B_n. If both control inputs are high, a bit output is high, regardless of the state of A_n and B_n. The two remaining possible combinations of C and D produce the output state shown by the truth table. The 8235 is used as a multiplexer in major register gating, where it is designated Data Line Multiplexer.

The output circuits of the 8235 are open-collector, enabling the 8235 to direct drive many signal lines on the OMNIBUS.

A.6 DEC 8251 IC

The 8251 IC is a BCD-to-Decimal decoder. The logic diagram, the truth table, and the pin locator are shown in Figure A-7.

As an example of the logic operation, consider the BCD representation for three: 0011. This combination of voltage levels (A and B high, C and D low) results in all output gates, with the exception of gate 3, being disqualified. The voltage at the output of gate 3 goes low, indicating a decimal 3 to the succeeding circuit.

In the truth table, 0s and 1s are used because binary numbers are generally recognized in these terms. However, it is important to remember that these 0s and 1s represent only voltage levels. A signal in the PDP-8/E can be logically true when the signal is at ground; this is usually the case. Furthermore, care should be exercised when attempting to relate the 8251 decimal outputs to the PDP-8/E basic instruction octal codes. For example, the octal code for an OPR instruction is 7XXX (we are concerned only with the three most significant bits). The 8251 IC in major register control decodes the OPR instruction and asserts decimal output 0, rather than 7. The concept detailed in this paragraph will help avoid confusion when considering this particular use of the 8251.

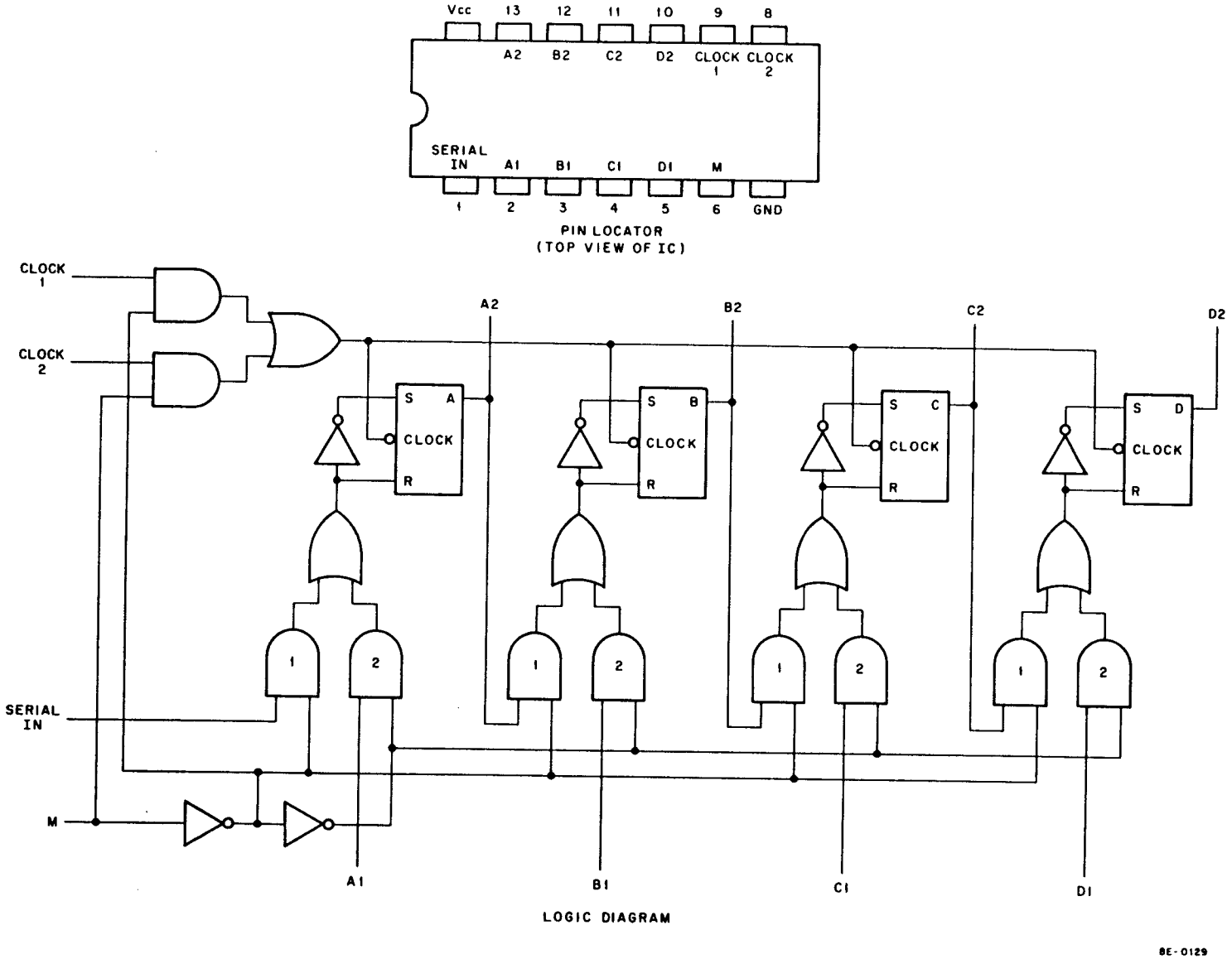
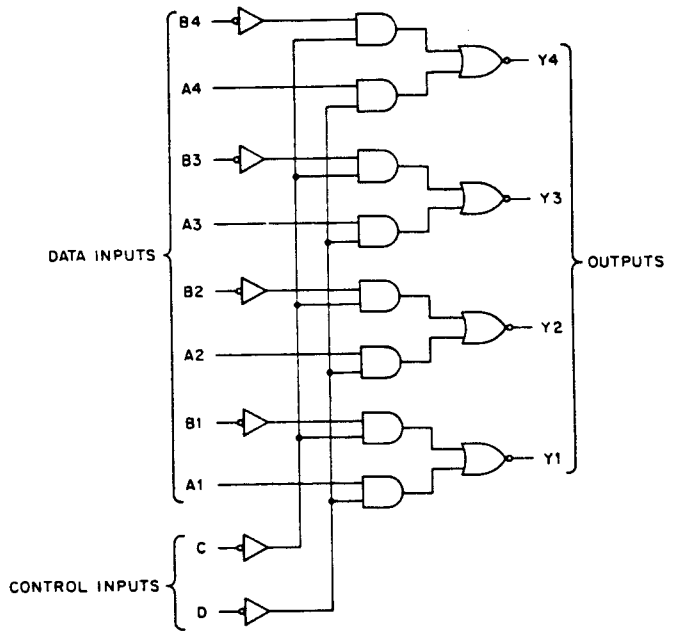


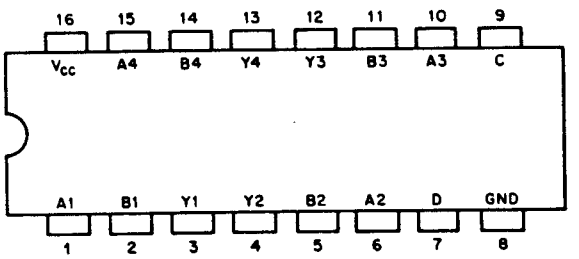
Figure A-5 DEC 7495 IC Illustrations



LOGIC DIAGRAM

CONTROL INPUT		DATA INPUT		OUTPUT
C	D	An	Bn	Yn
LOW	LOW	LOW	LOW	LOW
		LOW	HIGH	HIGH
		HIGH	LOW	LOW
		HIGH	HIGH	LOW
LOW	HIGH	–	–	Bn
HIGH	LOW	–	–	$\overline{An}$
HIGH	HIGH	–	–	HIGH

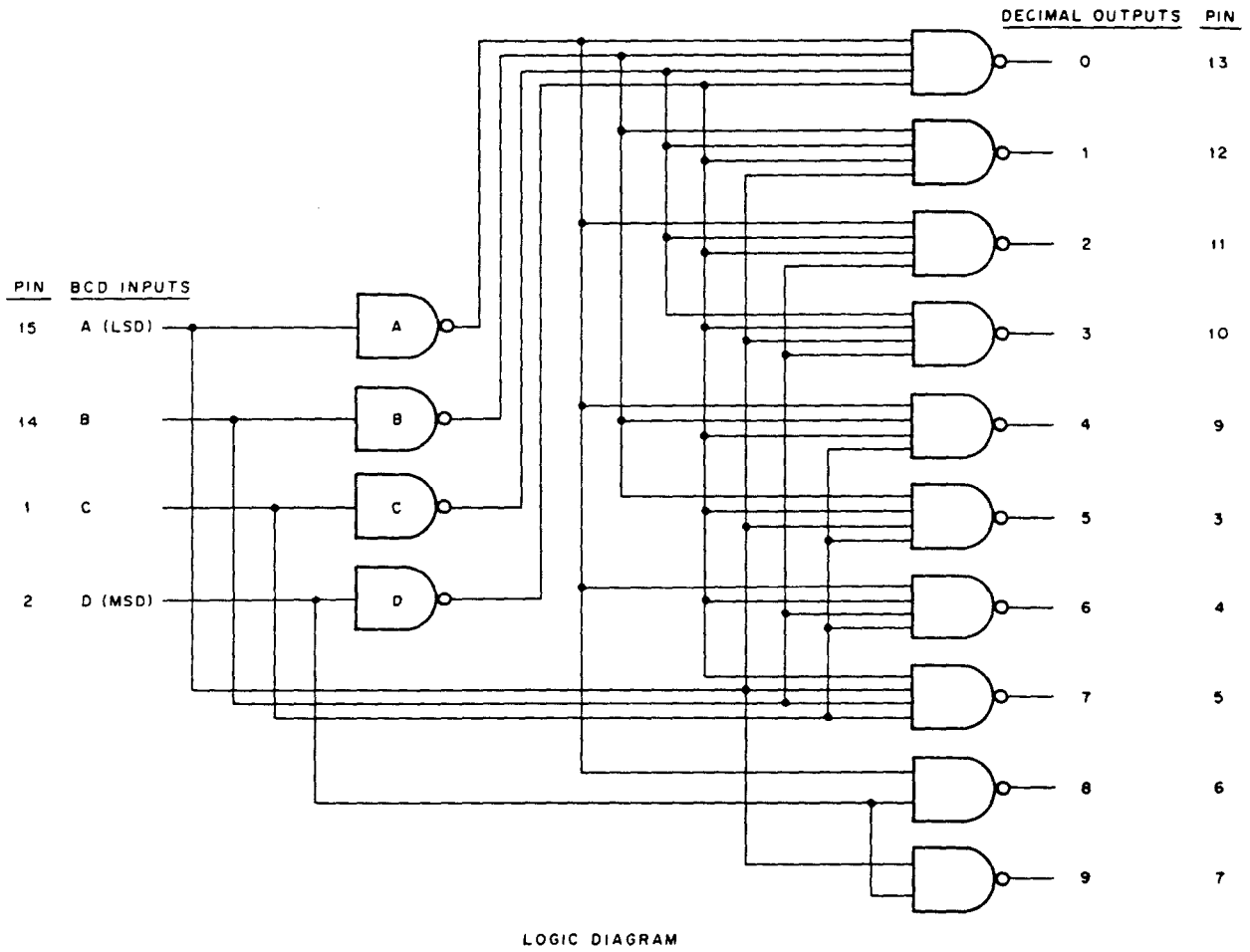
TRUTH TABLE



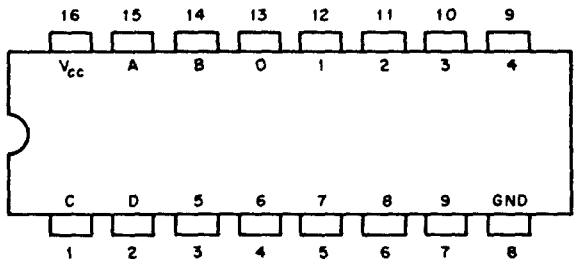
PIN LOCATOR
(TOP VIEW OF IC)

8E-0128

Figure A-6 DEC 8235 IC Illustrations



LOGIC DIAGRAM



PIN LOCATOR
(TOP VIEW OF IC)

8E-0134

Figure A-7 DEC 8251 IC Illustration

Input States					Output States									
D	C	B	A		0	1	2	3	4	5	6	7	8	9
0	0	0	0		0	1	1	1	1	1	1	1	1	1
0	0	0	1		1	0	1	1	1	1	1	1	1	1
0	0	1	0		1	1	0	1	1	1	1	1	1	1
0	0	1	1		1	1	1	0	1	1	1	1	1	1
0	1	0	0		1	1	1	1	0	1	1	1	1	1
0	1	0	1		1	1	1	1	1	0	1	1	1	1
0	1	1	0		1	1	1	1	1	1	0	1	1	1
0	1	1	1		1	1	1	1	1	1	1	0	1	1
1	Repeat above sequence	Repeat above sequence	Repeat above sequence		1	1	1	1	1	1	1	1	0	1
1					1	1	1	1	1	1	1	1	1	0
1					1	1	1	1	1	1	1	1	0	1
1					1	1	1	1	1	1	1	1	1	0
1					1	1	1	1	1	1	1	1	0	1
1					1	1	1	1	1	1	1	1	1	0
1					1	1	1	1	1	1	1	1	0	1
1					1	1	1	1	1	1	1	1	1	0

Note: 0 represents a low voltage level; 1 represents a high voltage level.

A.7 DEC 8266 IC

The 8266 IC is a 4-bit, dual data input logic element. The logic diagram, the truth table, and the pin locator are shown in Figure A-8.

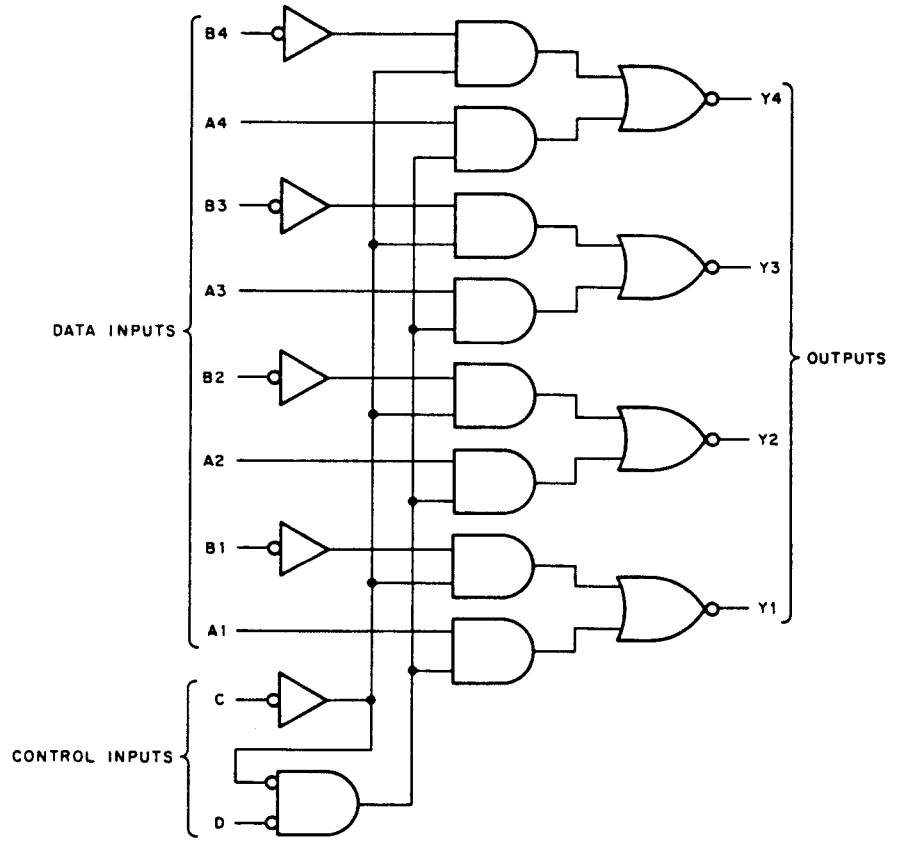
The 8266 is similar to the 8235 IC, already introduced. The major difference between the two is in the Y_n output state, when both control inputs are low. The 8266 provides an output of the same state as the B_n data input. This IC is used as a multiplexer in major register gating, where it is part of the Register Input Multiplexer.

The output circuits of the 8266 are TTC, making them unsuitable for directly driving the OMNIBUS.

A.8 DEC 8271 IC

The 8271 IC is a 4-bit shift register. The logic diagram, a function table, and the pin locator are shown in Figure A-9.

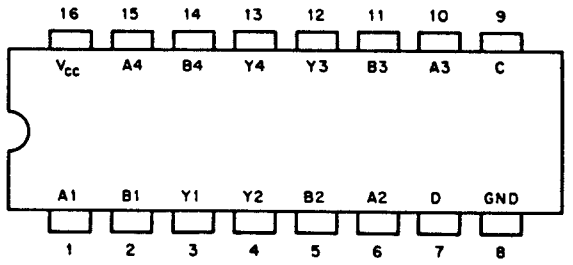
This IC can be used for either serial or parallel data entry. As the function table indicates, the SHIFT signal is high for right-shift operation. The 1 output of each flip-flop is coupled to the R_c/S_c input of the next flip-flop. Data is placed on the D_s line, and a pulse at the CLOCK input shifts the data into the first flip-flop. Each succeeding pulse does likewise, at the same time right-shifting the register. If the SHIFT line is low, the register may be either parallel loaded, or placed in the "hold" condition, depending on the state of the LOAD signal. Data to be parallel-loaded is placed on the D_n inputs and clocked into the respective flip-flop by the negative-going edge of the clock pulse. The outputs of the flip-flops are available during both shifting and parallel loading.



LOGIC DIAGRAM

CONTROL INPUT		OUTPUT
C	D	Yn
LOW	LOW	Bn
LOW	HIGH	Bn
HIGH	LOW	$\overline{An}$
HIGH	HIGH	HIGH

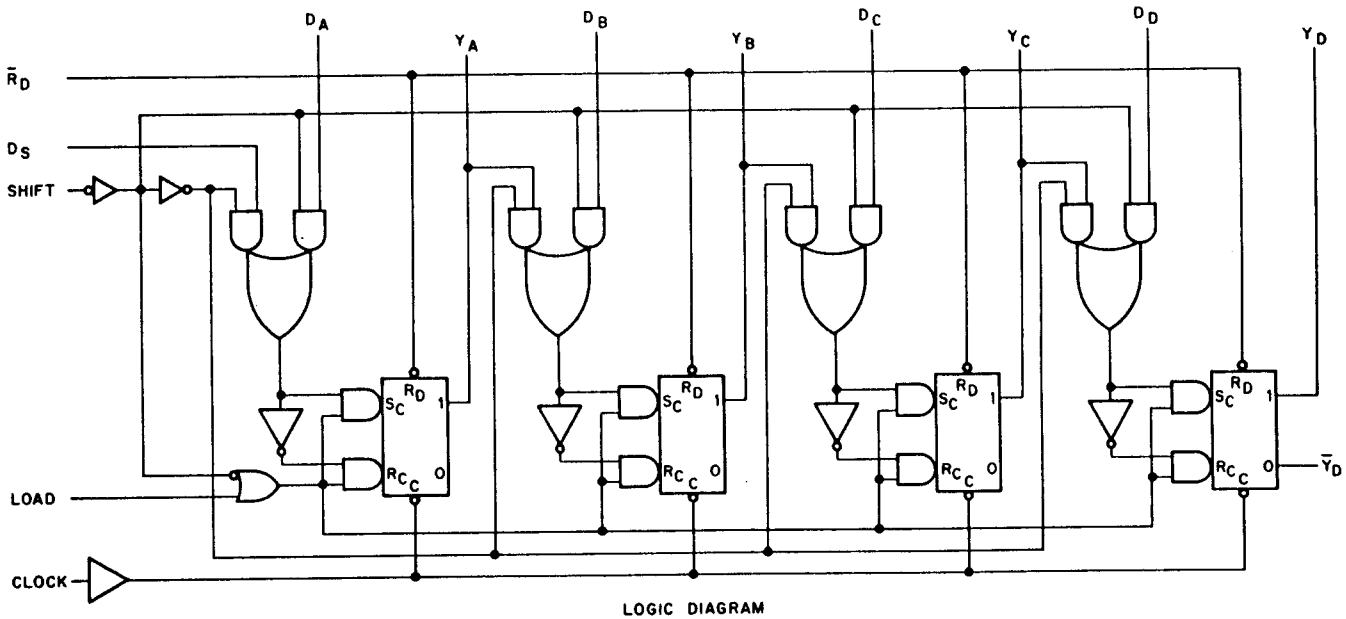
TRUTH TABLE



PIN LOCATOR
(TOP VIEW OF IC)

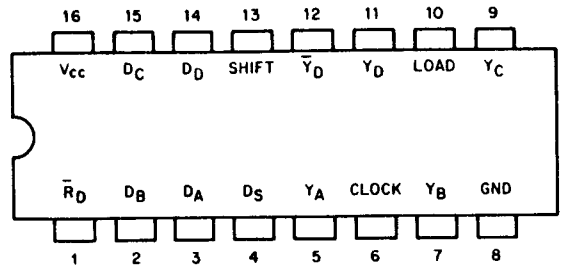
8E-0141

Figure A-8 DEC 8266 IC Illustrations



CONTROL SIGNAL		REGISTER FUNCTION
LOAD	SHIFT	
LOW	LOW	HOLD
HIGH	LOW	PARALLEL LOAD
LOW	HIGH	SHIFT RIGHT
HIGH	HIGH	

FUNCTION TABLE



PIN LOCATOR
(TOP VIEW OF IC)

8E-0140

Figure A-9 DEC 8271 IC Illustrations

The PDP-8/E uses the 8271 as the component flip-flop of the major registers. In this application, only the parallel entry mode is used. Thus, the SHIFT input is grounded, and the LOAD input is connected to a positive voltage.

A.9 DEC 74151 and 74153 ICs

The 74151 and 74153 ICs are data selectors/multiplexers. The 74151 is an 8-bit element, which provides an output signal and its complement. The 74153 is a dual 4-bit element that provides a single output for each section.

The 74151 illustrations are shown in Figure A-10; the 74153 illustrations are presented in Figure A-11. These ICs are used in the PDP-8/E CPU, exclusively.

A.10 DEC 723C IC

The 723C IC is a monolithic voltage regulator, used in the PDP-8/E power supply. The device equivalent circuit and a pin locator are shown in Figure A-12.

The voltage regulator IC consists of a temperature compensated reference amplifier (this supplies a V_{ref} of 7.15V, typical), an error amplifier, a power series pass transistor, and current limit circuitry. Because of the high current requirements of the power supplies, additional pass transistors are used with this voltage regulator. The current limit and current sense capabilities of the IC are not used in the PDP-8/E application; these connections are left open.

A.11 DEC 1540G IC

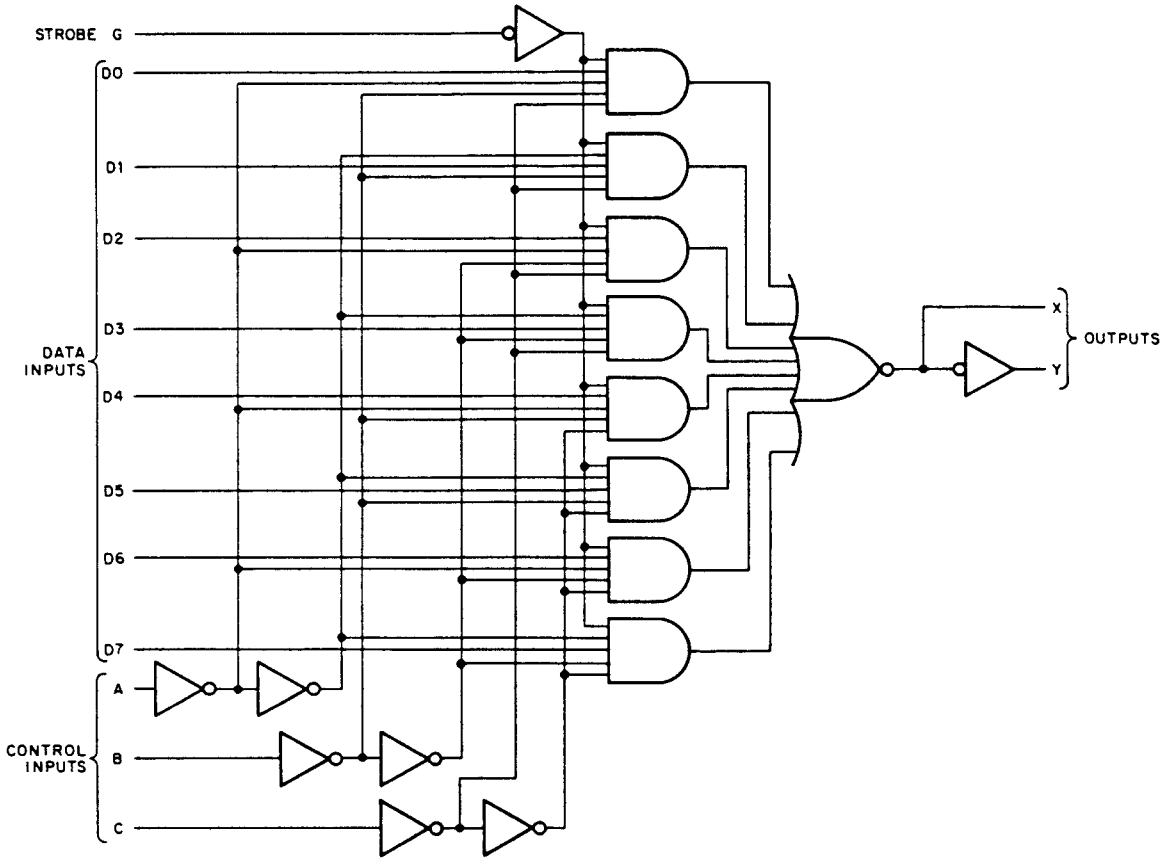
The DEC 1540G IC is a sense amplifier, slicer, and strobe gate used in the PDP-8/E memory, type MM8-E. The device block diagram and a pin locator are shown in Figure A-13.

The input differential amplifier has a typical gain of 85. The resulting output waveform (points A and A^1) is compared with the slice level, and the normally low signal at point B goes positive when the signal at point A or at A^1 is more positive than the internal slice voltage controlled by the voltage on the SLICE LEVEL pin. The slice level is strobed by a pulse applied to the TIME STROBE, and the resulting OUTPUT is used to set a flip-flop external to the IC.

A.12 DEC 7493 IC

The 7493 IC is a binary counter that can be externally wired to operate in either a 4-bit or a 3-bit mode. The logic diagram, the truth table, and the pin locator are shown in Figure A-14.

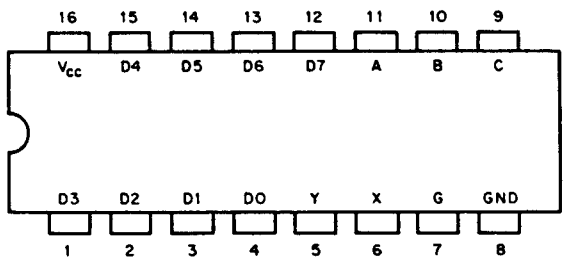
The 7493 counter consists of four J-K master-slave flip-flops. The counter can operate in the 3-bit, ripple-through mode if the operator applies clock pulses at the A2 input. The counter can operate in the 4-bit ripple-through mode if the operator connects Y1 to A2, and applies clock pulses at A1. A gated reset input is provided to inhibit the count inputs and, simultaneously, return each flip-flop to logical 0.



LOGIC DIAGRAM

CONTROL INPUTS			STROBE	OUTPUT
A	B	C	G	X
LOW	LOW	LOW	LOW	$\overline{D0}$
HIGH	LOW	LOW	LOW	$\overline{D1}$
LOW	HIGH	LOW	LOW	$\overline{D2}$
HIGH	HIGH	LOW	LOW	$\overline{D3}$
LOW	LOW	HIGH	LOW	$\overline{D4}$
HIGH	LOW	HIGH	LOW	$\overline{D5}$
LOW	HIGH	HIGH	LOW	$\overline{D6}$
HIGH	HIGH	HIGH	LOW	$\overline{D7}$
DON'T CARE			HIGH	HIGH

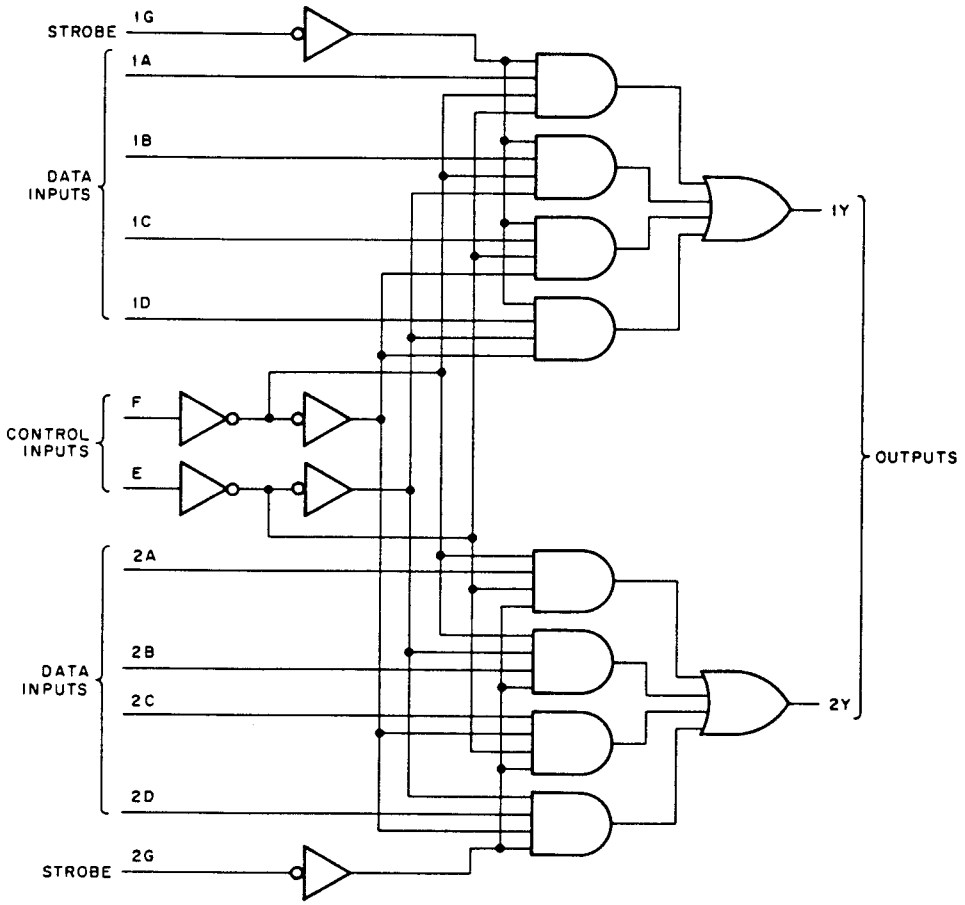
TRUTH TABLE



PIN LOCATOR
(TOP VIEW OF IC)

8E-0139

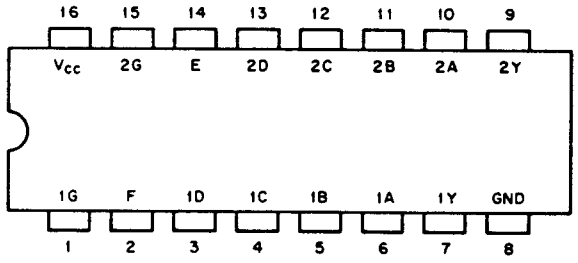
Figure A-10 DEC 74151 IC Illustrations



LOGIC DIAGRAM

CONTROL INPUT		STROBE	OUTPUT
E	F	G	Y
LOW	LOW	LOW	A
HIGH	LOW	LOW	B
LOW	HIGH	LOW	C
HIGH	HIGH	LOW	D
DON'T CARE		HIGH	LOW

TRUTH TABLE (EACH HALF)



PIN LOCATOR
(TOP VIEW OF IC)

8E-0138

Figure A-11 DEC 74153 IC Illustrations

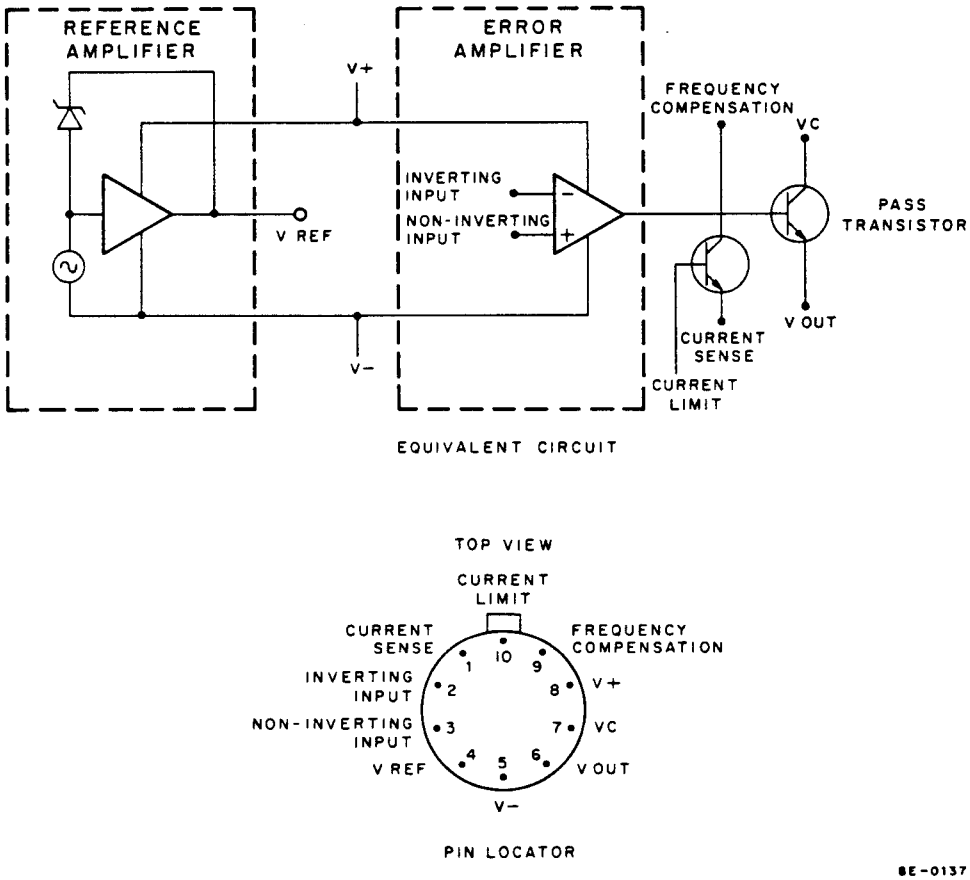


Figure A-12 DEC 723C IC Illustrations

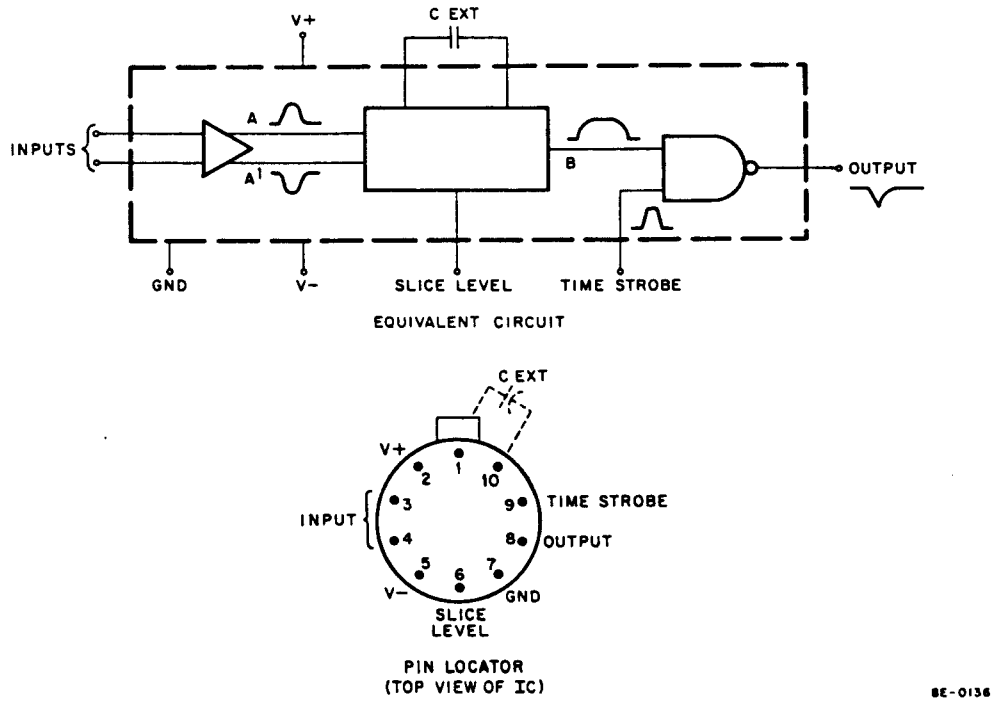


Figure A-13 DEC 1540G IC Illustrations

TOGGLE INPUT PULSE	OUTPUT			
	Y1	Y2	Y3	Y4
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

*TRUTH TABLE

*Applies When 7493 Is Used As 4-Bit Ripple-Through Counter.

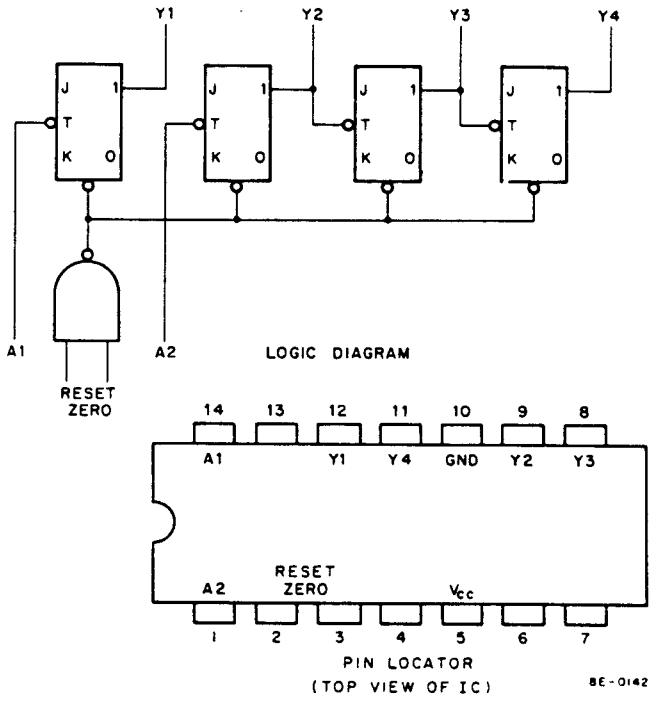


Figure A-14 DEC 7493 IC Illustrations

A.13 DEC 709C IC

The DEC 709C IC is an operational amplifier. The circuit schematic and the pin locator are shown in Figure A-15.

The IC is designed for general-purpose analog amplifier application. In the DK8-EP Programmable Real-Time Clock option, the 709C is used as a comparator and, as such, is the central component in the Schmitt trigger circuits on the M518 module. In this application only half the IC circuitry is used, the output being taken from pin 8 of the IC. As can be seen from the circuit schematic, the output at pin 8 has the same relationship to the summing inputs as does the output at pin 6.

A.14 DEC 7475 IC

The DEC 7475 IC is a 4-bit bistable latch. The logic diagrams, a truth table, and a pin locator are shown in Figure A-16.

Information present at the data input (D) of a latch is transferred to the 1 output when the clock input (C) goes high. If the C input remains high, the 1 output follows the D input. When the C input goes low the 1 output holds the state it was in prior to the transition.

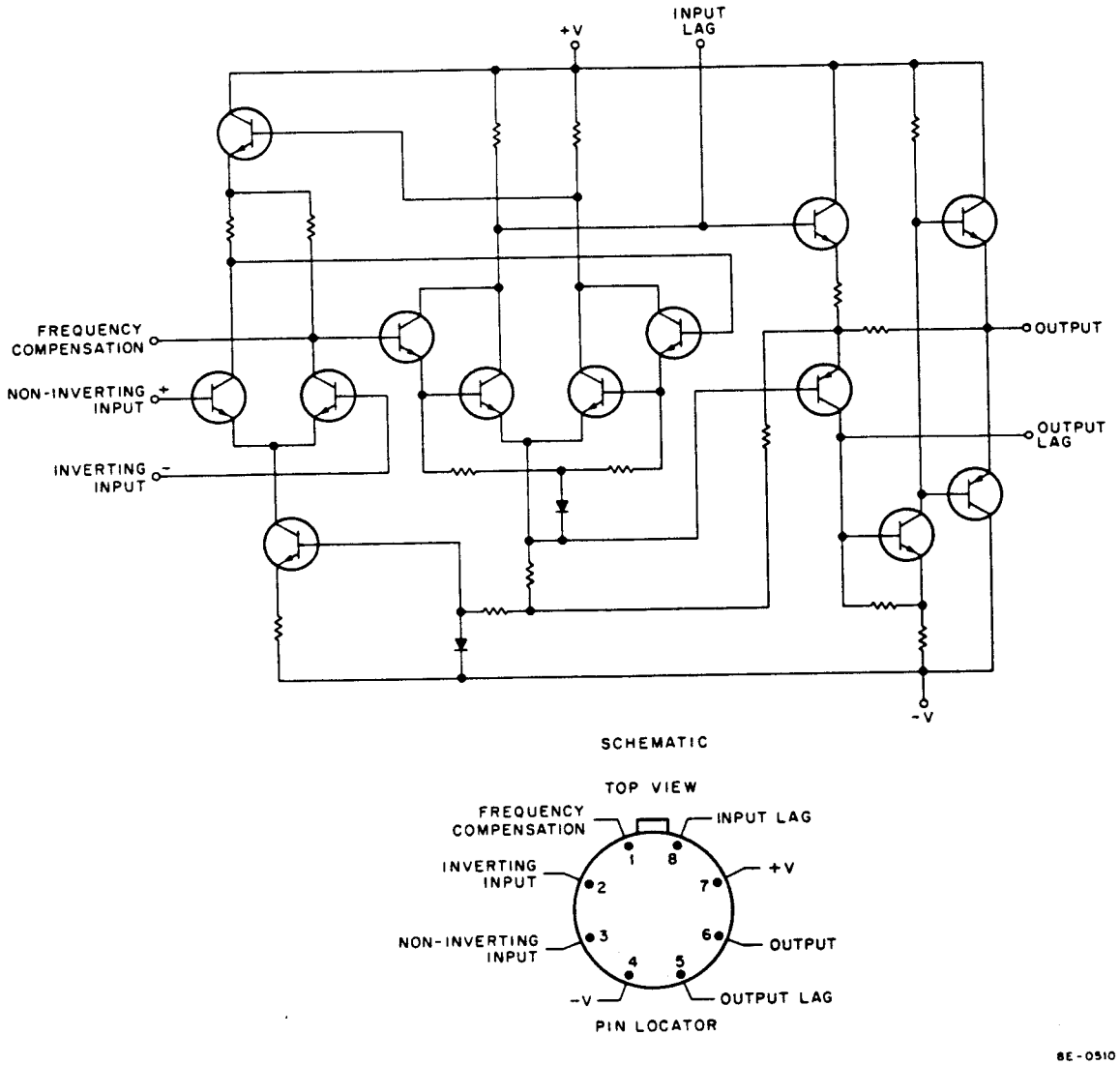


Figure A-15 DEC 709C IC Illustrations

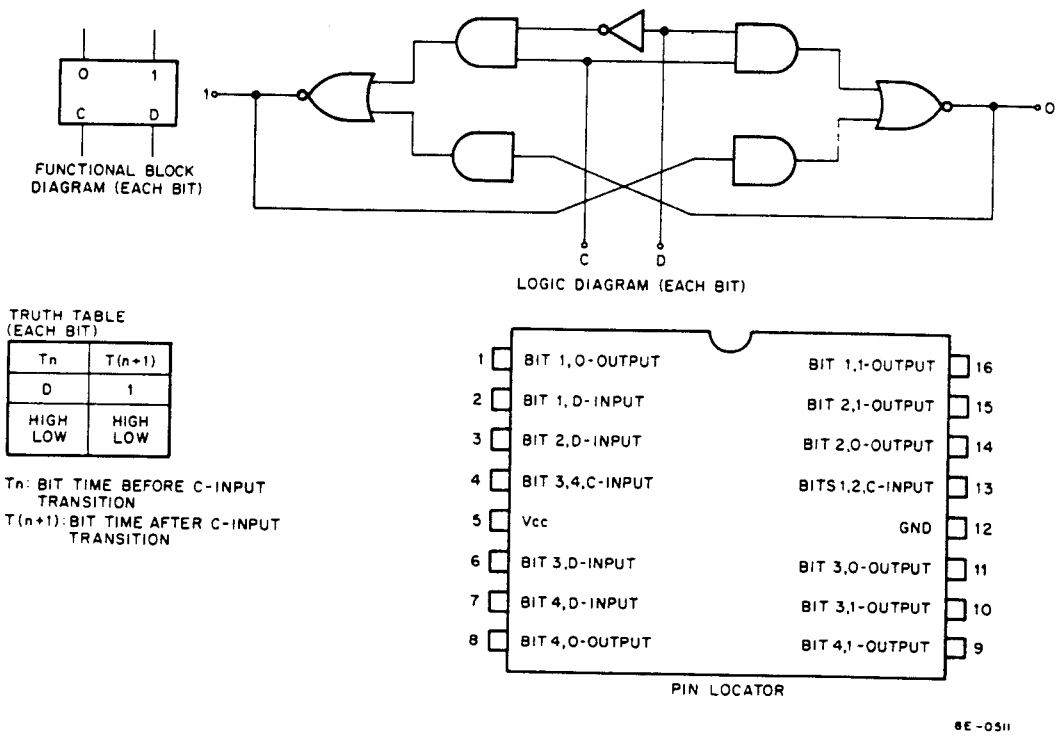


Figure A-16 DEC 7475 IC Illustrations

A.15 DEC 7490 IC

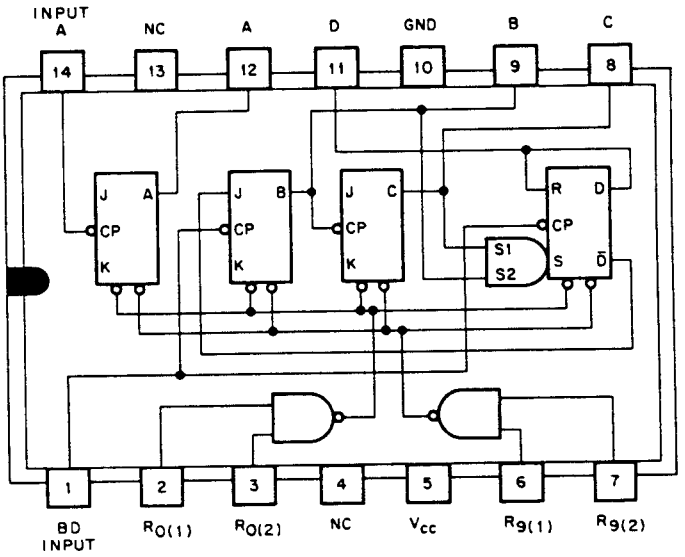
The DEC 7490 IC is a high-speed counter consisting of 4 master-slave flip-flops, connected to provide a divide-by-two counter and a divide-by-five counter. The logic diagram, truth tables, and a pin locator are shown in Figure A-17.

The 7490 can be used in three independent counting modes, namely; a divide-by-two/divide-by-five mode, a divide-by-ten mode, and a BCD count mode. No external interconnections of the IC pins are necessary in the first listed mode. An input at pin 14 is divided by two by flip-flop A and the result is taken from pin 12; an input at pin 1 is divided by five by flip-flops B, C, and D, and the result is taken from pin 11. The output of each flip-flop is made available and all four flip-flops are reset simultaneously, if the gated reset lines are used.

If the divide-by-ten mode is desired, pin 11 must be connected to pin 14. The input at pin 1 is divided by ten and the output is taken from pin 12 (this mode of operation is used in the DK8-EP Programmable Real-Time Clock option). The third listed mode is obtained by connecting pin 1 to pin 12 and applying the input at pin 14; the BCD count sequence is shown in truth table A. The reset inputs are provided to reset a BCD count for 9's complement decimal applications.

A.16 DEC 7470 IC

The DEC 7470 IC is an edge-triggered J-K flip-flop. The logic diagram, pin locator, and truth table are shown in Figure A-18.



LOGIC DIAGRAM/PIN LOCATOR

TRUTH TABLES

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

A– BCD COUNT SEQUENCE

RESET INPUTS				OUTPUT
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	D C B A
1	1	0	X	0 0 0 0
1	1	X	0	0 0 0 0
X	X	1	1	1 0 0 1
X	0	X	0	COUNT
0	X	0	X	COUNT
0	X	X	0	COUNT
X	0	0	X	COUNT

B–RESET/COUNT

NOTES:
1. X in tables indicates either 1 or 0 may be present.
2. NC indicates no internal connections.

BE-0512

Figure A-17 DEC 7490 IC Illustrations

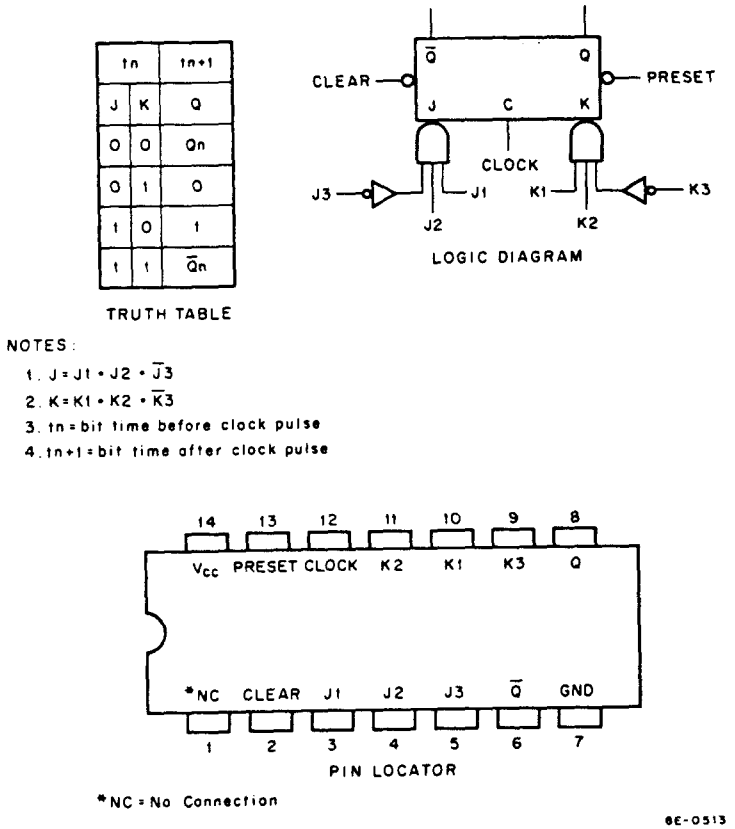


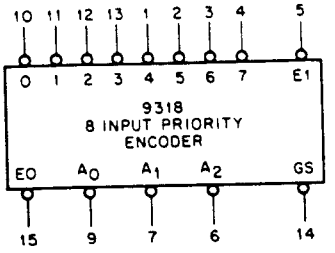
Figure A-18 DEC 7470 Illustrations

The 7470 features gated inputs and direct clear and preset inputs. Input information is transferred to the outputs on the positive edge of the clock pulse. Direct-coupled clock triggering occurs at a specific voltage level of the clock pulse; when the input threshold has been exceeded, the gated inputs are locked out. The preset and clear inputs have effect only when the clock input is low.

A.17 DEC 9318 IC

The DEC 9318 IC is an 8-input priority encoder. The functional logic diagram and a truth table are shown in Figure A-19.

The 9318 accepts data from 8 active low inputs and provides a binary representation on the 3 active low outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line 7 having the highest priority. A high on the input enable (EI) will force all outputs to the inactive state and allow new data to settle without producing erroneous information at the outputs. A group signal output (GS) and an enable output (EO) are provided with the three data outputs. The GS is active level low when any input is low; this indicates when any input is active. The EO is active level low when all inputs are high. Using the output enable along with the input enable allows priority encoding of N input signals. Both EO and GS are inactive high when the input enable is high.



FUNCTIONAL LOGIC DIAGRAM

TRUTH TABLE

E1	0	1	2	3	4	5	6	7	GS	A_0	A_1	A_2	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = High Voltage level
L = Low Voltage level
X = Don't Care

8E-0514

Figure A-19 DEC 9318 IC Illustrations

A.18 DEC 74194 IC

The DEC 74194 IC is a 4-bit bidirectional shift register. The logic diagram, mode-control table, and pin locator are shown in Figure A-20.

In the parallel load mode, data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input. Clocking of the flip-flops is inhibited when both mode-control inputs are low. The mode control should be changed only while the clock input is high.

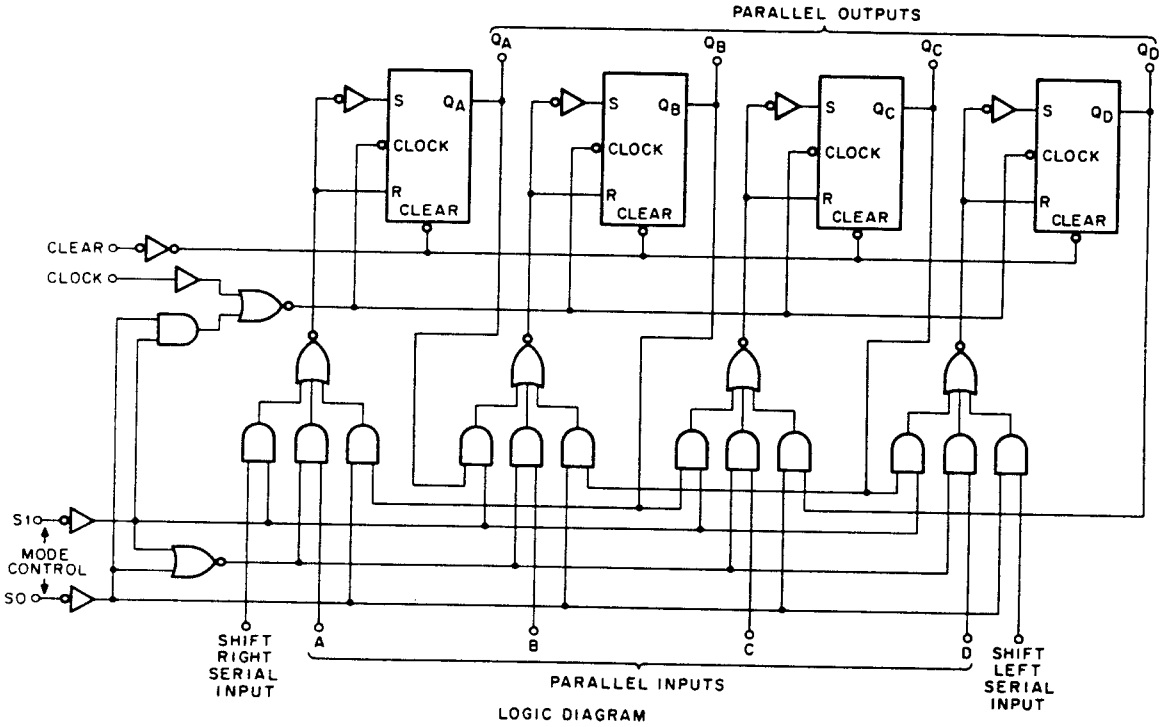
A.19 DEC 74123 IC

The DEC 74123 IC is a retriggerable monostable multivibrator (one-shot). The functional logic diagram/pin locator and a truth table are shown in Figure A-21.

Output pulse width is a function of the external capacitor and resistor. For C_{ext} greater than 1000 pF, the output pulse width (t_w) is:

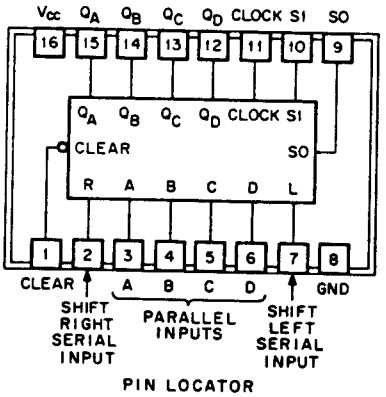
$$t_w = 0.32\ R_T\ C_{ext}\ (1 + \frac{0.7}{R_T}),$$ where R_T is in kΩ, C_{ext} is in pF, and t_w is in ns.

For pulse widths when C_{ext} is less than or equal to 1000 pF, see the plot in Figure A-22.



LOGIC DIAGRAM

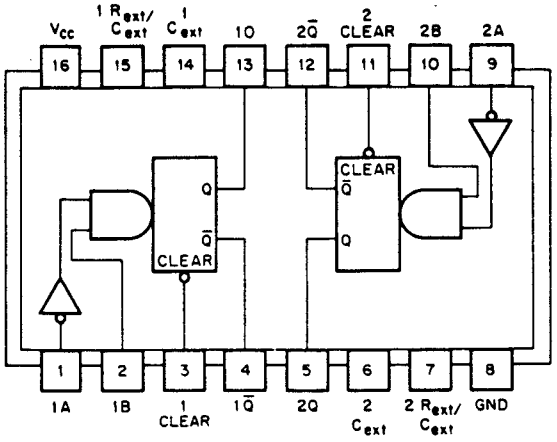
	MODE CONTROL	
	S1	S0
PARALLEL LOAD	H	H
SHIFT RIGHT (IN THE DIRECTION Q_A TOWARD Q_D)	L	H
SHIFT LEFT (IN THE DIRECTION Q_D TOWARD Q_A)	H	L
INHIBIT CLOCK (DO NOTHING)	L	L



PIN LOCATOR

8E-0515

Figure A-20 DEC 74194 IC Illustrations



FUNCTIONAL LOGIC / PIN LOCATOR

TRUTH TABLE

INPUTS		OUTPUTS	
A	B	Q	$\bar{Q}$
H	X	L	H
X	L	L	H
L	↑	⎍	⎍
↓	H	⎍	⎍

NOTE: H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high-level pulse, ⎍ = one low-level pulse, X = irrelevant (any input, including transitions).

8E-0516

Figure A-21 DEC 74123 IC Illustrations

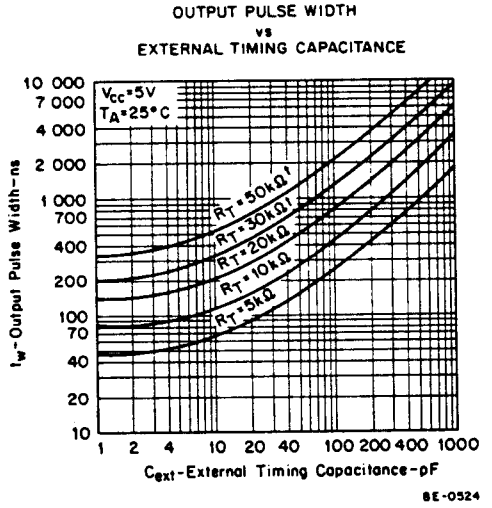


Figure A-22 DEC 74123 IC Output Pulse width vs. External Timing Capacitance

A.20 DEC 74197 IC

The DEC 74197 IC is a pre-settable binary counter that can also be used as a latch. The IC consists of four dc-coupled master-slave flip-flops connected to provide a divide-by-two counter and a divide-by-eight counter. The logic diagram is shown in Figure A-23. A truth table and a pin locator are shown in Figure A-24.

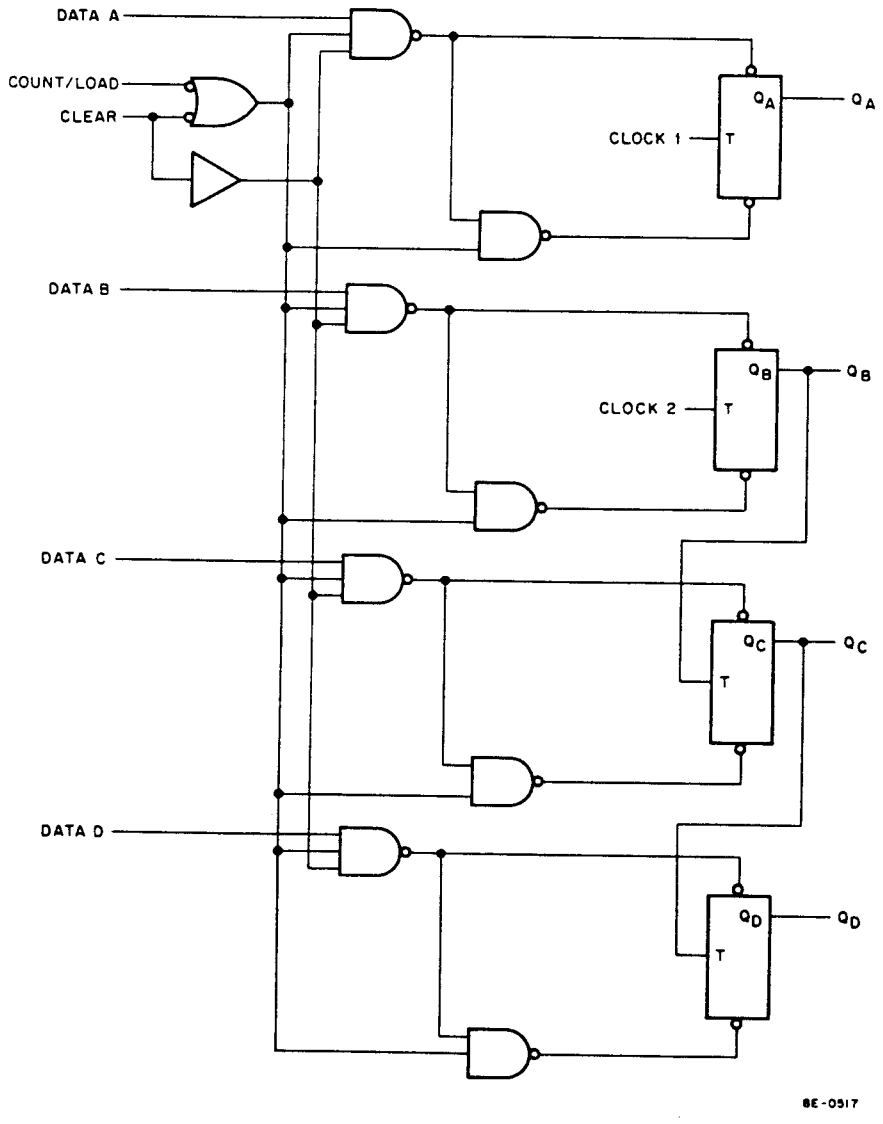


Figure A-23 DEC 74197 Logic Diagram

TRUTH TABLE

COUNT	OUTPUT			
CLOCK 1 INPUT	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Q_A connected to CLOCK 2 input.

PIN LOCATOR

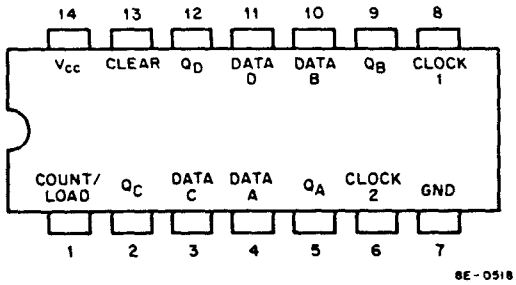


Figure A-24 DEC 74197 Truth Table and Pin Locator

The 74197 can be used in any one of three modes, viz; the divide-by-two/divide-by-eight mode, requiring no external interconnection of IC pins, the latch mode, and the binary counter mode. If the first listed mode is used, an input at pin 8 is divided by 2 by flip-flop A and the result is taken from pin 5; an input at pin 6 is divided by 8 by flip-flops B, C, and D and the result is taken from pin 12. Transfer of information to the outputs takes place on the negative-going (trailing) edge of the clock pulse.

If one wishes to use the latch mode, one must enter data at the four data inputs (pins 4, 10, 3, and 11) and enter a strobe pulse at pin 1. The output pins, 5, 9, 2, and 12, respectively, will follow the inputs when pin 1 is low, but will remain unchanged when pin 1 is high and the clock inputs are inactive.

The third mode, binary counting, is used in the DK8-EP Programmable Real-Time Clock option. Pin 5 must be externally connected to pin 6. The clock input is applied at pin 8. The initial count can be preset to any value by placing a low on pin 1 and entering the data on pins 4, 10, 3, and 11. When pin 13 is taken low, all outputs are set low, regardless of the state of the clock inputs.

APPENDIX B
OMNIBUS SIGNAL LOCATOR

Pin	Signal	Source	Destination
A1A	TP		Not bussed
A1B	TP		Not bussed
A1C	SP GND	P.S.	ALL
A1D	MA0 L	M8360 M8300	KC8-EA, M8330, M8300, G227
A1E	MA1 L	M8360 M8300	KC8-EA, M8330, M8300, G227
A1F	GND	P.S.	ALL
A1H	MA2 L	M8360 M8300	KC8-EA, M8330, M8300, G227
A1J	MA3 L	M8360 M8300	KC8-EA, M8330, M8300, G227
A1K	MD0 L	G104 M8300	KC8-EA, M8330, M8310, M8300, G104, M8350
A1L	MD1 L	G104 M8300	KC8-EA, M8330, M8310, M8300, G104, M8350
A1M	MD2 L	G104 M8300	KC8-EA, M8330, M8310, M8300, G104, M8350
A1N	GND	P.S.	ALL
A1P	MD3 L	G104 M8300	KC8-EA, M8330, M8310, M8300, G104, M8650, M835

Pin	Signal	Source	Destination
A1R	DATA0 L	KC8-EA M8350 M8300 M8360	KC8-EA, M8330, M8300, M8350, M8360
A1S	DATA1 L	KC8-EA M8350 M8300 M8360	KC8-EA, M8300, M8350, M8360
A1T	GND	P.S.	ALL
A1U	DATA2 L	KC8-EA M8350 M8300 M8360	KC8-EA, M8330, M8300, M8350, M8360
A1V	DATA3 L	KC8-EA M8350 M8300 M8360	KC8-EA, M8300, M8350, M8360
A2A	+5	P.S.	ALL
A2B	-15	P.S.	ALL
A2C	GND	P.S.	ALL
A2D	EMA0 L	M8360	KC8-EA, G104
A2E	EMA1 L	M8360	KC8-EA, G104
A2F	GND	P.S.	ALL
A2H	EMA2 L	M8360	KC8-EA, G104
A2J	MEM START L	KC8-EA	M8330
A2K	MD DIR L	M8330 KC8-EA M8360	KC8-EA, M8300, G104
A2L	SOURCE	M8330	G227
A2M	STROBE	M8330	G104
A2N	GND	P.S.	ALL

Pin	Signal	Source	Destination
A2P	INHIBIT	M8330	G104
A2R	RETURN	M8330	G104, G227
A2S	WRITE L	M8330	G104, G227
A2T	GND	P.S.	ALL
A2U	ROM ADDR L	M880	M8310, G104, M880
A2V	LINK L	M8310	M8330
B1A	TP		Not bussed
B1B	TP		Not bussed
B1C	GND	P.S.	ALL
B1D	MA4 L	M8360 M8300	KC8-EA, M8330, M8300, G227
B1E	MA5 L	M8360 M8300	KC8-EA, M8330, M8300, G227
B1F	GND	P.S.	ALL
B1H	MA6 L	M8360 M8300	KC8-EA, M8330, M8300, G227
B1J	MA7 L	M8360 M8300	KC8-EA, M8330, M8300, G227
B1K	MD4 L	G104 M8300	KC8-EA, M8330, M8310, M830, G104, M8650, M8350
B1L	MD5 L	G104 M8300	KC8-EA, M8330, M8310, M830, G104, M8650, M8350
B1M	MD6 L	G104 M8300	KC8-EA, M8330, M8310, M8300, G104, M8650, M8350
B1N	GND	P.S.	ALL
B1P	MD7 L	G104 M8300	KC8-EA, M8330, M8310, M8300, G104, M8650, M8350
B1R	DATA4 L	M8360 KC8-EA M8650 M8300 M8350	KC8-EA, M8300, M8650, M8350

Pin	Signal	Source	Destination
B1S	DATA5 L	M8360 KC8-EA M8650 M8300 M8350	KC8-EA, M8300, M8650, M8350
B1T	GND	P.S.	ALL
B1U	DATA6 L	M8360 KC8-EA M8650 M8300 M8350	KC8-EA, M8300, M8650, M8350
B1V	DATA7 L	M8360 KC8-EA M8650 M8300 M8350	KC8-EA, M8300, M8650, M8350
B2A	+5	P.S.	ALL
B2B	-15	P.S.	ALL
B2C	GND	P.S.	ALL
B2D	INT STROBE	M8330	M8330, M8360
B2E	BRK IN PROG L	M8360	KC8-EA
B2F	GND	P.S.	ALL
B2H	MA, MS LOAD CONT L	M8360	M8310
B2J	OVERFLOW L	M8310	M8360
B2K	BRK DATA CONT L	M8360 KC8-EA	KC8-EA, M8310
B2L	BREAK CYCLE L	M8360	KC8-EA
B2M	LD ADD ENABLE L	KC8-EA	KC8-EA, M8310
B2N	GND	P.S.	ALL
B2P	INT IN PROG H	M8330	M8310, M8330
B2R	RES1		Reserved for DEC use only
B2S	RES2		Reserved for DEC use only

Pin	Signal	Source	Destination
B2T	GND	P.S.	ALL
B2U	RUN L	M8330	KC8-EA, M8330, M8350
B2V	POWER OK	P.S.	M8330, G104
C1A	TP		Not bussed
C1B	TP		Not bussed
C1C	GND	P.S.	ALL
C1D	I/O PAUSE L	M8330	M8330, M8310, M8650, M8350
C1E	C0 L	M8650 M8350 M8330	M8310
C1F	GND	P.S.	ALL
C1H	C1 L	M8650 M8350 M8330	M8310
C1J	C2 L	M8350	M8310
C1K	BUS STROBE	M8330 M8350	M8310, M8330
C1L	INTER. I/O L	M8330	M8650, M8350
C1M	NOT LAST TRANSFER L	M8350	M8330
C1N	GND	P.S.	ALL
C1P	INT RQST L	M8650	M8330, M8350
C1R	INITIALIZE	KC8-EA M8330	KC8-EA, M8330, M8310, M8300, M8650, M8350 M836
C1S	SKIP L	M8650	M8330, M8310
C1T	GND	P.S.	ALL
C1U	CPMA DISABLE L	M836	M8300
C1V	MS,IR DISABLE L	KC8-EA M8360	M8330, M8310

Pin	Signal	Source	Destination
C2A	+5	P.S.	ALL
C2B	-15	P.S.	ALL
C2C	GND	P.S.	ALL
C2D	TP1 L	M8330	M8310, M8330, M8350, M8360
C2E	TP2 L	M8330	M8310, M8330, M8350, M8360
C2F	GND	P.S.	ALL
C2H	TP3	M8330	M8310, M8330, M8650, M835
C2J	TP4	M8330	KC8-EA, M8310, M836
C2K	TS1 L	M8330	KC8-EA, M8330, M8310, M8350, M8360
C2L	TS2 L	M8330	M8310, M8360
C2M	TS3 L	M8330	KC8-EA, M8310, M8350
C2N	GND	P.S.	ALL
C2P	TS4 L	M8330	KC8-EA, M8310, M8360
C2R	LINK DATA L	M8330	M8310
C2S	LINK LOAD L	M8330	M8310
C2T	GND	P.S.	ALL
C2U	IND1 L	KC8-EA	M8330, M8310
C2V	IND2 L	KC8-EA	M8330, M8310
D1A	TP		Not bussed
D1B	TP		Not bussed
D1C	GND	P.S.	ALL
D1D	MA8 L	M8360 M8300	KC8-EA, M8330, M8300, G227
D1E	MA9 L	M8360 M8300	KC8-EA, M8300, G227
D1F	GND	P.S.	ALL

Pin	Signal	Source	Destination
D1H	MA10 L	M8360 M8300	KC8-EA, M8300, G227
D1J	MA11 L	M8360 M8300	KC8-EA, M8300, G227
D1K	MD8 L	G104 M8300	KC8-EA, M8330, M8310, M8300, G104, M8650, M8350
D1L	MD9 L	G104 M8300	KC8-EA, M8330, M8310, M8300, G104, M8650, M8350
D1M	MD10 L	G104 M8300	KC8-EA, M8330, M8310, M8300, G104, M8650, M8350
D1N	GND	P.S.	ALL
D1P	MD11 L	G104 M8300	KC8-EA, M8330, M8310, M8300, G104, M8650, M8350
D1R	DATA8 L	M8360 KC8-EA M8650 M8300 M8350	KC8-EA, M8300, M8650, M8350
D1S	DATA9 L	M8360 KC8-EA M8650 M8300 M8350	KC8-EA, M8300, M8650, M8350
D1T	GND	P.S.	ALL
D1U	DATA10 L	M8360 KC8-EA M8650 M8300 M8350	KC8-EA, M8300, M8650, M8350
D1V	DATA11 L	M8360 KC8-EA M8650 M8300 M8350	KC8-EA, M8300, M8650, M8350

Pin	Signal	Source	Destination
D2A	+15	P.S.	ALL
D2B	-15	P.S.	ALL
D2C	GND	P.S.	ALL
D2D	IR0 L	M8310	KC8-EA, M8330, M8310
D2E	IR1 L	M8310	KC8-EA, M8330, M8310
D2F	GND	P.S.	ALL
D2H	IR2 L	M8310	KC8-EA, M8330, M8310
D2J	F L	M8310	KC8-EA, M8330, M8310
D2K	D L	M8310	KC8-EA, M8330, M8310
D2L	E L	M8310	KC8-EA, M8330, M8310
D2M	USER MODE	USER	KC8-EA, M8330
D2N	GND	P.S.	ALL
D2P	F SET L	M8310	KC8-EA, M8330, M8310
D2R	PULSE LA ADDR H	KC8-EA	M8310
D2S	STOP L	M8330 KC8-EA	M8330
D2T	GND	P.S.	ALL
D2U	KEY CONT L	KC8-EA	M8330, M8310
D2V	SWITCH L	KC8-EA	KC8-EA

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VOLUME 1
DEC-8E-HMM1A-D-D

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