DIGITAL EQUIPMENT CORPORATION

MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION

DATE 18 July 77

TITLE MS8-C 32K PDP-8 MOS MEMORY ENGINEERING SPECIFICATION

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

ENG [illegible] APPD [illegible] SIZE A CODE SP NUMBER MS8-C-2 REV

DEC 16-(392)-1075A-R873
DRA 107A

ENGINEERING SPECIFICATION

digital CONTINUATION SHEET

TITLE MS8-C 32K PDP-8 MOS MEMORY ENGINEERING SPECIFICATION

GENERAL DESCRIPTION: The MS8-C is a 32K X 12 MOS memory using 4096 bit MOS RAM's, packaged on a standard hex module and designed to interface to the PDP-8 OMNIBUS. It requires +5 and -15 Volts.

DETAILED SPECIFICATIONS

PACKAGING: DEC standard hex module. Multilayer printed circuit board with inner layers distributing the +12V, +5V, -5V and ground. The module has a standard metal handle with retractors.

ADDRESS SPACE: May be 16K or 32K by 12 bits. For any of these options, the address space may be programmed by a dip switch to start on any 16K boundary from 0 to 128K. The memory size is programmed by a machine insertable jumper.

STORAGE DEVICE: The MS8-C uses the 16 pin, address multiplexed, dynamic 4096 bit MOS RAM as the storage device.

INTERFACE: The control logic is designed to provide complete timing for the RAM's. Connections are made on Connectors A thru E as outlined in Table 1. It will perform Fetch, Defer and Execute cycles in accordance with the OMNIBUS specification. In addition, the logic will perform refresh cycles, every 13.5 usec synchronized to be hidden in between the Read and Write half of any cycle. The control, to insure data integrity, forces asynchronous refresh cycles if the processor timing is halted due to a halt or an I/O stall.

Refresh is resynchronized with the processor by the use of the NTS Stall line. The processor timing is stalled at TP1 from 0 to 500 nsec on restart.

ROM ADRS L allows a ROM to overlay memory locations. The control performs a memory cycle but no data is put on the MD bus.

SOURCE H is used as the memory go signal and also is used to clear the MD bus at the start of a Fetch, Defer or Execute cycle.

The control requires initialization upon power up which is done by a positive transition on the POWER OK H line. The memory is ready for operation a maximum of 2.5 msec after POWER OK H. The memory is volatile so if power is lost, the memory data is lost.

The memory requires +5V, -15V and Ground to operate. The memory array requires +12V, -5V, +5V and Ground to operate. The module generates -5V from -15V through a fixed regulator. The +12V is generated from +5 through a switching regulator. The least significant bit of the refresh counter alternately drives a pair of transistors switches connected to a 1:3 step up transformer. The voltage on the secondary is rectified and put into a fixed 12V regulator. The drive transistors are controlled to not turn on unless the +5V is greater than 3.8V to prevent current surges on the +5 supply.

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They also are turned off if the -5V supply falls below -3V to protect the MOS RAM's. An etch inductor and a pair of capacitors between the transformer center taps and +5V prevents switching noise from being injected onto the +5V supply lines. DAI and EPI are the -5V margin and +12V margin control pins. Supplying a bi-directional voltage to these pins allows margining of the array during manufacturing test.

Both the -5V and the +12V supplies start automatically upon power up. Asynchronous refresh is also started automatically upon power up.

All MA and EMA lines are terminated with a clamp diode to prevent undershoot. BANK SEL 0L thru BANK SEL 3L are pulled up to +5 by a 10KΩ resistors since they are unterminated in systems not extended beyond 32K.

For manufacturing margining purposes, nodes in two resistor networks determining RAM timing are brought through buffer resistors to pins AA1 and BA1, T MARGIN 1 and T MARGIN 2.

Test points from the board position switches are brought to the E connector for manufacturing test, as is a refresh disable line, EA1, and the refresh oscillator output, DB1.

Four test points are brought to the connectors for the purpose of adjusting the internal timing on the module. They are TRAS L at CA1, TMUX L at AB1, TDSTB1L at BB1 and LOCKOUT L at CB1. These timing adjustments are made at module test.

POWER: The memory requires +5V ± 5% and -15V ± 10% inclusive of all abberations. The current required for operating and standby is shown below, assuming a maximum operating frequency of .83 MHz.

	16K				32K			
	OPERATE		STANDBY		OPERATE		STANDBY	
	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX
+5V	2.3 A	3.3 A	1.7 A	2.6 A	2.6 A	3.5 A	2.0 A	2.8 A
-15V	.05A	.07A	.05A	.07A	.05A	.07A	.05A	.07A
TOTAL WATTS	12.? W	17.6 W	9.3 W	14.1 W	13.8 W	18.6 W	10.8 W	15.1 W

SPEED: The access time assumes that no stall has occurred and is measured from SOURCE H to memory data on the MD lines.

T_{access}: 285 nsec Max
265 nsec Typ

T_{cycle}: 1.2 usec Max Fetch Cycle
1.4 usec Max Execute Cycle

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MTBF: Calculated by DEC Part Count method using F = .5%/1000 Hours for Ground Fixed MOS RAM and F = .3%/1000 Hours for Ground Benign.

	GROUND BENIGN	GROUND FIXED
16K X 12	48.3K Hours	23.4K Hours
32K X 12	28.5K Hours	15.0K Hours

ADJUSTMENTS: The internal memory timing is adjusted at module test by the removal or insertion of a resistor in the timing generators.

TRASL CA1 To TMUXL AB1

$25nsec < T_D < 45nsec$ OK

$T_D < 25$ nsec Insert R100

TRASL CA1 To TDSTB1L BB1

$200nsec < T_D < 220nsec$ OK

$T_D > 220nsec$ Cut R92 Out

$T_D < 200nsec$ Insert R140

TRASL CA1 To LOCKOUT L CB1

$130nsec < T_D < 150nsec$ OK

$T_D > 150nsec$ Insert R88

$T_D < 130nsec$ Cut R87 Out

MARGINS: The memory should operate with all permutations of +5 ± 5% and -15V ± 10% with any program and stored content. It should also run at +5V and -15V with Pins AA1 and BA1 tied to any voltage source between Ground and +5V, with any program and stored contents.

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ENVIRONMENTAL: DEC Std 102 Class "C".

TABLE 1

A CONN

SIDE 1		SIDE 2
T.P. T MARGIN 1	A	+5V
T.P. TMUXL	B	---
GND	C	GND
MA0L	D	EMA0L
MA1L	E	EMA1L
GND	F	GND
MA2L	H	EMA2L
MA3L	J	---
MD0L	K	MD DIR L
MD1L	L	SOURCE H
MD2L	M	STROBE H
GND	N	GND
MD3L	P	---
---	R	---
---	S	WRITE H
GND	T	GND
---	U	ROM ADRS L
---	V	---

B CONN

SIDE 1		SIDE 2
T.P. T MARGIN 2	A	+5V
T.P. T DSTB1L	B	---
GND	C	GND
MA4L	D	---
MA5L	E	---
GND	F	GND
MA6L	H	---
MA7L	J	---
MD4L	K	---
MD5L	L	---
MD6L	M	---
GND	N	GND
MD7L	P	---
---	R	STALL L
---	S	---
GND	T	GND
---	U	RUN L
---	V	POWER OK H

C CONN

SIDE 1		SIDE 2
T.P. TRAS L	A	+5V
T.P. LOCKOUT L	B	-15V
GND	C	GND
---	D	---
---	E	---
GND	F	GND
---	H	TP3H
---	J	---
BUS STROBE L	K	---
---	L	---
NOT LAST XFER L	M	---
GND	N	GND
---	P	---
---	R	---
---	S	---
GND	T	GND
---	U	---
---	V	---

D CONN

SIDE 1		SIDE 2
T.P. -5V MARGIN	A	---
T.P. REF OSC H	B	---
GND	C	GND
MA8L	D	---
MA9L	E	---
GND	F	GND
MA10L	H	---
MA11L	J	---
MD8L	K	---
MD9L	L	---
MD10L	M	---
GND	N	GND
MD11L	P	---
---	R	---
---	S	---
GND	T	GND
---	U	---
---	V	---

TABLE 1
(Continued)

E CONN

SIDE 1		SIDE 2
T.P. REF DIS L	A	---
T.P. POS 1	B	BANK SEL 0L
GND	C	GND
T.P. POS 2	D	BANK SEL 1L
T.P. POS 3	E	---
GND	F	GND
T.P. POS 4	H	---
T.P. POS 5	J	---
T.P. POS 6	K	---
T.P. POS 7	L	BANK SEL 2L
T.P. POS 8	M	---
GND	N	GND
T.P. +12V MARGIN	P	---
T.P. -5V	R	BANK SEL 3L
---	S	---
---	T	GND
---	U	---
T.P. +12V	V	---

F CONN

SIDE 1	SIDE 2
BLANK	

M8417-AA (16K)
X = SWITCH OPEN OR OFF

	E62-1	E62-2	E62-3	E62-4	E62-5	E62-6	E62-7	E62-8
Ø-16	X							
16-32		X						
32-48			X					
48-64				X				
6Ø-8Ø					X			
8Ø-96						X		
96-112							X	
112-128								X

M8417-BA (32K)
X = SWITCH OPEN OR OFF

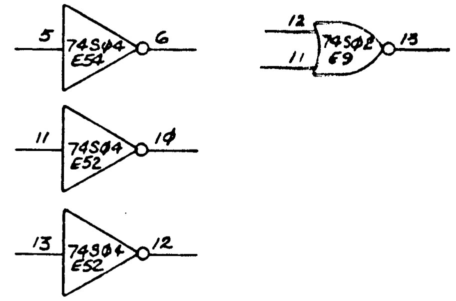
	E62-1	E62-2	E62-3	E62-4	E62-5	E62-6	E62-7	E62-8
Ø-32	X	X						
16-48		X	X					
32-64			X	X				
48-8Ø				X	X			
64-96					X	X		
8Ø-112						X	X	
96-128							X	X

NOTES:

1. MODULE DESIGNATION: M8417-AA = M8417-AB, -AC, -AD, -AE, ETC.
   16K MOS MEMORY
   REFERENCE DESIGNATIONS NOT USED:
   E1Ø1 E2Ø1 E3Ø1 E4Ø1
   E1Ø3 E2Ø3 E3Ø3 E4Ø3
   E1Ø5 E2Ø5 E3Ø5 E4Ø5
   E1Ø7 E2Ø7 E3Ø7 E4Ø7
   E1Ø9 E2Ø9 E3Ø9 E4Ø9
   E111 E211 E311 E411
   E113 E213 E313 E413
   E115 E215 E315 E415
   E117 E217 E317 E417
   E119 E219 E319 E419
   E121 E221 E321 E421
   E123 E223 E323 E423
2. MODULE DESIGNATION: M8417-BA = M8417-BB, -BC, -BD, -BE, ETC.
   32K MOS MEMORY
3. ALL 8837'S HAVE PINS 7 & 9 GROUNDED.
4. TIMING RESISTORS R87 AND R92 MAY BE REMOVED AT MODULE TEST FOR TIMING ADJUSTMENTS.
5. TIMING RESISTORS R88, R1ØØ, R14Ø MAY BE INSTALLED AT MODULE TEST FOR TIMING ADJUSTMENTS.

R88	3.16K 1/4W 1% MF	13-Ø3Ø45-ØØ
R1ØØ	6Ø4Ω 1/4W 1% MF	13-13155-ØØ
R14Ø	1.21K 1/4W 1% MF	13-Ø2871-ØØ

SPARES



JUMPER CONFIGURATIONS		
JUMPER	M8417-AA (16K)	M8417-BA (32K)
W2	X	X
W3	X	X
W4	X	X
W9	X	X
W1Ø	X	
W11	X	X

ALL JUMPERS ARE MACHINE INSERTABLE.

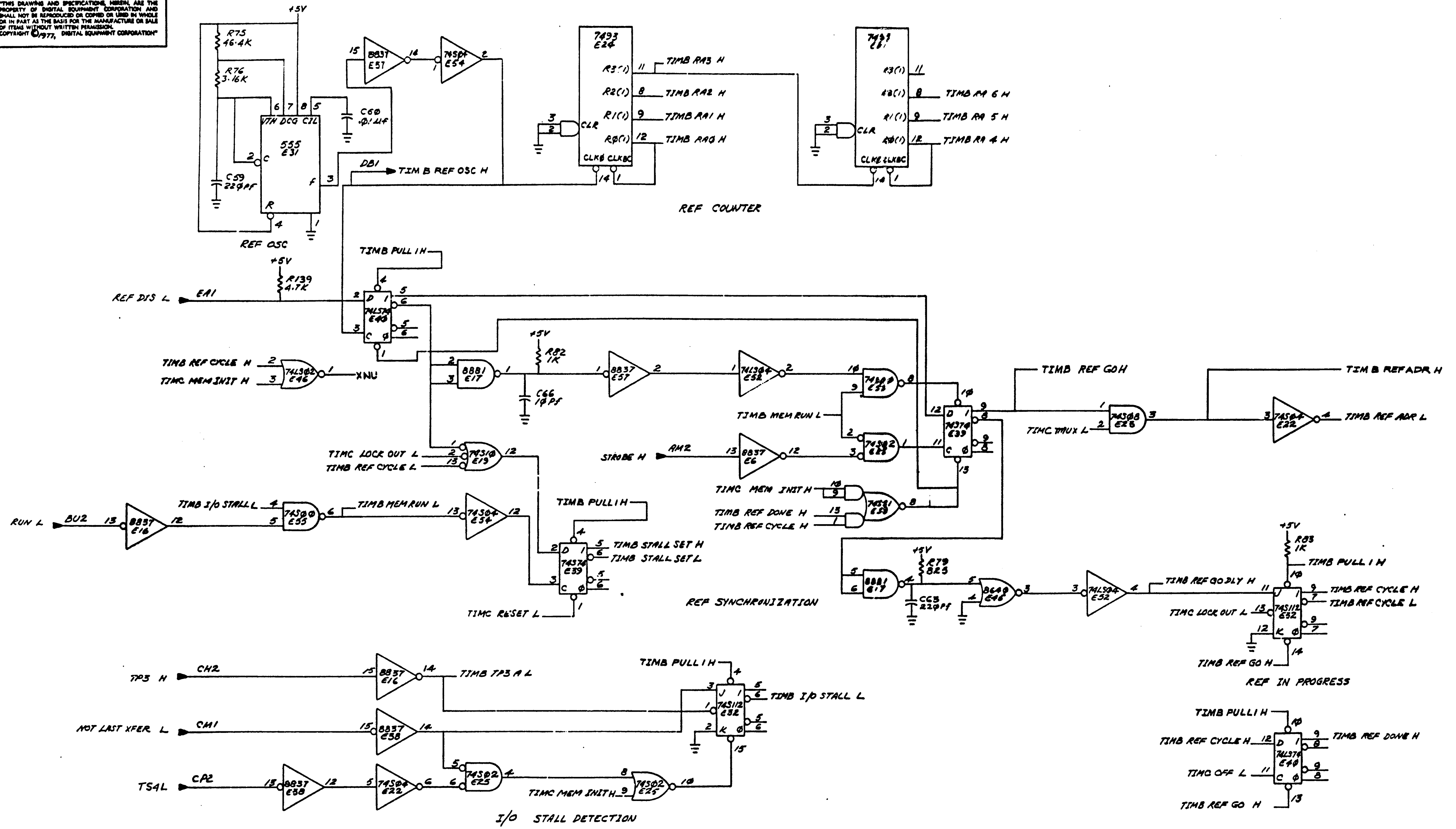
THESE JUMPERS ARE REMOVED:
W1, W5, W6, W7, W8, W12, W13, W14, W15, W16
X = JUMPER INSTALLATION

IC PIN LOCATIONS				
IC TYPE	GND	+5	-5	+12
555	1	8		
7493	1Ø	5		
74LS75	12	5		
864Ø	1	8		
751Ø7B	7	14	13	
MK4Ø27	16	9	1	8
OTHER 16 PIN IC'S	8	16		
OTHER 14 PIN IC'S	7	14		
75451	4	8		

REVISIONS

REV.	CHANGE NO.	CHK.
B	M8417-00001	J. STEGEMAN
C	M8417-00002	J. STEGEMAN
D	M8417-00003	J. STEGEMAN
E	8417-ML 6184	J. STEGEMAN

DRN. ANGEL COLON 4/29/77	FIRST USED ON MS8-C
CHK'D 7/1/77	TITLE
ENG. 7/1/77	PDP8 MOS MEMORY
PROJ. ENG.	
NEXT HIGHER ASSY. B-DD-M8417-Ø	SIZE D, CODE CS, NUMBER M8417-Ø-1, REV. E
SCALE NONE	
SHEET 1 OF 14	DIST.



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE: PDP8 MOS MEMORY (TIM B)

SIZE: D | CODE: CS | NUMBER: M8417-0-1 | REV.: E

SCALE: NONE | SHEET 2 OF 14

ML

* NOTE: THESE RESISTORS MAY BE REMOVED AT MODULE TEST TO ADJUST THE TIMING.

** NOTE: THESE RESISTORS MAY BE INSERTED AT MODULE TEST TO ADJUST THE TIMING.

TIMING GO LOGIC

POWER UP INIT

MD LATCH CLR

TIMING GENERATORS

HOLD OFF CKT

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	PDP8 MOS MEMORY (TIMC)		SIZE D	CODE DCS	NUMBER M8417-0-1 REV. E
SCALE NONE	SHEET 3 OF 14		DIST.		