# PART 3
# REAL-TIME CLOCK OPTIONS

# CHAPTER 1
# REAL-TIME CLOCK OPTIONS

## SECTION 1 INTRODUCTION

Three real-time clock options are available for use with the PDP-8/E. The DK8-EA and DK8-EC are similar; each consists of a clock frequency source and control logic contained on a single quad module that plugs into the OMNIBUS. These two clock options cause program interrupts of the PDP-8/E at predetermined intervals that are not subject to program control. The options can be used by the programmer to sample processes or to count events. The DK8-EP, a more sophisticated clock option, provides a large amount of program control. It provides the means to measure and/or count intervals and events in different ways. This option is discussed in detail in the *LAB 8-E Maintenance Manual*. Only the DK8-EA and DK8-EC are discussed here.

## SECTION 2 BLOCK DIAGRAM

The difference between the DK8-EA and DK8-EC options is the way in which the clock frequency source operates. The DK8-EA derives a clock frequency of 100 Hz (for 50-Hz primary power) or 120 Hz (for 60-Hz primary power) from a power supply ac voltage. The DK8-EC derives a clock frequency of 1 Hz, 50 Hz, 500 Hz, or 5 kHz from a 20-MHz crystal-controlled oscillator. Because the options are similar in all other respects, the logic description pertains to both, except when the clock frequency logic is discussed. Reference designations on logic symbols, E3, E12, for example, are for reference only. They may or may not coincide with the reference designations on a specific schematic drawing.

Figure 1-1 is a block diagram of the DK8-EA/C. The control logic consists of the select logic, the INTERRUPT flip-flop logic, and the clock flag logic. The clock frequency is provided by the clock logic.

When an IOT instruction causes I/O PAUSE L to be asserted by the CPU Timing Generator, the option select logic decodes bits MD-03 through MD-11. The INTERNAL I/O L signal is asserted to direct the positive I/O bus interface to ignore the IOT instruction. The three instructions that pertain to the DK8-EA/C are 6131, 6132, and 6133. 6131 and 6132 are used in the INTERRUPT flip-flop logic where they set and clear, respectively, the INTERRUPT flip-flop. If this flip-flop is set, the clock flag is logically connected to the interrupt system. Upon receipt of an interrupt request, the computer begins to execute the interrupt servicing routine to determine the identity of the requesting device. When the 6133 instruction in the servicing routine is decoded, the clock flag logic asserts SKIP L. At the same time, the CLOCK FLAG flip-flop is cleared. The computer then proceeds to the subroutine associated with the Real-Time Clock option. Both the INT RQST L and SKIP L signals are negated. The next clock pulse asserts INT RQST L again and the procedure is repeated. Each succeeding clock pulse causes an interrupt request until the 6132 instruction clears the INTERRUPT flip-flop.

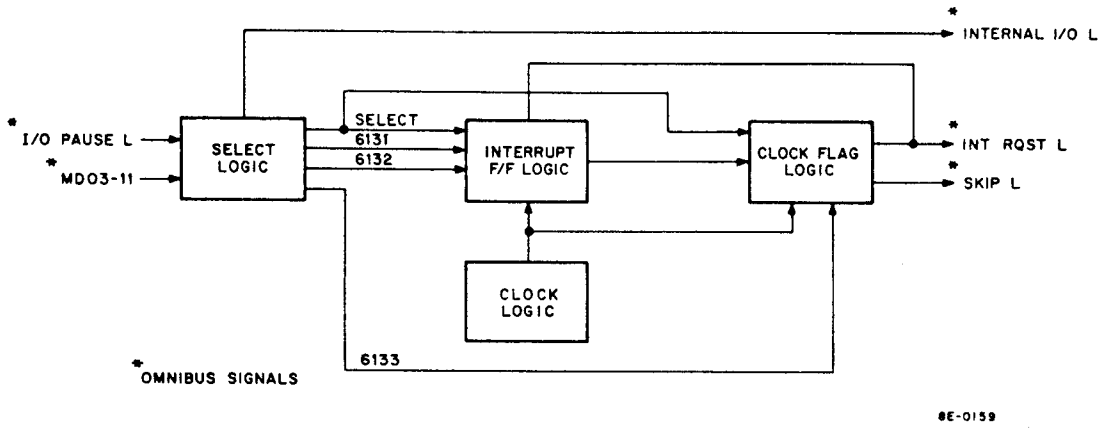


Figure 1-1 Real-Time Clock (DK8-EA, DK8-EC), Block Diagram

## SECTION 3 DETAILED LOGIC

### 1.1 SELECT LOGIC

The select logic is shown in Figure 1-2. The SELECT signal is asserted by NAND gate E5 when a 613X instruction is decoded. The SELECT signal, in turn, asserts INTERNAL I/O L, which causes the positive I/O bus interface to ignore the IOT instruction. The SELECT signal is gated with bits MD-09 through MD-11 to provide instruction 6131, 6132, or 6133.

### 1.2 INTERRUPT FLIP-FLOP LOGIC

The INTERRUPT flip-flop logic is shown in Figure 1-3. The flip-flop, E11B, is cleared by INITIALIZE; it can be set by the first clock pulse following power turn-on. This flip-flop remains set until cleared by the 6133 instruction, as is discussed in Paragraph 1.3.

The first TP1 pulse to be generated after E11A is set causes flip-flop E7 to be set; the 1-output of E7 provides the desired high level at one input of NAND gate E9. The other input of the gate is from the 1-output of the INTERRUPT flip-flop. If the select logic decodes 6131, the INTERRUPT flip-flop is set at TP3 and E9 asserts INT RQST L.

The 6132 instruction is used to disable the interrupt capability of the option. It, like the 6131 instruction, is contained in the background program and, when decoded by the select logic, clears the INTERRUPT flip-flop at TP3.

### 1.3 CLOCK FLAG LOGIC

The clock flag logic is shown in Figure 1-4. When 6133, which is usually located in the interrupt servicing routine, is decoded by the select logic, NAND gate E9B in the clock flag logic asserts SKIP L (E7 is set at TP1 following power turn-on). At TP3, the CLOCK FLAG flip-flop is cleared. Simultaneously, the CPU SKIP flip-flop, which is conditioned by SKIP L, is set. This action causes the program counter to be incremented during TS4. Thus, the instruction following 6133 is skipped and the next instruction that is performed is the first instruction of the real-time-clock subroutine. At TP1 of this instruction, latch E7 in the clock flag logic is cleared, negating both

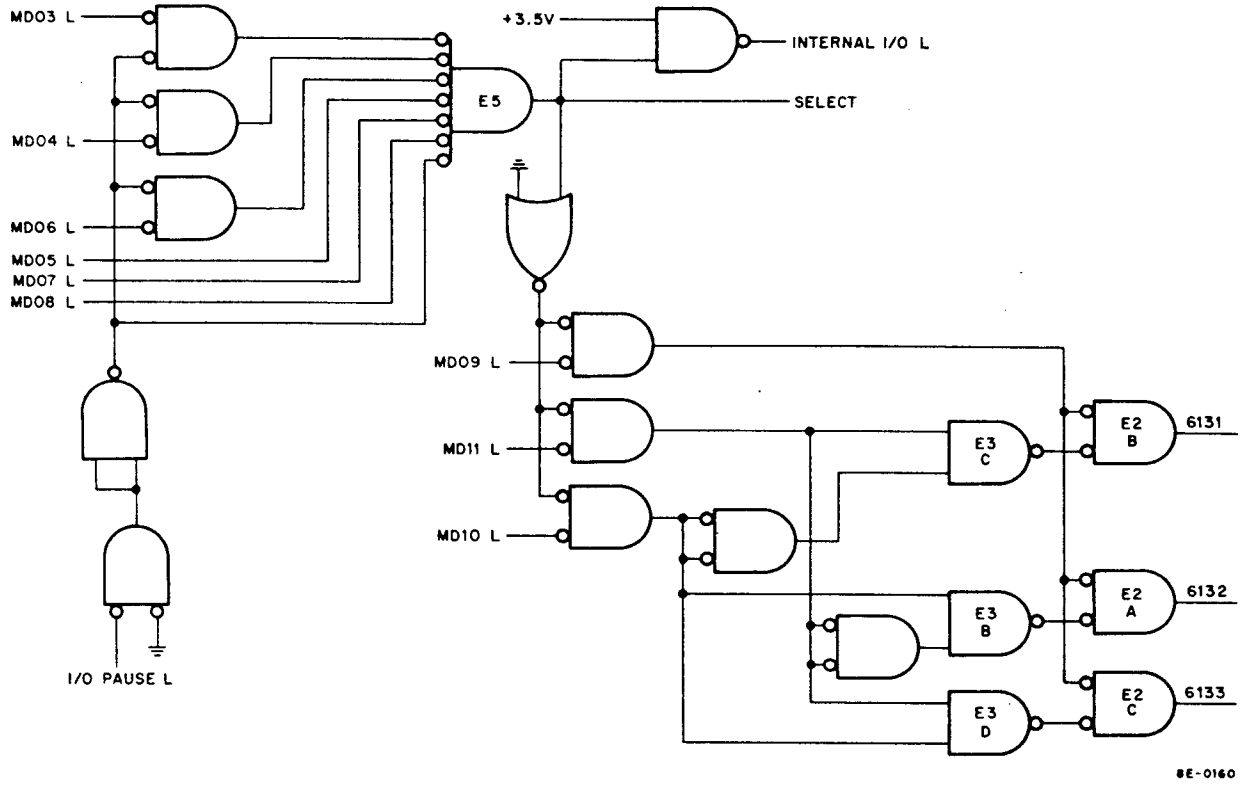


Figure 1-2 Select Logic

INT RQST L and SKIP L. The next interrupt request occurs when the CLOCK FLAG flip-flop is again set by a clock pulse and the following TP1 pulse causes E7 to be set.

Naturally, the time required for the service loop must be less than the clock period. Furthermore, the clock is free-running. Hence, the program must be able to handle two nearly simultaneous clock interrupts when the CLOCK INTERRUPT flip-flop is enabled. Consider what happens if the clock is enabled just before it is ready to generate a clock pulse. The enabling process generates an interrupt and the CPU may still be executing the first clock subroutine when the option requests the second program interrupt. If this occurs, the interrupt servicing routine is entered immediately after the first clock subroutine is exited, and the second execution of the subroutine occurs just after the first. Thus, an uncertainty of one count is always present because of the unknown clock phase.

## 1.4 CLOCK LOGIC

### 1.4.1 DK8-EA

The clock logic for the DK8-EA is shown in Figure 1-5. The DK8-EA connects to the 28-Vac output of the H724 or H724A Power Supply via the cable supplied with the option. The cable connects to the option with an 8-pin connector (2 pins are not used). Each ac input is wired, via the board etch, to an adjacent pin so that the 28 Vac is not dead-ended (the KP8-E Power Fail and Auto Restart option also uses the 28-Vac output of the power supply; if both options are in the system, one is connected directly to the power supply, while the second is connected to J1 of the first).