PART 3
REAL-TIME CLOCK OPTIONS

CHAPTER 1
REAL-TIME CLOCK OPTIONS

SECTION 1 INTRODUCTION

Three real-time clock options are available for use with the PDP-8/E. The DK8-EA and DK8-EC are similar; each consists of a clock frequency source and control logic contained on a single quad module that plugs into the OMNIBUS. These two clock options cause program interrupts of the PDP-8/E at predetermined intervals that are not subject to program control. The options can be used by the programmer to sample processes or to count events. The DK8-EP, a more sophisticated clock option, provides a large amount of program control. It provides the means to measure and/or count intervals and events in different ways. This option is discussed in detail in the *LAB 8-E Maintenance Manual*. Only the DK8-EA and DK8-EC are discussed here.

SECTION 2 BLOCK DIAGRAM

The difference between the DK8-EA and DK8-EC options is the way in which the clock frequency source operates. The DK8-EA derives a clock frequency of 100 Hz (for 50-Hz primary power) or 120 Hz (for 60-Hz primary power) from a power supply ac voltage. The DK8-EC derives a clock frequency of 1 Hz, 50 Hz, 500 Hz, or 5 kHz from a 20-MHz crystal-controlled oscillator. Because the options are similar in all other respects, the logic description pertains to both, except when the clock frequency logic is discussed. Reference designations on logic symbols, E3, E12, for example, are for reference only. They may or may not coincide with the reference designations on a specific schematic drawing.

Figure 1-1 is a block diagram of the DK8-EA/C. The control logic consists of the select logic, the INTERRUPT flip-flop logic, and the clock flag logic. The clock frequency is provided by the clock logic.

When an IOT instruction causes I/O PAUSE L to be asserted by the CPU Timing Generator, the option select logic decodes bits MD-03 through MD-11. The INTERNAL I/O L signal is asserted to direct the positive I/O bus interface to ignore the IOT instruction. The three instructions that pertain to the DK8-EA/C are 6131, 6132, and 6133. 6131 and 6132 are used in the INTERRUPT flip-flop logic where they set and clear, respectively, the INTERRUPT flip-flop. If this flip-flop is set, the clock flag is logically connected to the interrupt system. Upon receipt of an interrupt request, the computer begins to execute the interrupt servicing routine to determine the identity of the requesting device. When the 6133 instruction in the servicing routine is decoded, the clock flag logic asserts SKIP L. At the same time, the CLOCK FLAG flip-flop is cleared. The computer then proceeds to the subroutine associated with the Real-Time Clock option. Both the INT RQST L and SKIP L signals are negated. The next clock pulse asserts INT RQST L again and the procedure is repeated. Each succeeding clock pulse causes an interrupt request until the 6132 instruction clears the INTERRUPT flip-flop.

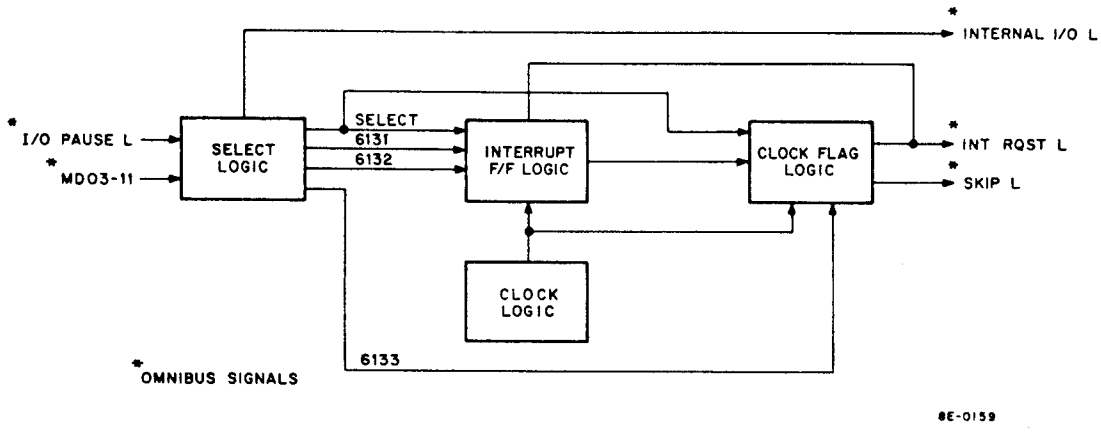


Figure 1-1 Real-Time Clock (DK8-EA, DK8-EC), Block Diagram

SECTION 3 DETAILED LOGIC

1.1 SELECT LOGIC

The select logic is shown in Figure 1-2. The SELECT signal is asserted by NAND gate E5 when a 613X instruction is decoded. The SELECT signal, in turn, asserts INTERNAL I/O L, which causes the positive I/O bus interface to ignore the IOT instruction. The SELECT signal is gated with bits MD-09 through MD-11 to provide instruction 6131, 6132, or 6133.

1.2 INTERRUPT FLIP-FLOP LOGIC

The INTERRUPT flip-flop logic is shown in Figure 1-3. The flip-flop, E11B, is cleared by INITIALIZE; it can be set by the first clock pulse following power turn-on. This flip-flop remains set until cleared by the 6133 instruction, as is discussed in Paragraph 1.3.

The first TP1 pulse to be generated after E11A is set causes flip-flop E7 to be set; the 1-output of E7 provides the desired high level at one input of NAND gate E9. The other input of the gate is from the 1-output of the INTERRUPT flip-flop. If the select logic decodes 6131, the INTERRUPT flip-flop is set at TP3 and E9 asserts INT RQST L.

The 6132 instruction is used to disable the interrupt capability of the option. It, like the 6131 instruction, is contained in the background program and, when decoded by the select logic, clears the INTERRUPT flip-flop at TP3.

1.3 CLOCK FLAG LOGIC

The clock flag logic is shown in Figure 1-4. When 6133, which is usually located in the interrupt servicing routine, is decoded by the select logic, NAND gate E9B in the clock flag logic asserts SKIP L (E7 is set at TP1 following power turn-on). At TP3, the CLOCK FLAG flip-flop is cleared. Simultaneously, the CPU SKIP flip-flop, which is conditioned by SKIP L, is set. This action causes the program counter to be incremented during TS4. Thus, the instruction following 6133 is skipped and the next instruction that is performed is the first instruction of the real-time-clock subroutine. At TP1 of this instruction, latch E7 in the clock flag logic is cleared, negating both

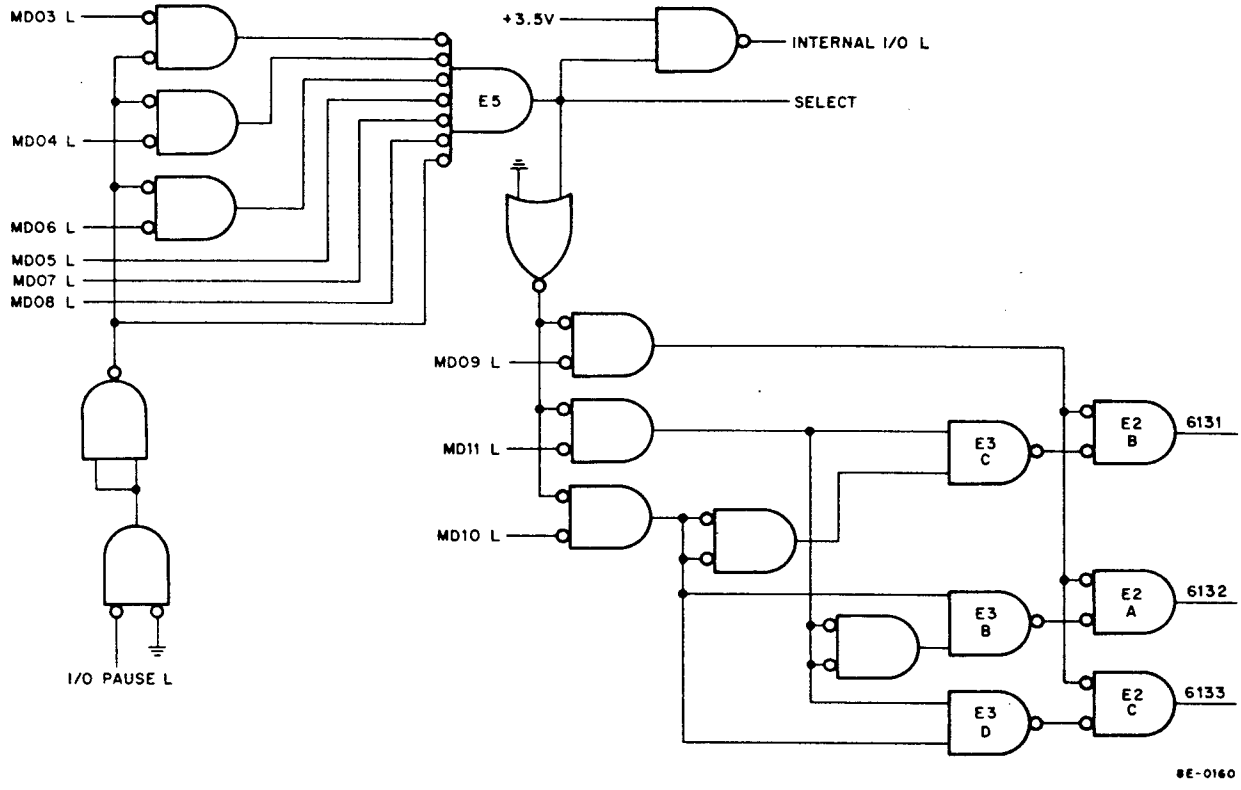


Figure 1-2 Select Logic

INT RQST L and SKIP L. The next interrupt request occurs when the CLOCK FLAG flip-flop is again set by a clock pulse and the following TP1 pulse causes E7 to be set.

Naturally, the time required for the service loop must be less than the clock period. Furthermore, the clock is free-running. Hence, the program must be able to handle two nearly simultaneous clock interrupts when the CLOCK INTERRUPT flip-flop is enabled. Consider what happens if the clock is enabled just before it is ready to generate a clock pulse. The enabling process generates an interrupt and the CPU may still be executing the first clock subroutine when the option requests the second program interrupt. If this occurs, the interrupt servicing routine is entered immediately after the first clock subroutine is exited, and the second execution of the subroutine occurs just after the first. Thus, an uncertainty of one count is always present because of the unknown clock phase.

1.4 CLOCK LOGIC

1.4.1 DK8-EA

The clock logic for the DK8-EA is shown in Figure 1-5. The DK8-EA connects to the 28-Vac output of the H724 or H724A Power Supply via the cable supplied with the option. The cable connects to the option with an 8-pin connector (2 pins are not used). Each ac input is wired, via the board etch, to an adjacent pin so that the 28 Vac is not dead-ended (the KP8-E Power Fail and Auto Restart option also uses the 28-Vac output of the power supply; if both options are in the system, one is connected directly to the power supply, while the second is connected to J1 of the first).

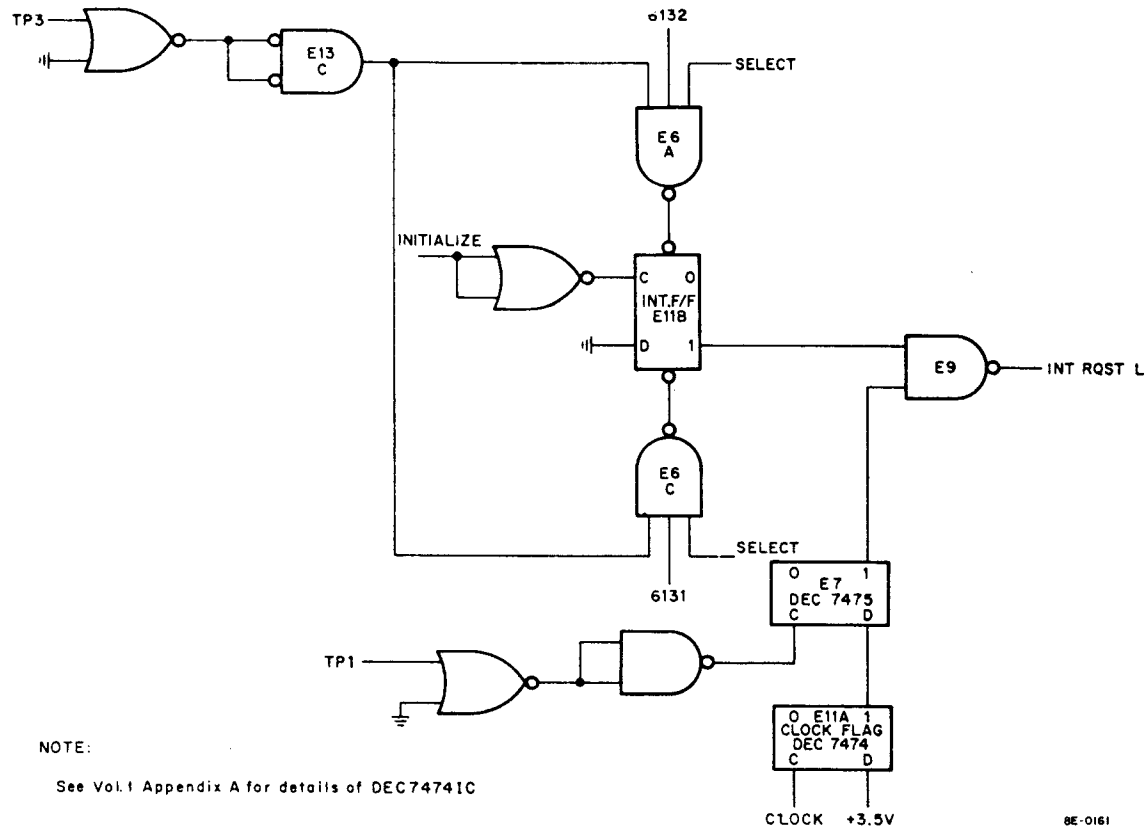


Figure 1-3 INTERRUPT Flip-Flop Logic

The circuit consists of a full-wave rectifier, a clamp, and a Schmitt trigger. The rectified ac voltage is clamped to +5V by D1 to prevent damage to the E12 IC. E12 is wired as a Schmitt trigger and its output is a reasonably well-shaped square wave with a pulse repetition frequency that is twice the frequency of the primary power source.

1.4.2 DK8-EC

The clock logic for the DK8-EC is shown in Figure 1-6. The basic clock frequency, 20 MHz, is provided by a crystal-controlled oscillator (see the option schematic). This frequency is divided by a factor of four by the two J-K flip-flops, E17 and E18 (when both the J and the K inputs are high, the 1 output is changed with each positive transition at the C input). The 5-MHz clock frequency is applied to a chain of DEC 7490 decade counters, each counter except the last is wired to divide by ten; the last counter is wired to divide by five. The output of counter E4, E8, E12, or E21 can be selected by connecting a jumper wire, as illustrated in Figure 1-6. (The option is manufactured with an etch connection from the output of E21 to the terminal that connects to the CLOCK FLAG flip-flop; if a clock frequency of other than 1 Hz is desired, cut the etch connection and wire a jumper from the terminal to the desired flip-flop output.)

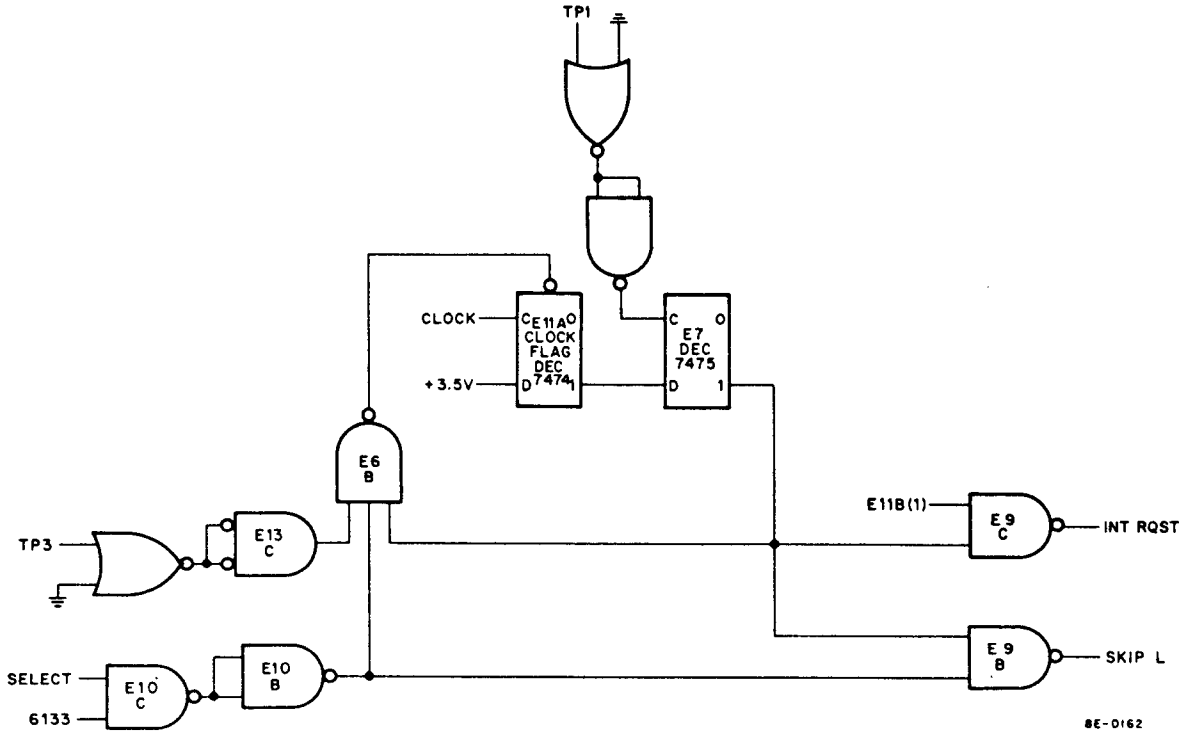


Figure 1-4 Clock Flag Logic

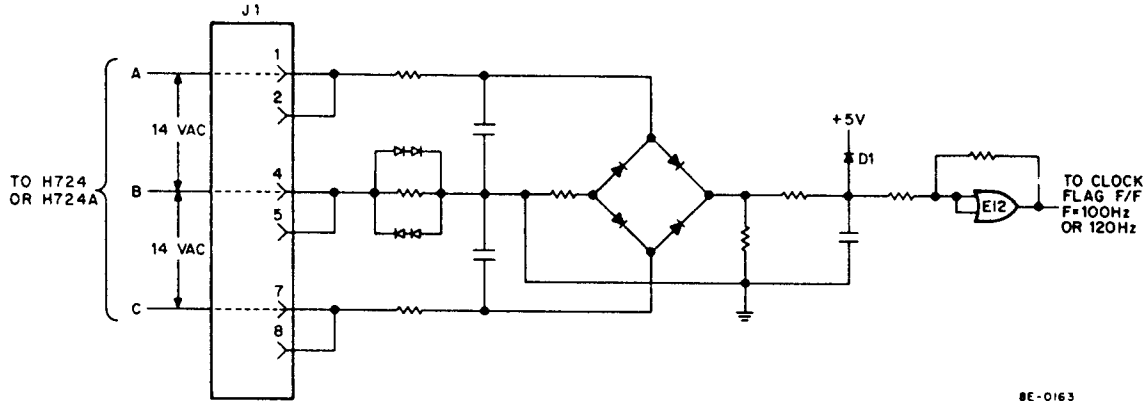


Figure 1-5 Clock Logic DK8-EA

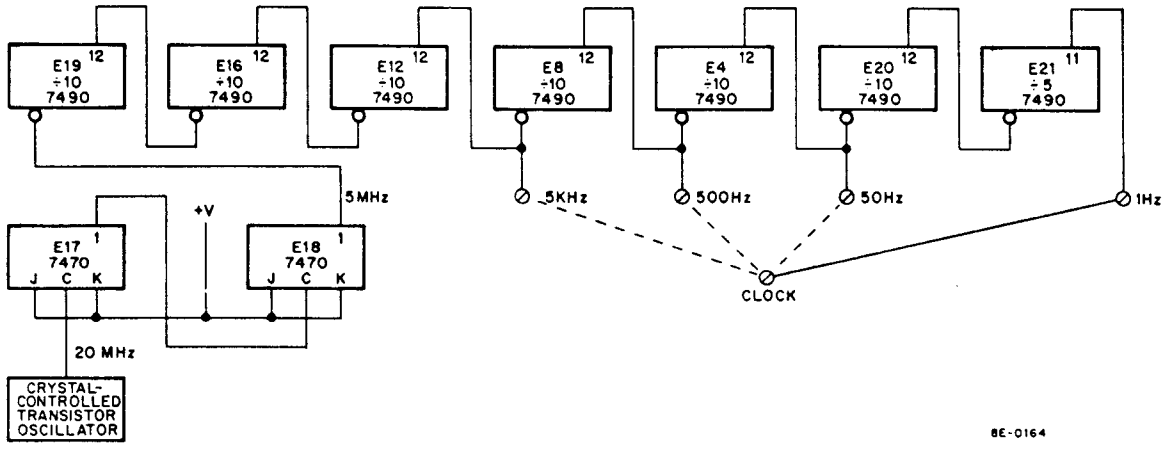


Figure 1-6 Clock Logic, DK8-EC

SECTION 4 MAINTENANCE

General instructions concerning preventive and corrective maintenance are given in Chapter 4, Volume 1. When corrective maintenance is required, use the MAINDEC-8E-D8AA maintenance program to determine the nature of the problem. The option schematics, E-CS-M883-0-1, E-CS-M882-0-1, E-CS-M860-0-1, and E-CS-M518-0-1 must be referred to for IC locations and pin numbers. Test points are provided on the option to facilitate trouble-shooting.

SECTION 5 SPARE PARTS

Table 1-1 lists the M882/M883 spare parts. Spare parts can be obtained from any local DEC office or from DEC, Maynard, Massachusetts.

Table 1-1
Recommended DK8-EA/DK8-EC – (M882/M883) Spare Parts

DEC Part No.	Description	Quantity
19-9705	DEC 8881	1
19-9704	DEC 314	1
19-9485	DEC 380	1
19-9051	DEC 7490	1
19-9050	DEC 7475	1
19-9004	DEC 7402	1
19-5589	DEC 7470	1
19-5576	DEC 7410	1
19-5575	DEC 7400	1
19-5547	DEC 7474	1
19-9486	DEC 384	1

(continued on next page)

Table 1-1 (Cont)

Recommended DK8-EA/DK8-EC – (M882/M883) Spare Parts

DEC Part No.	Description	Quantity
18-9880	Crystal (M883 only)	1
16-9651	Pulse Transformer (M883 only)	1
10-9678	Capacitor 0.047 μF, 16-15 + 20%	1
10-1610	Capacitor 0.01 μF, 100V, 20%	1
10-0016	Capacitor 100 pF, 100V, 5%	1
10-0014	Capacitor 68 pF, 100V, 5%	1
10-0011	Capacitor 47 pF, 100V, 5%	1
10-0006	Capacitor 10 pF, 100V, 5%	1
10-1765	Capacitor 0.005 μF,	1

PART 4
POWER-FAIL OPTION

CHAPTER 1

KP8-E POWER-FAIL AND AUTO-RESTART

SECTION 1 INTRODUCTION

The KP8-E Power-Fail and Auto-Restart option monitors the computer's primary power source and initiates a controlled shut-down sequence if a power failure occurs. This power-fail sequence protects the operating program by storing the contents of the PC Register, AC Register, MQ Register, and the Link in known memory locations. When normal primary power is restored, the KP8-E automatically restarts the computer in location 0000, 0200, 1000, 2000, or 4000. The address is selected by installing a jumper.

The KP8-E Power-Fail and Auto-Restart option consists of the M848 quad module which is inserted into the OMNIBUS and connected to the computer ac power supply by a 7007128 power cable. The PDP-8/E supplies 28 Vac and the PDP-8/F and PDP-8/M supply 56 Vac. The 56 Vac input is reduced to 28 Vac by removing a jumper (W2) on the M848 module.

SECTION 2 M848 BLOCK DIAGRAM

The KP8-E block diagram is shown in Figure 1-1. The power monitor logic checks the PDP-8/E power supply 28 Vac output or the PDP-8/F and PDP-8/M 56 Vac power supply output which reflects the condition of the primary power source. If line voltage drops below a predetermined minimum value, the UP signal is negated and the PWR LOW flip-flop is set, asserting the OMNIBUS INT RQST L signal. Filter capacitors in the power supply guarantee continued operation for 1 ms; this is sufficient time for the interrupt request to be recognized and the program interrupt routine to be carried out (because of the time limitation, the KP8-E SPL instruction, Skip on PWR LOW flag, 6102, should be the first status check made by the program interrupt routine).

SECTION 3 M848 DETAILED LOGIC

1.1 SELECT LOGIC

The select logic is shown in Figure 1-2. When the SPL instruction (6102) is decoded, the logic asserts the INTERNAL I/O L signal that causes the Positive I/O Bus Interface to ignore the IOT instructions. The status of the PWR LOW flip-flop is checked; if the flag is set, indicating a power failure has occurred, the SKIP L signal is asserted. The program then skips the next sequential instruction and jumps to a subroutine that begins executing the power-fail routine.

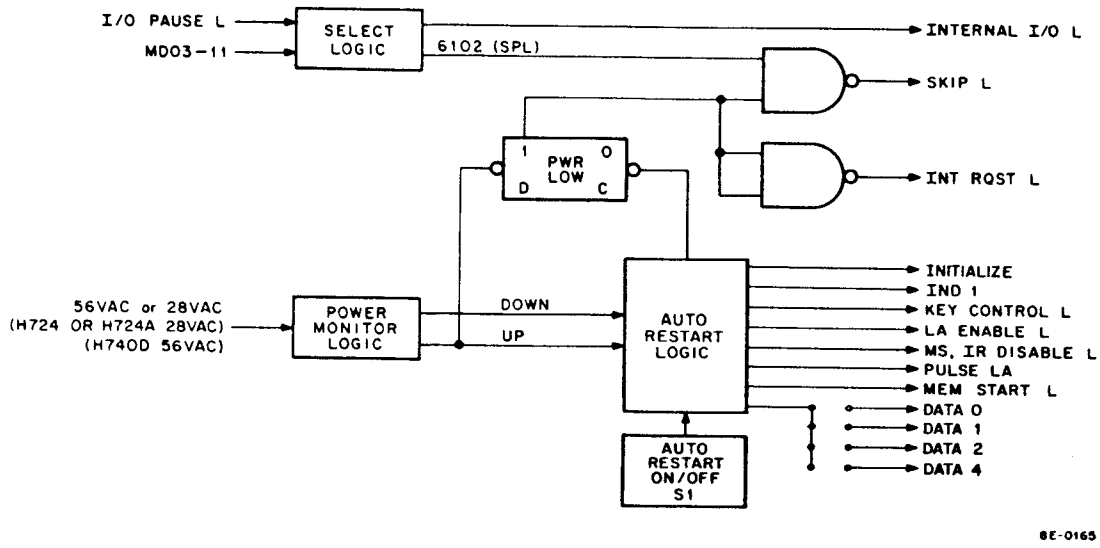


Figure 1-1 M848 Power-Fail and Auto-Restart Option, Block Diagram

1.2 POWER MONITOR LOGIC

The power monitor logic is shown in Figure 1-3. The logic directly monitors the ac output of the computer's power supply, to which the option is connected by a cable. The cable connects to the option with an 8-pin connector (2 pins are not used). Each ac input at J1 is wired via the board etch to an adjacent pin so that the ac is not dead-ended (the DK8-E Real-Time Clock option (line frequency) also uses the ac output of the power supply; if both options are in the system, one is connected directly to the power supply while the second is connected to J1 of the first).

NOTE

The W2 jumper must be removed when the KP8-E is installed in a PDP-8/F or PDP-8/M.

The ac is full-wave rectified and applied to two comparator circuits. One of these circuits includes transistor pair Q4/Q5 and initiates the auto-restart sequence. The second circuit includes transistor pair Q2/Q3 and initiates the power-fail sequence. There are two thresholds for power fail. An upper threshold, 103 Vac, which is used to start the RESTART logic, and a lower threshold, 93 Vac, which sets the PWR LOW flip-flop. Q4 and Q5 detects the 103 Vac threshold; Q2 and Q3 detect the 93 Vac threshold. The upper and lower thresholds have a tolerance of ±1.0V. Q2 provides a trigger for one-shot E7 when the amplitude of the line voltage, and hence, the amplitude of the ac input of J1, is above the desired minimum. The -10.3 Vdc reference voltage is generated by a precision voltage regulator that is not shown (see the option schematic for this and for the resistor network).

The resistor network is equipped with jumpers that are installed to keep the power-fail line voltage thresholds at their correct value, independent of nominal line voltage. Table 1-1 shows the jumpers that should be installed for 115/230, 220, and 240 Vac inputs.

WARNING

The two threshold adjustments on the resistor network should not be adjusted in the field. These potentiometers are set at the factory to compensate for component tolerances.

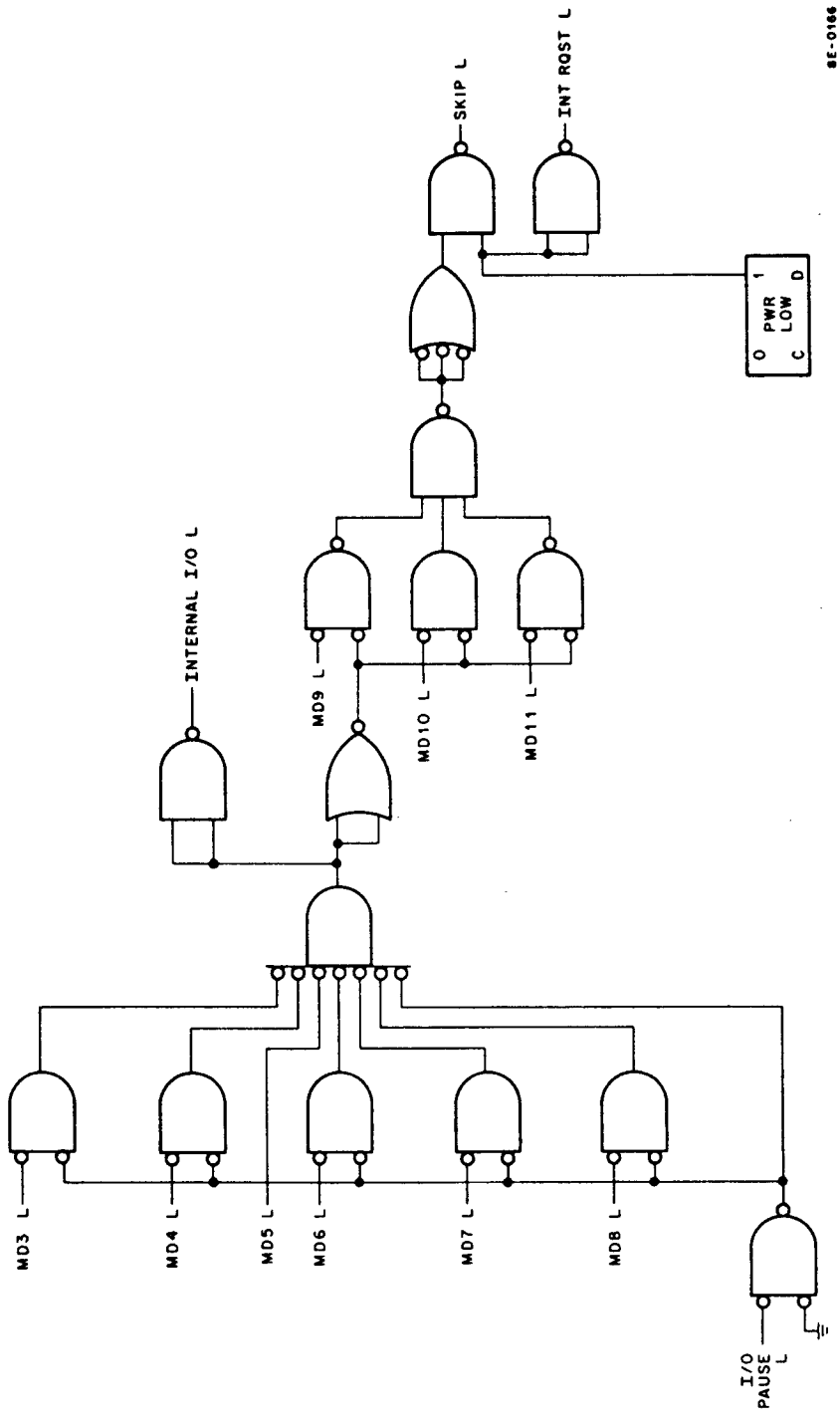


Figure 1-2 Select Logic

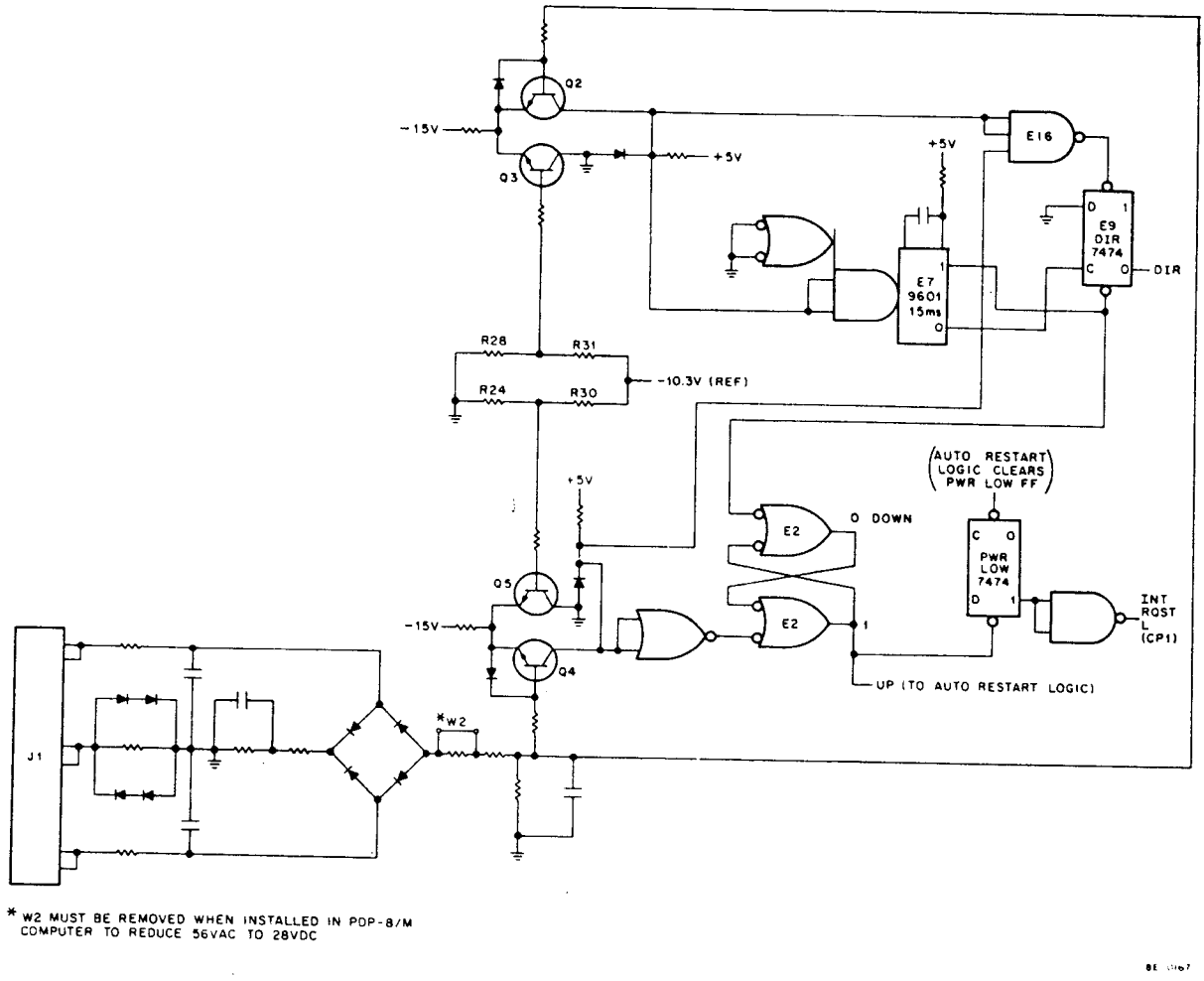


Figure 1-3 Power Monitor Logic

Table 1-1
Jumper Installation

Line Voltage (Nominal Value)	Add Jumpers Labeled	Remove Jumpers Labeled
115/230	115/230 and 240	220
220	220	115/230
240	115/230	220 and 240

Figure 1-4 presents idealized waveforms to illustrate how E7 is controlled by the comparator circuit. If the line voltage is above the selected minimum value, the positive transition at the collector of Q2 will be of sufficient amplitude to trigger E7. Because the period of the collector waveform is less than the triggered delay time of E7, the one-shot will remain active. If the line voltage falls below the minimum value for as little as one-half cycle, as illustrated, E7 times out and an interrupt request is generated. Even though the power recovers almost instantaneously, the power-fail sequence is carried out.

The timing diagram shows the UP signal being asserted by the half-cycle immediately following the missing half-cycle. Thus, the auto-restart sequence begins 1.5 seconds later, as detailed in the following paragraphs.

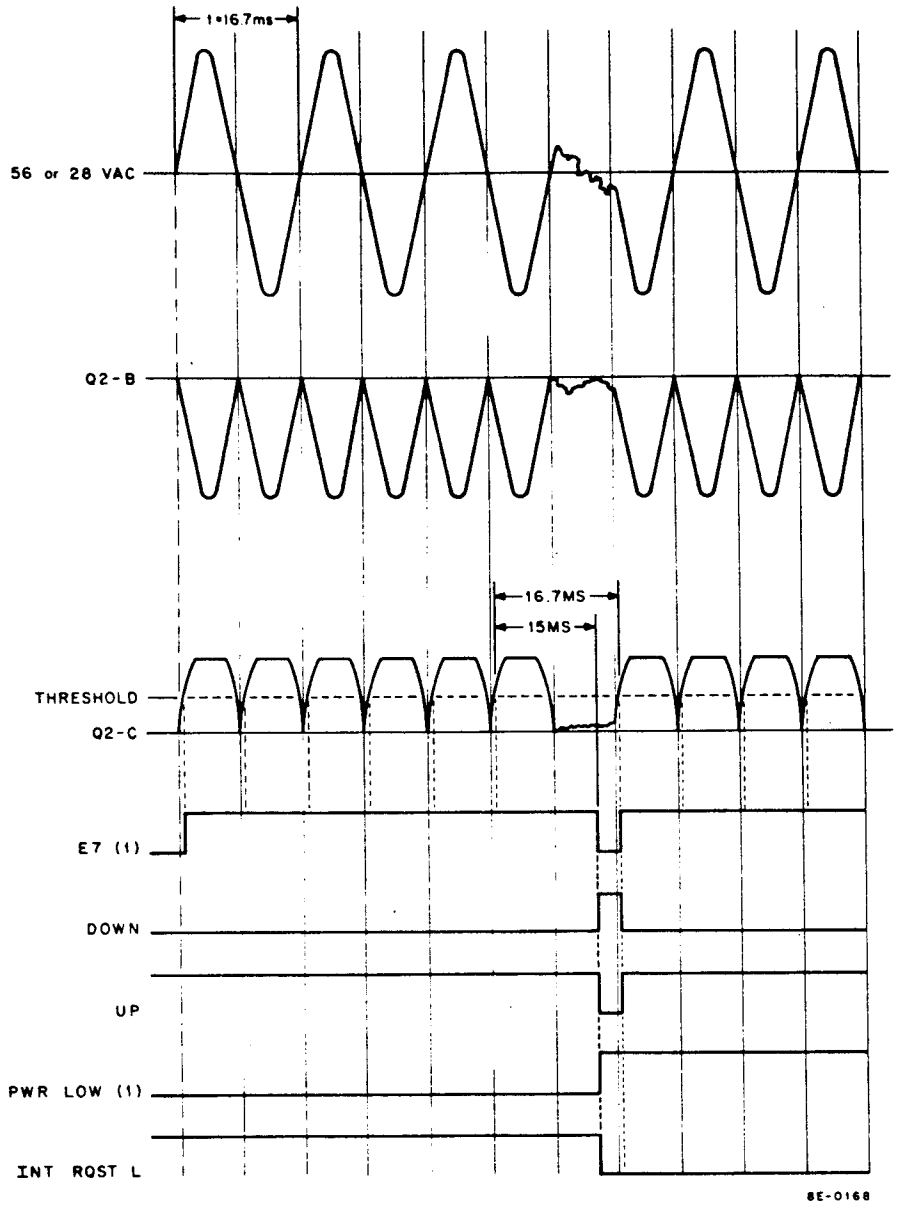


Figure 1-4 Power Fail Timing

1.3 AUTO-RESTART LOGIC

The computer must resume operation by executing the instruction that was stored in the starting location by the power-fail routine. Consequently, the CPMA Register and the IF and DF Registers of the KM8-E option must be loaded with the starting address before CPU timing is renewed. Furthermore, the CPU Major State Register must be manipulated so that a FETCH cycle is entered when timing begins. The auto-restart logic meets these requirements by simulating some of the operations that normally occur when the programmer's console is being used.

Thus, to load the CPMA Register with the starting address, the auto-restart logic first asserts the LA ENABLE L signal (at the same time, the MS, IR DISABLE L signal is asserted, this signal places the CPU in the DMA state, ensuring that the first timing cycle begins in the FETCH state). The LA ENABLE L signal:

a. ensures that only "bus" information is placed on the DATA 0–11 lines; because nothing has access to "bus" at this time, the DATA 0–11 lines carry the starting address jumper selected at the output of E3 (Figure 1-5) (Volume 1, Section 5, Paragraph 3.3.3, for clarification),

b. causes the address on the DATA 0–11 lines to be gated through the CPU Major Register gating to the MAJOR REGISTERS BUS.

After a delay to ensure that the control lines have settled, the logic asserts PULSE LA. This signal causes the CPU to generate the CPMA LOAD L signal that loads the CPMA Register with the starting address. CPMA LOAD L also sets the F flip-flop of the Major State Register; thus, a FETCH cycle will be entered when timing begins. IND1 is asserted at the same time as LA ENABLE to ensure only the starting address bits are on the bus if the programmer's console is not installed (Volume 1, Paragraph 3.33.10).

When the CPMA Register has been loaded and the F flip-flop set, the auto-restart logic asserts the KEY CONTROL L signal. After a delay that enables the control line to settle, PULSE LA is asserted again. However, because KEY CONTROL L is true, CPMA LOAD L is not generated by this assertion of PULSE LA, nor is the Major State Register clocked.

Rather, the 0s on the DATA 6–11 lines are loaded into the IF and DF Registers of the KM8-E option (the auto-restart logic allows for the KM8-E option even if the option is not contained in the system). After this assertion of the PULSE LA signal, the MS, IR DISABLE L, IND1, and LA ENABLE L signals are negated and a final delay period is allowed. When this delay times out, MEM START L is asserted, initiating CPU timing, and the computer fetches the instruction from location 0000, 0200, 1000, 2000 or 4000 of field 0. The starting address is determined by the output of E3 (Figure 1-5) which pulls DATA 0, DATA 1, DATA 2, or DATA 4 low at the same time PULSE LA is asserted.

The auto-restart logic is shown in Figure 1-5; the relative timing of the logic is shown in Figure 1-6. The ENABLE/DISABLE switch, S1, must be in the ENABLE position (up) if the automatic restart is to function after a power interrupt has occurred. If S1 is in the DISABLE position, the PWR LOW flip-flop is cleared when ac power comes up, but the program must be restarted manually.

The auto-restart sequence begins when the power monitor logic asserts the UP signal. The positive transition of this signal triggers one-shot multivibrator E2. During the active 1.5 seconds of this one-shot, all system equipment (computer, peripherals, options) can complete operations initiated by the OMNIBUS INITIALIZE signal. The LA flip-flop is set and at the end of the 1.5 second delay, bistable latch E5 is triggered. This latch sets the KC (key control) flip-flop, clears the PWR LOW flip-flop, and triggers the E1 one-shot (the 0-output of E2 provides a required high signal at one input of E1; this high precedes the E1 trigger signal by an appreciable amount of time). The 1-output of the LA flip-flop asserts the LA ENABLE L, IND1 and MS, IR DISABLE L signals. The E1 one-shot, when it times out after 250 ns, triggers one-shot E4, which is active for 100 ns. During the 100 ns period, NAND gate E6 is, enabled and PULSE LA is asserted. Thus, the CPMA Register is loaded and the FETCH flip-flop is set. The E1 one-shot is retriggered, coincidently with the trailing edge of the PULSE LA signal; while the KC flip-flop is cleared, via NOR gate E6C, to assert the KEY CONTROL L signal. When E1 times out the second time, PULSE LA is produced again. Thus, the IF and DF Registers are loaded at this time. As before, E1 is retriggered coincidently with the trailing edge of PULSE LA. At the end of PULSE LA, when E4 times out for the second time, the LA flip-flop is cleared, and LA ENABLE L, IND1, and MS, IR DISABLE L are negated.

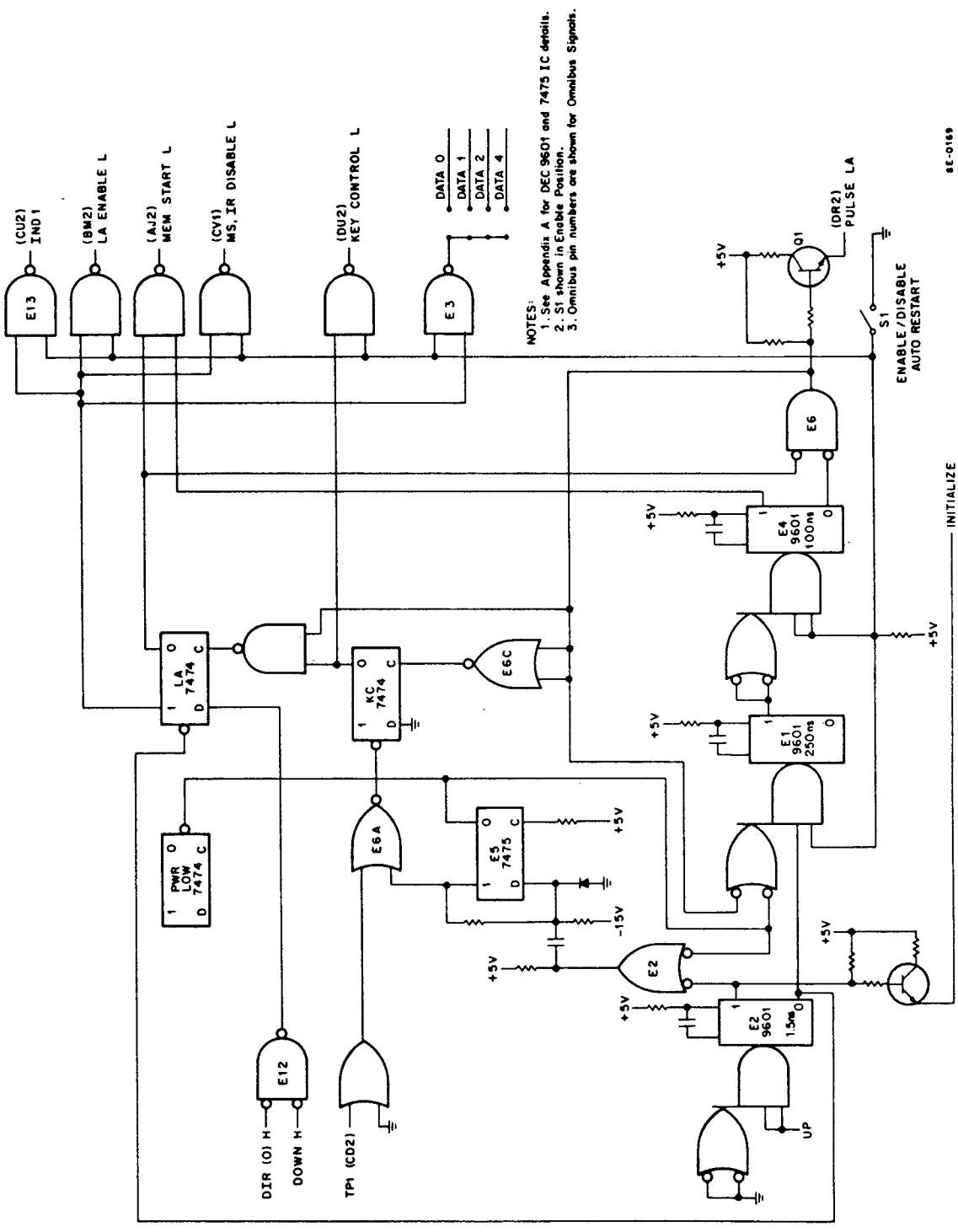


Figure 1-5 Auto-Restart Logic

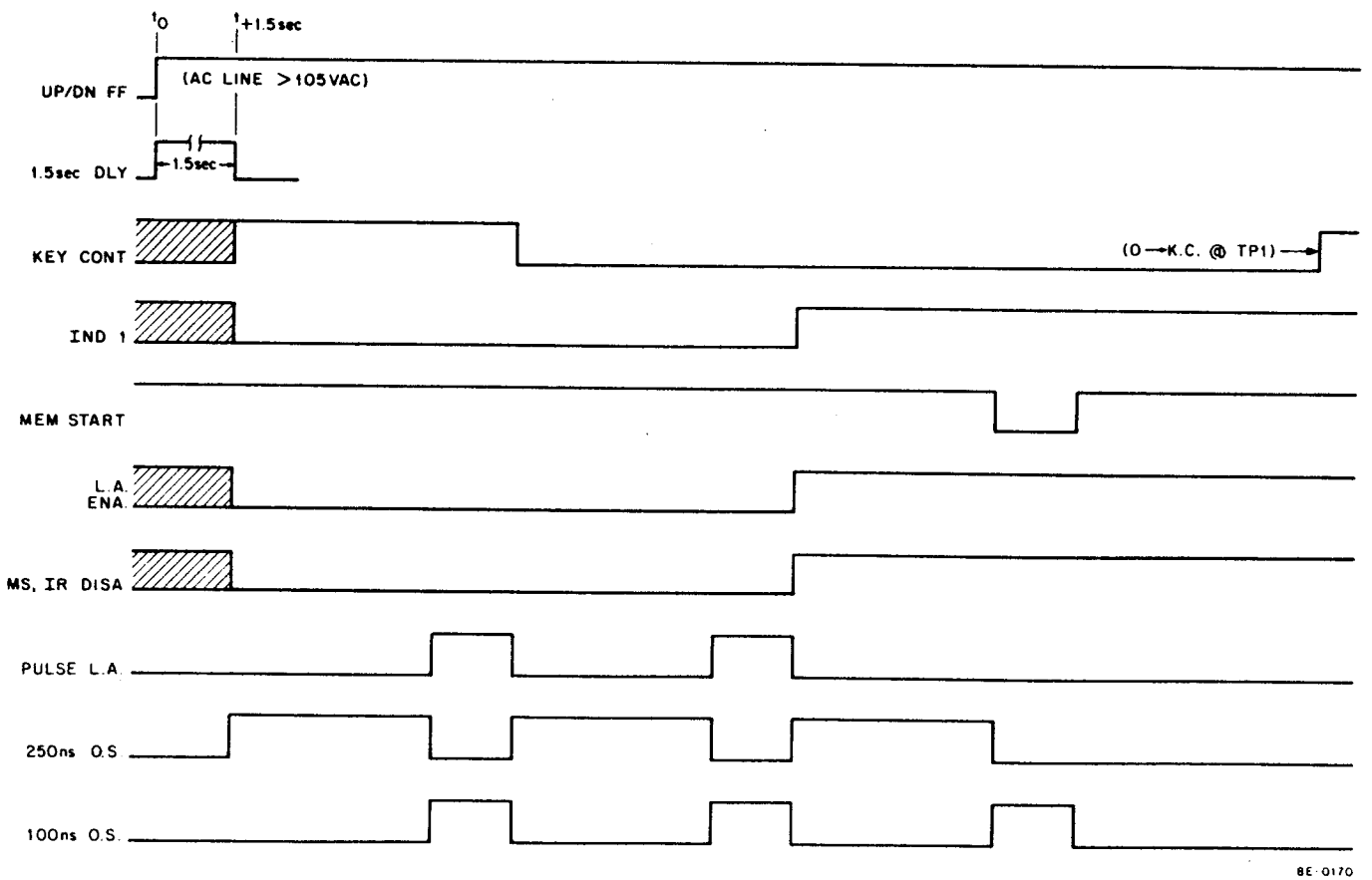


Figure 1-6 Auto-Restart Timing

When E1 times out for the third time, it once again triggers E4. However, because the LA flip-flop is now clear, no PULSE LA signal is produced. Instead, the 1-output of E4 asserts MEM START L and CPU timing begins by fetching the instruction in the starting location. At TP1 time of this FETCH cycle, the KC flip-flop is set by NOR gate E6A and the KEY CONTROL L signal is negated.

The DIR (Direction) flip-flop ensures that a Restart Sequence is initiated only when ac voltage is rising, through the Restart threshold toward normal line Voltage Condition.

SECTION 4 MAINTENANCE

General instructions concerning preventive and corrective maintenance are given in Volume 1, Chapter 4. When corrective maintenance is required, the technician should use the maintenance program, MAINDEC-8E-DOKC-D (D), to determine the nature of the problem. The option schematic, drawing E-CS-M848-0-1, must be referred to for IC locations and pin numbers. Test points have been provided on the option to facilitate troubleshooting.

The threshold adjustment on the resistor network, which supplies the 10.3 Vdc reference, should not be adjusted during troubleshooting and maintenance operations.

SECTION 5 SPARE PARTS

Table 1-2 lists recommended spare parts for the KP8-E. These parts can be obtained from any local DEC office or from DEC, Maynard, Massachusetts.

Table 1-2
Recommended KP8-E Spare Parts

DEC Part Number	Description	Quantity
11-09991	Diode, AZ1-1/4M, 6.8V	1
11-00114	Diode, D664	1
11-00275	Diode, D672	1
15-04338	Transistor, 6531B	1
15-03409-01	Transistor, DEC 6534B	1
19-05547	IC DEC 7474	1
19-05575	IC DEC 7400	1
19-05576	IC DEC 7410	1
19-09004	IC DEC 7402	1
19-09050	IC DEC 7475	1
19-09373	IC DEC 9601	1
19-09486	IC DEC 384	1
19-09705	IC DEC 8881	1
19-09971	IC DEC 6380	1
19-09972	IC DEC 6314	1

PART 5
INTERPROCESSOR OPTIONS

CHAPTER 1
DB8-E INTERPROCESSOR BUFFER

SECTION 1 INTRODUCTION

The DB8-E Interprocessor Buffer is designed to plug directly into the PDP-8/E OMNIBUS. This option allows two PDP-8/E Computers to transfer data between themselves, one 12-bit word at a time, at a software-limited rate of 50 kHz. The DB8-E can also be used to transfer data to user-designed logic on single-ended data lines.

The basic DB8-E option has one M8326 Module and one BC08-R cable (up to 100-ft long). The DB8-EB has one M8326 Module, two BC08-R cables, and two 5409209 Module Adapters for connection to user-designed logic.

Device codes on the module are jumper-selected between 50 and 57, allowing a maximum of eight Interprocessor Buffers to be used in one PDP-8/E.

SECTION 2 INSTALLATION

The DB8-E Interprocessor Buffer is installed on site by DEC Field Service personnel. The customer should **not** attempt to unpack, inspect, install, checkout, or service the equipment.

1.1 INSTALLATION

To install the Interprocessor Buffer, remove power from PDP-8/E No. 1 and insert the M8326 Module into the OMNIBUS. Refer to Table 2-3, Volume 1, for information about recommended module priorities (the DB8-E is a non-memory option). Remove power from PDP-8/E No. 2 and insert the second M8326 Module into its OMNIBUS. Connect one of the BC08-R cables between J1 of the first and J2 of the second DB8-E Module. Connect the second BC08-R cable between J2 of the first DB8-E and J1 of the second DB8-E. This will connect the output of PDP-8/E No. 1 buffer to the input of PDP-8/E No. 2 module and the output of PDP-8/E No. 2 to the input of PDP-8/E No. 1. Table 1-1 shows the pin-to-pin connections of J1 and J2.

Table 1-1
Connection from J1 to J2

J1 Pin No.	Adapter Module Pins	J2 Pin No.	Adapter Module Pins
J1TT	A1	J2C	V2
J1RR	B1	J2E	U2
J1D	V1	J2SS	A2
J1F	U1	J2PP	B2
J1J	T1	J2MM	C2

(continued on next page)

Table 1-1 (Cont)
Connection from J1 to J2

J1 Pin No.	Adapter Module Pins	J2 Pin No.	Adapter Module Pins
J1L	S1	J2KK	D2
J1N	R1	J2HH	E2
J1R	T1	J2EE	F2
J1T	N1	J2CC	H2
J1V	M1	J2AA	J2
J1X	L1	J2Y	K2
J1Z	K1	J2W	L2
J1BB	J1	J2U	M2
J1DD	H1	J2S	N2

NOTE: All pins not listed are tied to ground.

1.2 ACCEPTANCE TEST

The acceptance test should be performed when the DB8-E Modules are installed and periodically after installation to check the operation of the DB8-E logic. A working M8326 Test Module is needed to perform this test. The programs in Section 5 can be used for preliminary operational checks.

Perform the following steps to check the DB8-E Modules installed in the PDP-8/E OMNIBUS.

NOTE
The PDP-8/E under test will be referred to as PDP-8/E No. 1; the PDP-8/E with test module used to check the DB8-E Module in PDP-8/E No. 1 will be referred to as PDP-8/E No. 2.

Step	Procedure
1	Remove the DB8-E Module from PDP-8/E No. 2 and install the test module in its place; connect the cables from the DB8-E Module to the test module.
2	Load binary loader in PDP-8/E No. 1 and No. 2.
3	Load diagnostic MAINDEC-8E-DOPA-PB in PDP-8/E No. 1 and No. 2.
4	Run Part 1 and Part 2 of the test for 5 minutes each. There should be no errors.
5	If there are no errors, remove the test module from PDP-8/E No. 2 and reinstall the DB8-E Module.
6	To check the DB8-E Module in PDP-8/E No. 2, repeat Steps 1 through 5 with test module in PDP-8/E No. 1.

SECTION 3 SYSTEM DESCRIPTION

The Interprocessor Buffer (Figure 1-1) receives or transmits data under control of programmed instructions from the CPU. Data can be put on the DATA BUS of the OMNIBUS to be transferred to the accumulator, or data can be taken from the DATA BUS and transferred to another PDP-8/E or user's equipment.

The following instructions are used to program interprocessor data transfers.

Skip on Receive Flag (DBRF)

Octal Code: 65X1
Operation: Skip if the RECEIVE FLAG equals one.

Read Incoming Data (DBRD)

Octal Code: 65X2
Operation: Read the incoming data into the AC, clear the RECEIVE FLAG, and set the remote PDP-8/E's DONE FLAG.

Skip on Transmit Flag (DBTF)

Octal Code: 65X3
Operation: Skip if the DONE FLAG equals one.

Transmit Data (DBTD)

Octal Code: 65X4
Operation: Transfer the contents of the AC Register to the transmit buffer. Transmit data and set the remote PDP-8/E's DONE FLAG.

Enable Interrupt (DBEI)

Octal Code: 65X5
Operation: Enable the interrupt request line.

Disable Interrupt (DBDI)

Octal Code: 65X6
Operation: Disable the interrupt line.

Clear Done Flag (DBCD)

Octal Code: 65X7
Operation: Clear the DONE FLAG.

To transfer data from PDP-8/E No. 1 to PDP-8/E No. 2, data is loaded into the AC of PDP-8/E No. 1 and transferred to the output buffer of its DB8-E using the 65X4 IOT. In addition to loading the output buffer, IOT 65X4 also sets the RECEIVE FLAG flip-flop in PDP-8/E No. 2. When the program in PDP-8/E No. 2 has sensed its RECEIVE FLAG flip-flop, data is gated into the AC of PDP-8/E No. 2 using IOT 65X2. IOT 65X2 then sets the DONE flip-flop of PDP-8/E No. 1, indicating the transfer was completed, and clears the RECEIVE FLAG flip-flop of PDP-8/E No. 2. PDP-8/E No. 1 then clears its DONE FLAG using IOT 6507.

SECTION 4 DETAILED LOGIC

The logic in the Interprocessor Buffer will be broken into functional groups for discussion purposes. Figure 1-1 should be used to understand the relationship between each group of logic.

1.3 DEVICE SELECT LOGIC

The device select logic is shown in Figure 1-2. Bits MD03 through MD11 are gated by I/O PAUSE when a 65XX instruction is decoded. An INT I/O L and SELECT L will be asserted to allow the operation decoder to receive its input and to cause the positive I/O bus interface to ignore the IOT instruction.

1.4 OPERATION SELECT LOGIC

SELECT L in Figure 1-3 will enable the gates for bits MD09 through MD11 and allow inputs to the operation decoder which is a BCD-to-decimal decoder. (Refer to Appendix A, Volume 1, for details about the 8251 IC.) The decoder will supply signals that represent instructions 65X1 through 65X7. When a 65X2 instruction is decoded, the C line select logic will pull C0 and C1 low to allow data to be transferred from the DATA BUS to the AC.

1.5 INTERRUPT AND SKIP LOGIC

The interrupt and skip logic is used to interrupt the program when a data transfer is required. To allow an interrupt to occur, the INT ENA flip-flop must be set (Figure 1-4) by a 65X5 instruction. The 1-output of the INT ENA flip-flop will go to E17 and assert one side of the AND gates allowing them to generate INT RQST L. A more detailed explanation of interrupt and skip logic can be found in Volume 1.

Table 1-2 shows the signal and data flow required to transfer information between two PDP-8/E Computers.

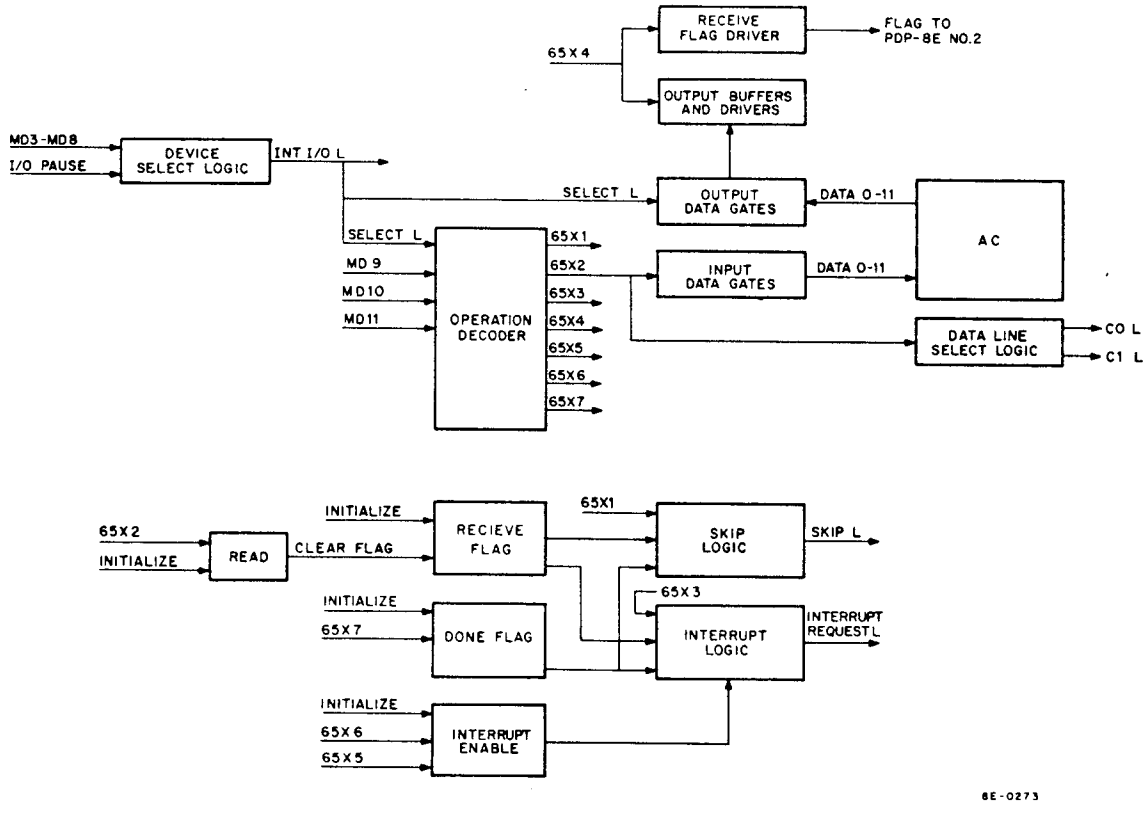


Figure 1-1 Interprocessor Buffer, Block Diagram

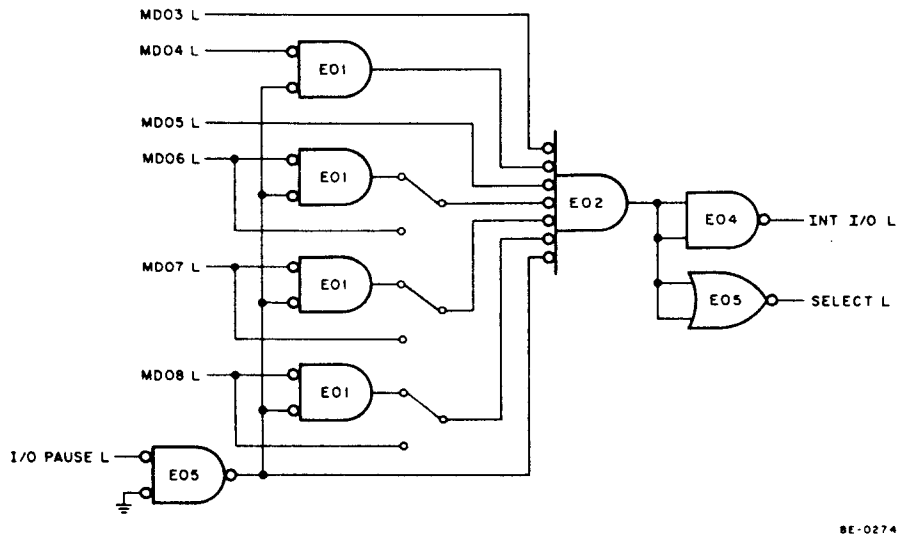


Figure 1-2 Device Select Logic

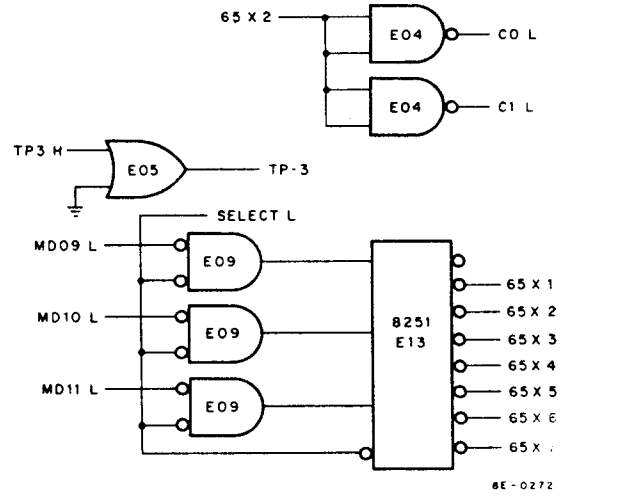


Figure 1-3 Operation Select Logic

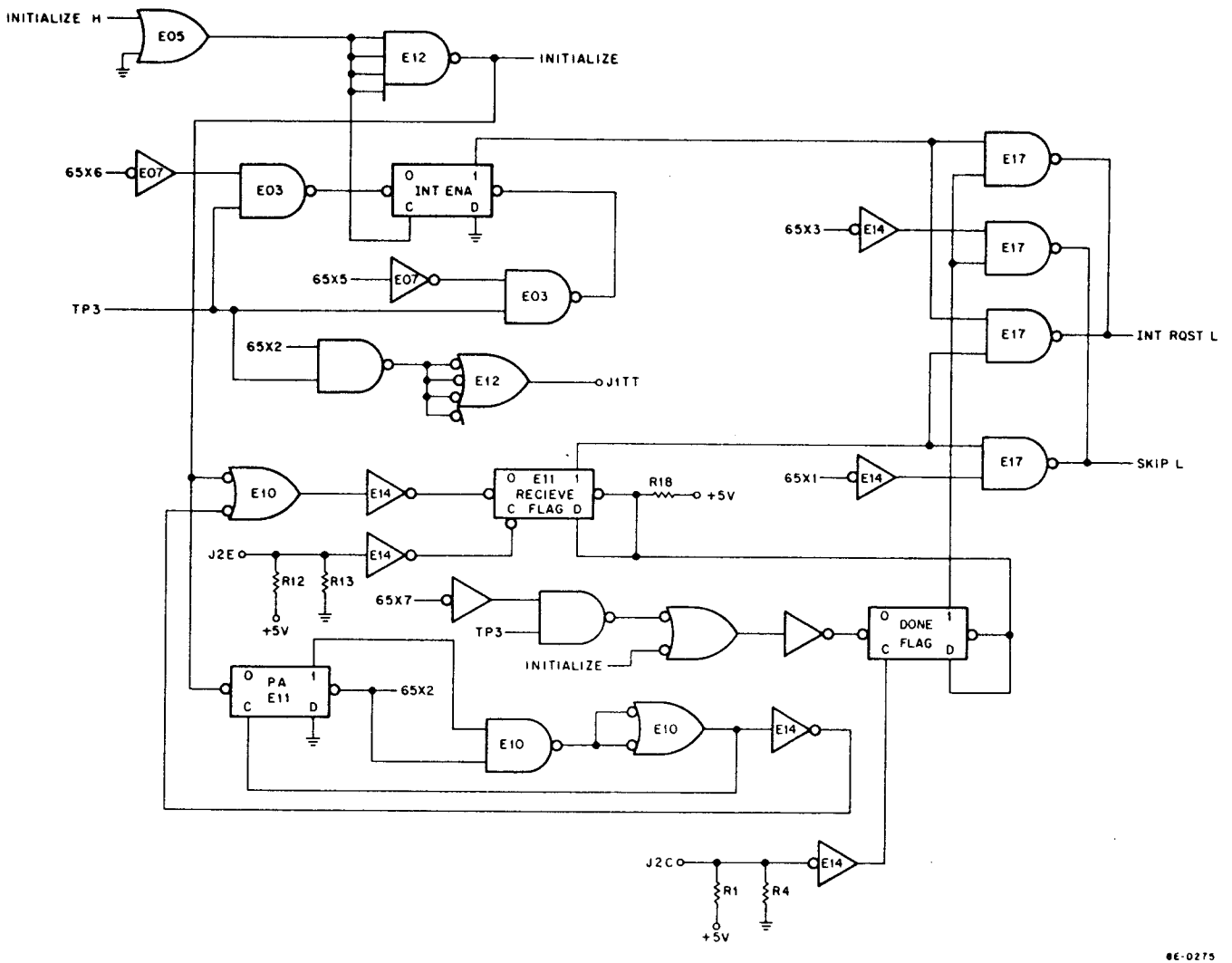


Figure 1-4 Interrupt and Skip Logic

1.6 INPUT DATA GATES AND OUTPUT BUFFERS

The input data gates (Figure 8-5) will be enabled by a 65X2 instruction and transfer data to the AC via the DATA BUS.

Table 1-2
Simultaneous Receive and Transmit Operation by Two PDP-8/E Computers Using Interprocessor Buffer

PDP-8/E No. 1 Data Transmitter	PDP-8/E No. 2 Data Receiver
Data is transferred from AC to the DATA BUS and applied to the data inputs of buffer flip-flops by programmed instructions.	
A 6504 instruction clocks the buffer flip-flops and transmits information to PDP-8/E No. 2 and simultaneously sends a signal from J1RR of PDP-8/E No. 1 to J2E of PDP-8/E No. 2.	Data is received and RECEIVE FLAG is set by signal at J2E. INT RQST if ENA is set, and SKIP generated, and subroutine to read data is started.
The trailing edge of the signal at J2C sets the DONE FLAG to indicate PDP-8/E No. 2 has read data.	6502 instruction gates data to DATA BUS. TP3 and 6502 instruction enable signal to J1TT to be transmitted to J2C of PDP-8/E No. 1.
Signal is removed from J2C when 6502 signal is removed from gate in PDP-8/E No. 2.	The RECEIVE Flag is cleared by trailing edge of 6502 instruction.
The DONE FLAG is cleared by 6507 instruction.	
PDP-8/E No. 1 is ready to transmit or receive data.	PDP-8/E No. 2 is ready to receive or transmit data.

The SELECT L signal applied to the output data gates will allow 1s to be transferred from the DATA BUS to the data input side of flip-flops in the output buffer. When a 65X4 instruction is generated, the clock input of the flip-flop will be pulsed and the data will be transferred to the input gates of PDP-8/E No. 2. This instruction will also cause J1 RR to go high and set the RECEIVE FLAG in PDP-8/E No. 2. The data transferred from the Interprocessor Buffer is +3V for true (1) signals and 0.0V for false (0) signals.

SECTION 5 MAINTENANCE

Refer to Volume 1 for maintenance information about PDP-8/E Computers. The acceptance test given in Section 2 should be performed when an error is suspected in the DB8-E.

1.7 DATA TRANSFER TEST

Perform the following programs to transfer data from the switch register of PDP-8/E No. 1 to the AC of PDP-8/E No. 2.

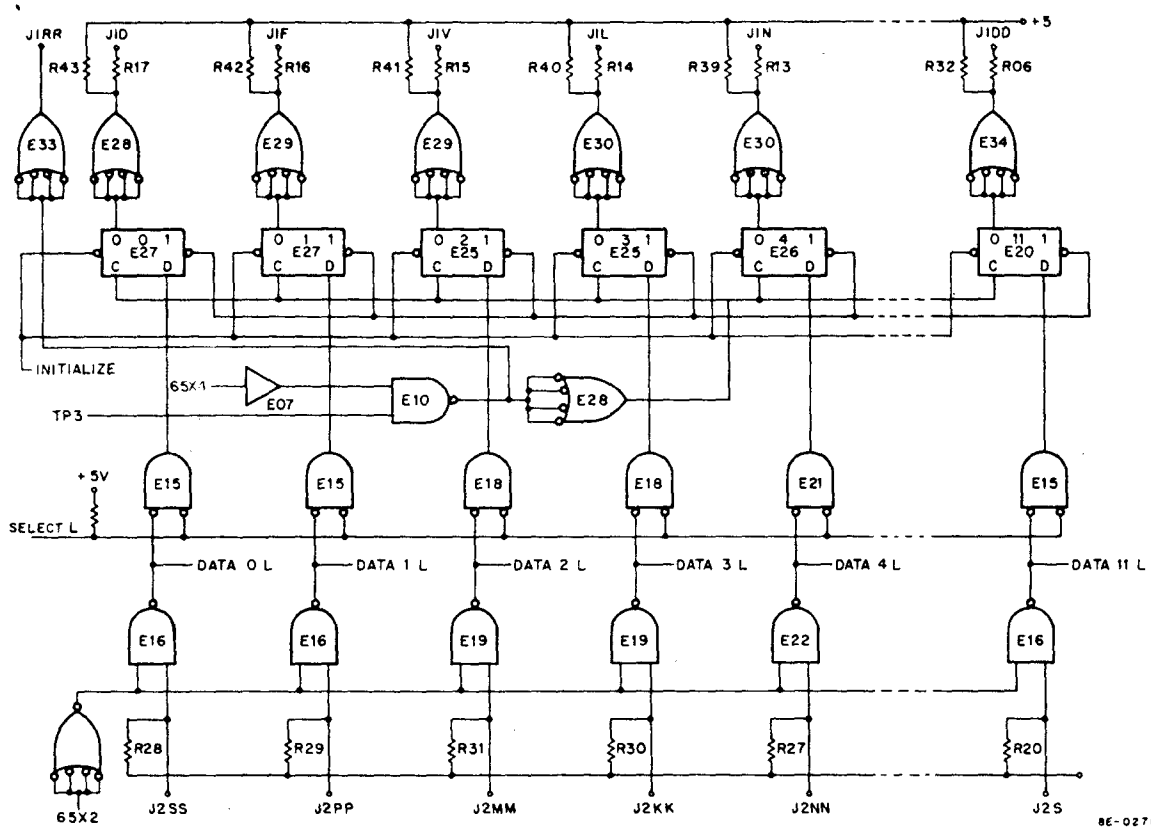


Figure 1-5 Input Data Gates and Output Data Gates and Drivers

PDP-8/E No. 1		PDP-8/E No. 2	
Address	**Contents**	**Address**	**Contents**
200	7604	200	6501
201	6504	201	5200
202	6503	202	6502
203	5202	203	5200
204	6507		
205	5200		

After the programs are loaded, load address 200 and start both PDP-8/Es. The AC lights of PDP-8/E No. 2 will display contents of SR on PDP-8/E No. 1. It is recommended that the following be tried.

a. All 1s
b. All 0s
c. A single 1 in each bit position
d. A single 0 in each bit position.

SECTION 6 SPARE PARTS

Table 1-3 lists recommended spare parts for the DB8-E. These spare parts can be obtained from any local DEC office or from DEC, Maynard, Massachusetts.

Table 1-3
DB8-E Recommended Spare Parts

DEC Part No.	Description	Quantity
19-05547	IC DEC 7474	1
19-05575	IC DEC 7400	1
19-05579	IC DEC 7440	1
19-09486	IC DEC 384	1
19-09594	IC DEC 8251	1
19-09686	IC DEC 7404	1
19-09973	IC DEC 97401	1
19-09971	IC DEC 6380	1
19-09972	IC DEC 6314	1

PART 6
EXTERNAL BUS INTERFACE CONTROL OPTIONS

CHAPTER 1
KA8-E POSITIVE I/O BUS INTERFACE

SECTION 1 INTRODUCTION

The KA8-E Positive I/O Bus Interface permits use of a PDP-8/I or PDP-8/L type peripheral with the PDP-8/E. If the peripheral is a data break device, a KD8-E data break interface must also be in the system. The concept of data transfers and the interrelationship of the KA8-E Positive I/O Bus Interface, the KD8-E Data Break Interface, and the OMNIBUS are explained in Chapters 6 and 10 of the *PDP-8/E & PDP-8/M Small Computer Handbook.* A detailed discussion of CPU operation during a programmed I/O transfer is presented in Volume 1, Chapter 3, Section 6. The reader should be thoroughly familiar with this referenced information to benefit from the detailed logic discussion presented in this chapter.

SECTION 2 BLOCK DIAGRAM

Figure 1-1 is a functional block diagram of the Positive I/O Bus Interface. When an IOT instruction is placed on the OMNIBUS MD lines, the I/O PAUSE L signal is asserted by the CPU timing generator. If INTERNAL I/O L is not asserted by an internal peripheral, I/O PAUSE L causes the interface IOP timing to assert the NOT LAST TRANSFER L signal. Thus, CPU timing is suspended at TP3 time. Simultaneously, IOP timing is initiated and the IOP signal that is subsequently generated enables the BIOP pulse generator to produce one or more pulses. These pulses are used by the peripheral in conjunction with BMB bits to decode IOT instructions.

The IOT instruction can clear and set flags and registers within the peripheral, or it can direct a data word transfer or a SKIP operation. Data words are transferred between the data gating logic and the CPU via the DATA0-11 lines; between the peripheral and data gating, the data path depends on the direction of transfer, as shown in the block diagram. The OMNIBUS C lines are asserted within the data gating logic in combinations that depend on the type and direction of transfer.

If a SKIP operation is directed by the IOT instruction, the peripheral asserts the external SKIP L signal when conditions warrant. IOP timing clocks the skip counter and either the DATA10 or DATA11 line, or both, is activated.

SECTION 3 DETAILED LOGIC

1.1 BIOP PULSE GENERATOR LOGIC

Figure 1-2 shows the BIOP pulse generator logic, which converts bits MD9—11 to BIOP pulses 4, 2, and 1, respectively. A logic 1 on any MD line conditions a corresponding NAND gate for enabling at TP2 time. When the NAND gate is enabled, it dc-sets a flip-flop that, in turn, conditions another NAND gate. Simultaneously, the

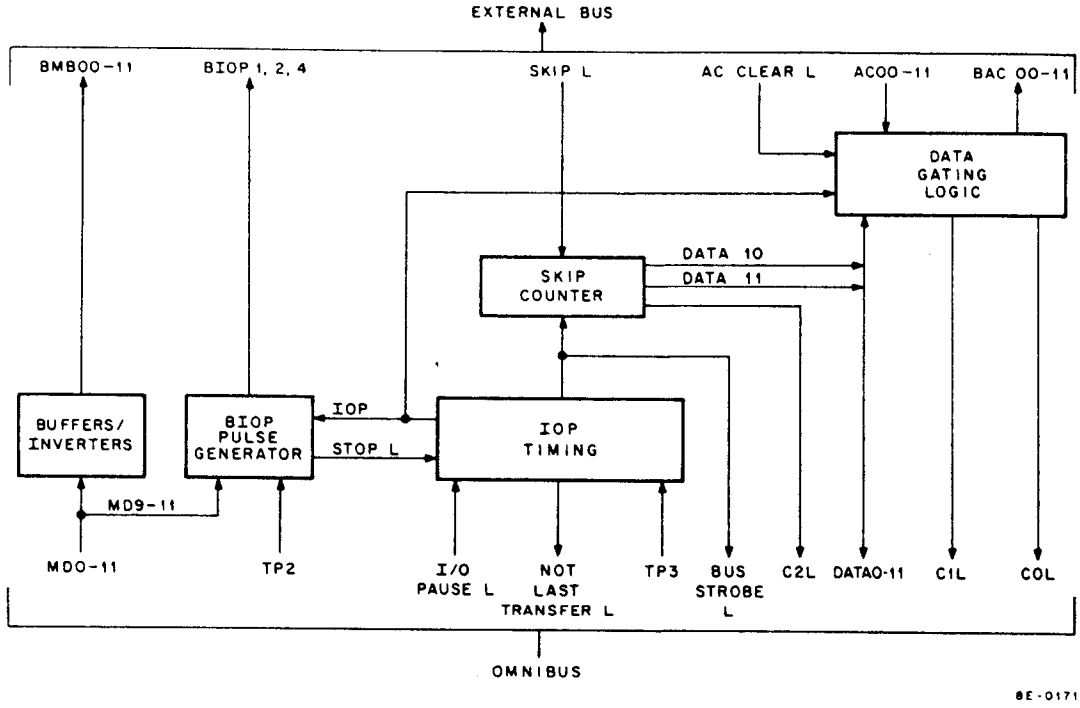


Figure 1-1 Positive I/O Bus Interface, Block Diagram

flip-flop causes the STOP L signal to be negated. If an I/O transfer involving an external bus peripheral is in progress, the STOP L signal enables TP3 to initiate the IOP timing operation. The IOP timing logic (Paragraph 1.3) responds by asserting a signal (IOP) that enables the flip-flop conditioned NAND gate. The resulting signal is buffered and designated BIOP4, BIOP2, or BIOP1.

For example, if MD bit 9 is a logic 1, flip-flop IO4 is dc-set at TP2 time (note that the IO flip-flops are cleared at each TP1 time). The 0-output of the flip-flop causes STOP L to be asserted and, providing the IO1 and IO2 flip-flops are cleared (MD bits 10 and 11 are logic 0), the 1-output conditions NAND gate E24 for enabling by the IOP signal. When the IOP timing asserts the IOP signal, E24 is enabled and the BIOP4 pulse is generated. The width of the pulse can be varied by adjusting a potentiometer in the IOP timing logic, thereby asserting the IOP signal for the desired amount of time (Paragraph 1.3). When the IOP signal is negated, E24 is disabled. Because the output of E24 is connected to the clock input of IO4, the flip-flop is cleared when E24 is disabled (note that the D inputs of the IO flip-flops are connected to ground; thus, a positive transition at a clock input clears the flip-flop). The 0-output of IO4 negates the STOP L signal; this action causes the IOP timing logic to terminate the I/O dialogue.

This example stipulated that bits MD10 and MD11 were logic 0. Suppose, instead, that all three MD bits are logic 1. All three IO flip-flops are then set at TP2. The STOP L signal is asserted and the 1-output of IO1 conditions E11C for enabling by the IOP signal. Observe that the 0-output of IO1 disables both NAND gate E8B and NAND gate E24. Thus, the IOP signal enables E11C first and the BIOP1 pulse is generated. When the IOP signal is negated, E11C is disabled and IO1 is cleared. This action removes the disabling signal from E8B; however, E24 remains disabled because the 0-output of IO2 is one of its inputs. NAND gate E8B is now conditioned for enabling by the IOP signal. When this signal is again asserted by the IOP timing logic, BIOP2 is generated. When BIOP2 ends, IO2 is cleared, removing the disabling signal from E24. Now the BIOP4 pulse is generated, as detailed earlier.

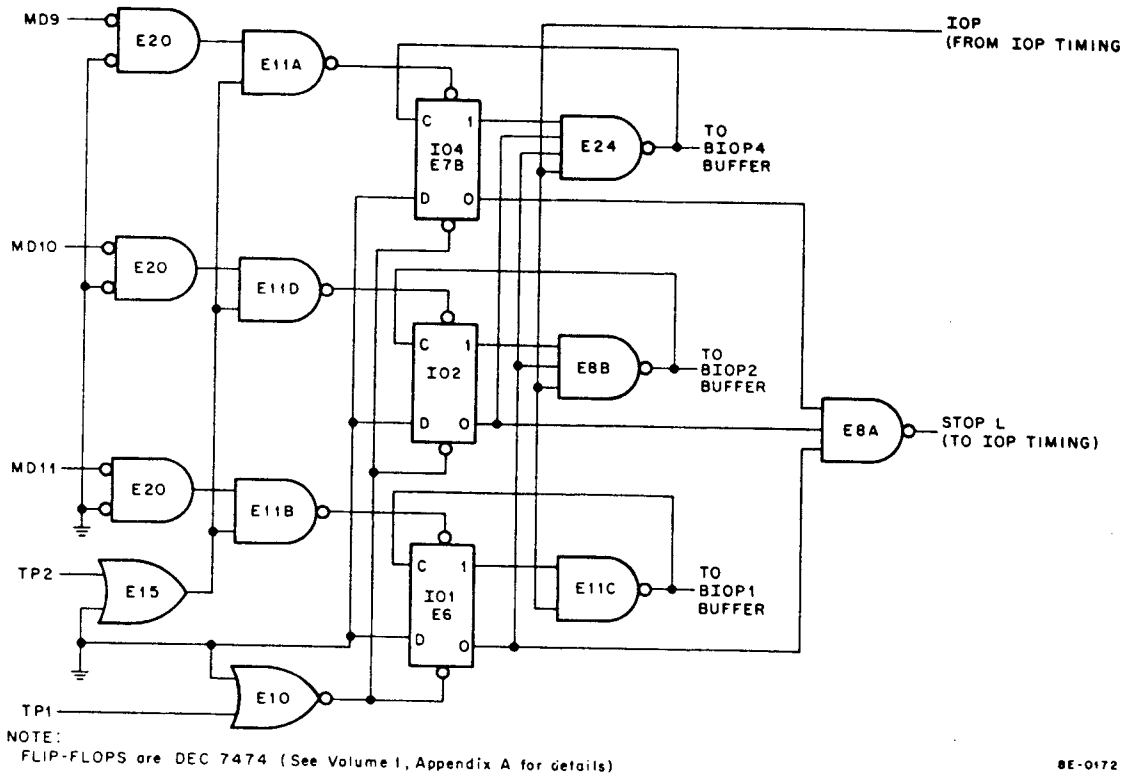


Figure 1-2 BIOP Pulse Generator Logic

Thus, the BIOP Pulse Generator logic operates in such a way that the BIOP pulses are not assigned specific time slots. If only one of the MD bits is a logic 1, then the corresponding BIOP pulse, whether 4, 2, or 1, is generated at the first assertion of the IOP signal. If more than one MD bit is logic 1, the least-significant bit is selected first and its corresponding BIOP pulse is generated; the most-significant bit is selected last.

1.2 BMB BUFFERS/INVERTERS

The preceding paragraphs discussed the BIOP pulse generator. A peripheral uses these BIOP pulses in conjunction with BMB bits to decode IOT instructions. The BMB bits are derived from the OMNIBUS MD bits, which are buffered and inverted by the interface. Figure 1-3 shows the buffer/inverter and network.

BMB bits 03–08 are used in peripheral device selection logic. Both the true and the false states of these bits are derived from the corresponding MD bit; this minimizes the device selection network in the external peripheral. Although programmed transfer peripherals use the BMB bits only for device selection, data break peripherals receive output (from the CPU) data via the BMB00–11 lines. Thus, all 12 BMB bits are derived, as shown in Figure 1-3.

1.3 IOP TIMING LOGIC

Figure 1-4 shows the IOP timing logic, which determines the duration of BIOP pulses and the separation between individual pulses, if more than one is programmed. Separation and duration can be varied individually by potentiometers that are indicated on the logic diagram and on the KA8-E etch as IOP SEP and IOP WIDTH. These

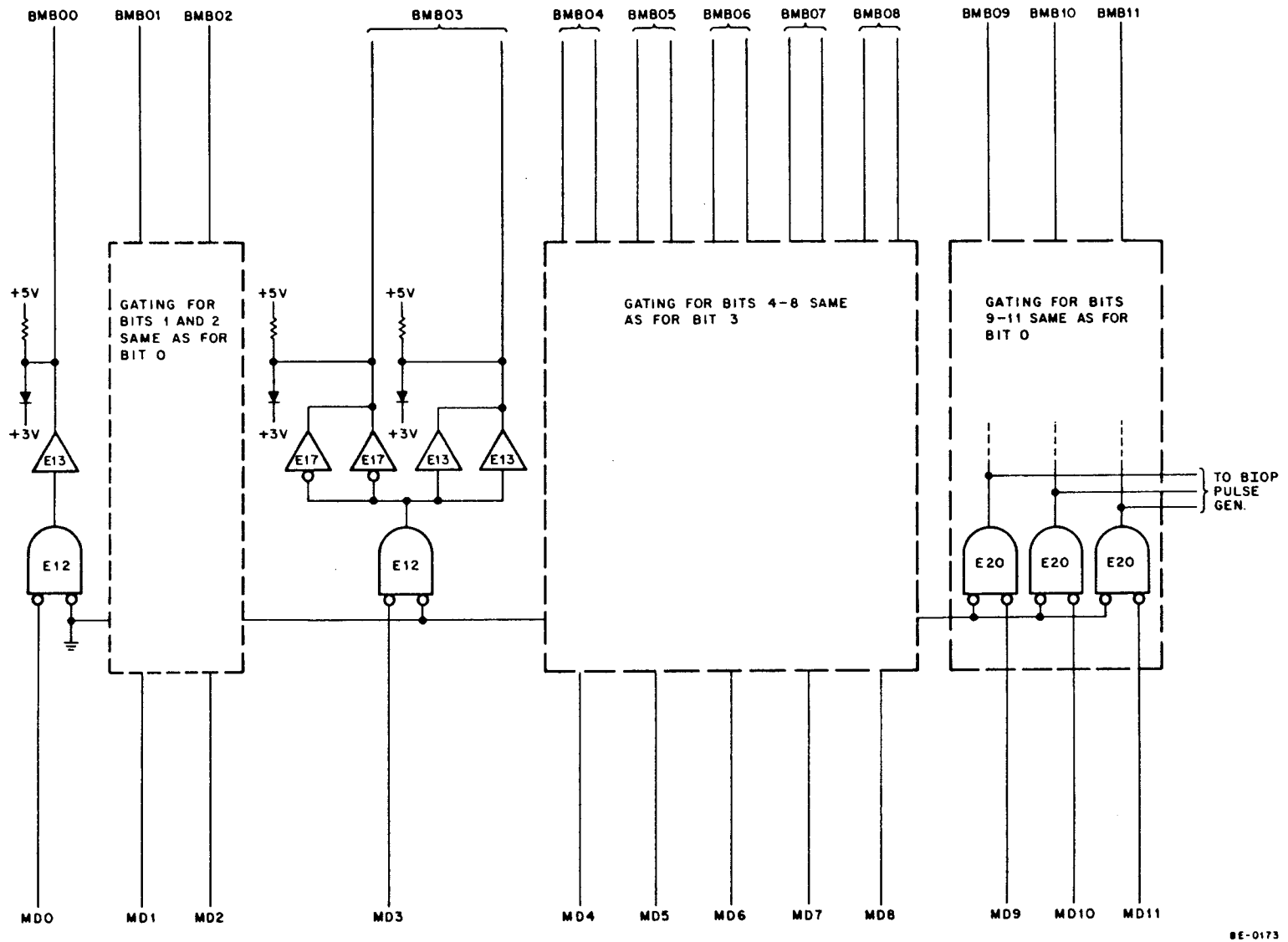


Figure 1-3 BMB Buffers/Inverters

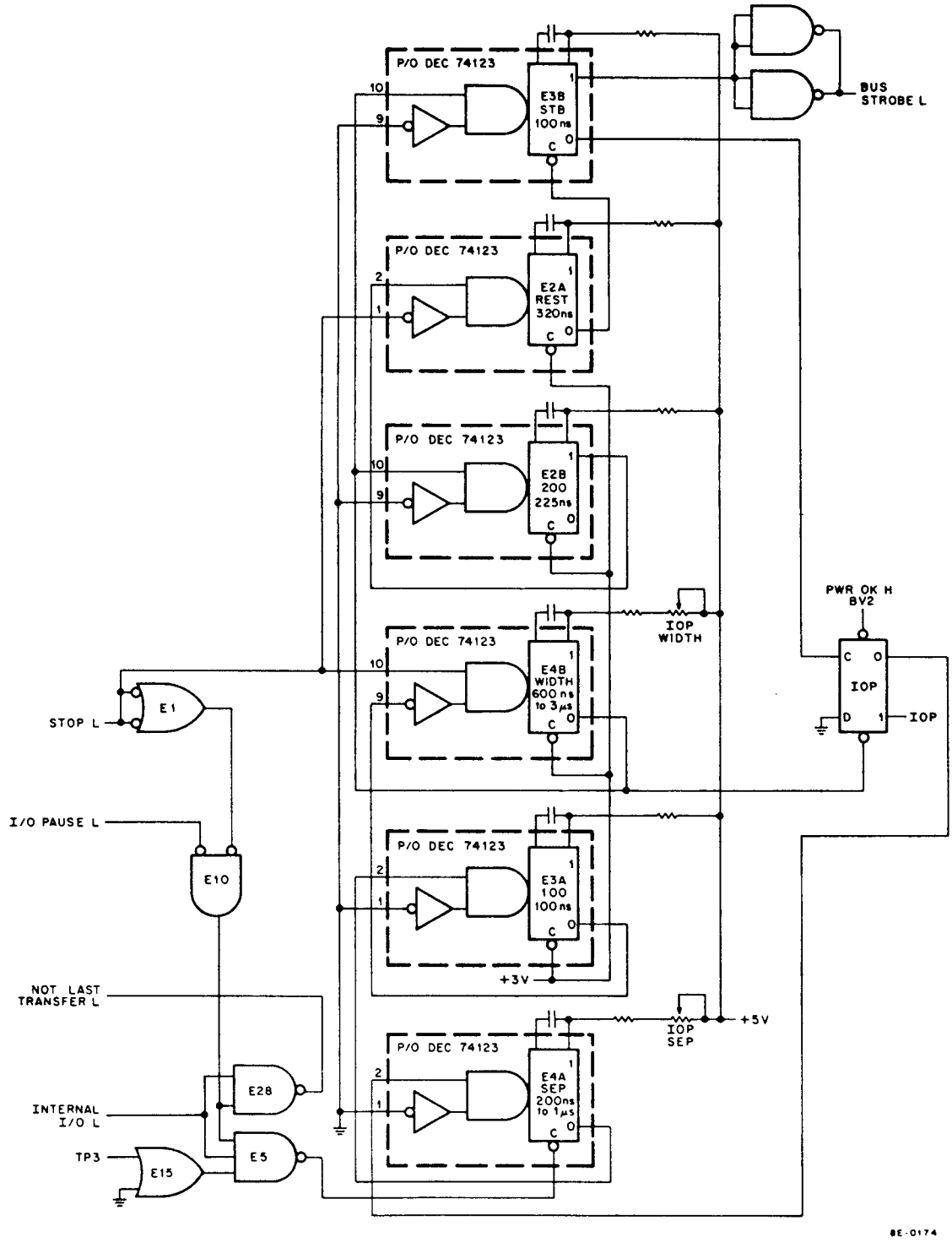


Figure 1-4 IOP Timing Logic

potentiometers determine the triggered delay time of associated one-shot multivibrators, shown as part of DEC 74123 ICs. Briefly, the one-shots contained within a 74123 can be triggered by:

a. a positive transition at pin 2, if, prior to the transition, pin 1 is low and the clear (C) input is high (for the "B" half of the IC, substitute pin 10 and pin 9 for pin 2 and pin 1, respectively),

b. a negative transition at pin 1, if, prior to the transition, pin 2 is high and C is high,

c. a positive transition at the C input, if, prior to the transition, pin 1 is low and pin 2 is high.

Figure 1-5 shows the IOP timing for a typical I/O transfer. The IOP signal is asserted three times during the time that I/O PAUSE is active; thus, three BIOP pulses are generated by the BIOP pulse generator (the identity of the BIOP pulses does not affect the waveform relationship). The waveforms representing SEP and WIDTH are shown for the minimum allowable triggered delay time, viz., 200 ns for SEP and 600 ns for WIDTH. The potentiometer values allow these delay times to be increased to five times the minimum value. Refer to both figures while studying the following description.

If the I/O transfer involves an external bus peripheral (INTERNAL I/O L remains negated) and the BIOP pulse generator negates the STOP L signal, and NAND gate E28 asserts the NOT LAST TRANSFER L signal; this signal indicates to the CPU timing generator the impending interruption of normal timing. At TP3 time, IOP timing is initiated, while CPU timing is suspended in TS3.

IOP timing begins when the SEP one-shot is triggered by the positive transition at its C input (TP3 going away) SEP (0) is used to trigger the 100 one-shot, which, in turn, triggers WIDTH. WIDTH (0) sets the IOP flip-flop; the resulting IOP signal enables the BIOP pulse generator to begin the BIOP pulse. The STB (Strobe) one-shot, triggered by the end of WIDTH (0), clears the IOP flip-flop; thus, the duration of the BIOP pulse is 100 ns longer than the duration of WIDTH (0). A BUS STROBE L signal is generated by STB (1) at the end of each BIOP pulse to execute the instruction represented by the BIOP pulse (BUS STROBE L causes the AC LOAD L signal to be asserted in the CPU; see Volume 1, Chapter 3, Section 6 for details). When the first BIOP pulse has ended, the sequence outlined begins again, this time with STB (0) triggering the SEP one-shot. When the last BIOP pulse ends, the STOP L signal is asserted by the BIOP pulse generator. This signal ensures that the WIDTH one-shot is not triggered by the next transition of 100 (0). Therefore, the IOP flip-flop remains clear through the remainder of the IOP timing. When REST (0) (the Restart one-shot), which is triggered by the STOP L signal transition, goes positive after 320 ns, STB is triggered again, producing a final BUS STROBE L signal. This BUS STROBE terminates I/O dialogue and reinstates CPU timing.

The 100 one-shot is necessary for proper triggering of WIDTH. It provides a negative transition at pin 9 of WIDTH when SEP times out. If the negative transition were supplied by the 0-output of SEP, WIDTH would trigger at the same time as SEP. On the other hand, if the negative transition were supplied by the 1-output of SEP, WIDTH would trigger at TP2 time, when the STOP L signal is negated. Consequently, the 100 one-shot is quite important to the timing operation.

The purpose of the 225 one-shot is to allow the STOP L signal to fire the restart one-shot when the IOP register empties.

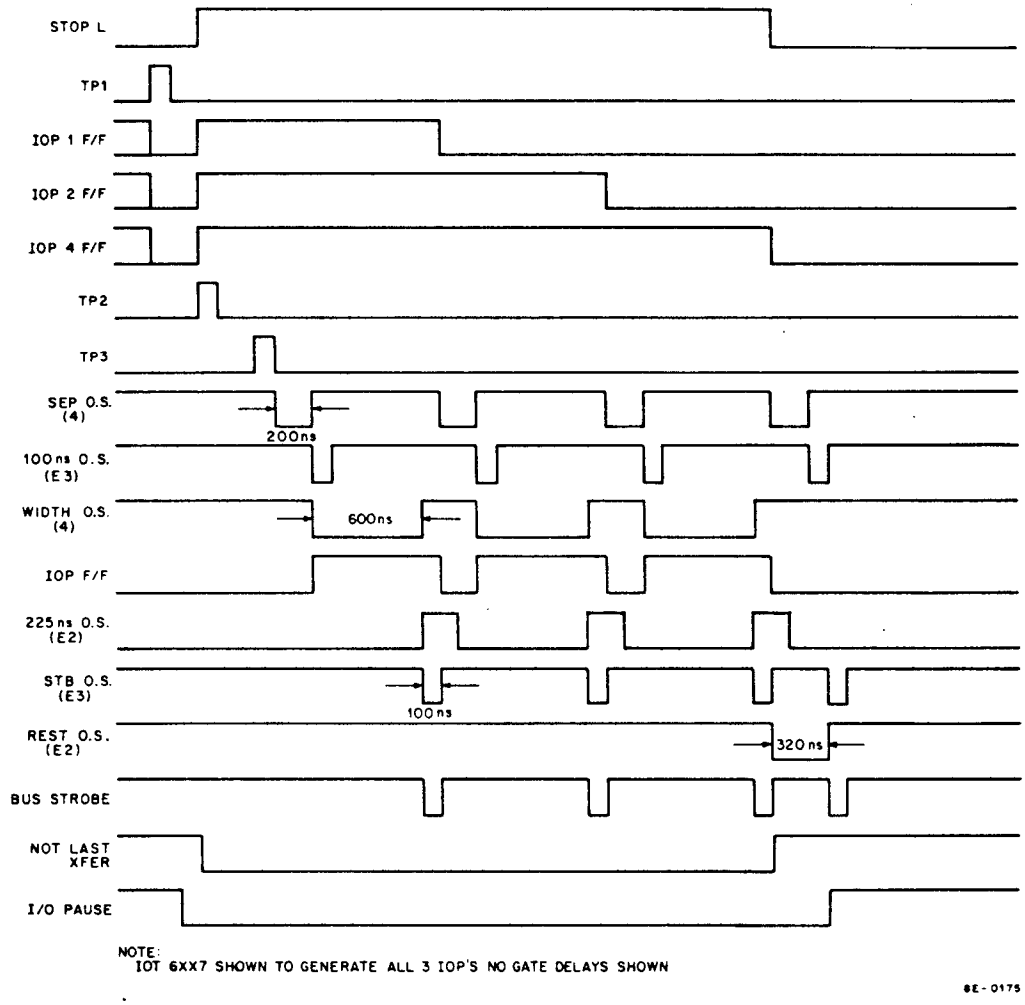


Figure 1-5 Waveforms, IOP Timing Logic

1.4 DATA GATING LOGIC

The data gating logic is shown in Figure 1-6. During a programmed I/O transfer, data is transferred to or from the CPU on the OMNIBUS DATA0–11 lines. Output data (from the CPU) is gated from the DATA lines through an interface buffer/inverter network (illustrated in Figure 1-6 for bits 0 and 11) to the external bus BAC00–11 lines. If the output transfer is to be accompanied by a clearing of the CPU AC Register, the peripheral is directed (by the BIOP pulse) to assert the OMNIBUS C0 L signal. The peripheral does this indirectly by grounding the external bus AC CLEAR line. The AC CLEAR L signal causes NAND gate E25D on the interface to assert the C0 L signal. If the AC Register does not have to be cleared, the C-lines remain negated high throughout the transfer.

On the other hand, an input transfer must always be accompanied by the assertion of at least one C-line. Note that when a data word is transferred from the peripheral on the external bus AC00–11 lines, the interface DATA IN L signal is asserted by NOR gate E29. If the data is placed on the AC lines during the BIOP pulse (as it must be), NAND gate E25C asserts the C1 L signal. Simultaneously, the AC INPUTS → DATA BUS signal gates the data onto the OMNIBUS DATA0–11 lines. The result of these actions is an OR operation of the AC contents and the data on the DATA0–11 lines. The peripheral can cause a jam input by grounding the AC CLEAR line, thereby asserting the C0 L signal. Thus, only the information on the DATA0–11 lines is placed in the AC Register. Note that if data word 0000_8 is transferred from the peripheral, the DATA IN L signal is not asserted. To transfer 0000_8, the peripheral must ground the AC CLEAR line and, in effect, cause a jam input of zeros.

These are the four types of data transfers that can be made by the PDP-8/I type peripherals. Another form of I/O transfer, other than a 12-bit data word, utilizes the interface skip logic to update the CPU PC Register. This type of transfer is discussed in Paragraph 1.5.

1.5 SKIP COUNTER LOGIC

The peripheral, when directed by an IOT instruction, can cause a skip of 1, 2, or 3 program instructions. It initiates a SKIP operation by grounding the external bus SKIP line. The interface skip logic, shown in Figure 1-7, asserts the OMNIBUS DATA10 and/or DATA11 lines, depending on the number of instruction skips required (during a SKIP operation the peripheral does not place data on the AC00–11 lines). At the same time, the OMNIBUS C lines are manipulated to provide a path for the DATA bits through the CPU major register gating to the PC Register. The DATA bits are added to the contents of the PC Register, increasing the program count in the register by 1, 2, or 3.

The timing diagram of a typical SKIP operation is shown in Figure 1-8. Refer to this diagram and to Figure 1-7 while studying the description that follows. The timing diagram shows that two BIOP pulses, 1 and 2, are generated during the IOT instruction. The imaginary peripheral that applies to this example decodes these two BIOP pulses and responds by grounding the SKIP line. Keep in mind that this is an example, only, and that this imaginary peripheral does not necessarily exist. The combination of BIOP1 and BIOP2 can produce a variety of operations, depending on how a peripheral decodes the pulses.

Nevertheless, when TP3 starts IOP timing, this peripheral is directed to initiate a SKIP operation by asserting SKIP L. The SKIP line controls the D-input of flip-flop E9, which is clocked when the STB one-shot is triggered. Because STB is triggered at the end of each BIOP pulse, E9 can be clocked twice during IOP timing. Note that the 100 one-shot dc-sets E9. Thus, E9 is set at the first triggering of the 100 one-shot, or (as shown in Figure 1-8) during a previous IOP timing cycle. Thereafter, 100 and STB are triggered alternately. Thus, E9 is alternately cleared and set, as long as SKIP L is asserted. Each time E9 is cleared, SKIP 1, the first stage of the 2-stage binary counter, is clocked. In this example, the binary counter is clocked twice, indicating that two instructions are to

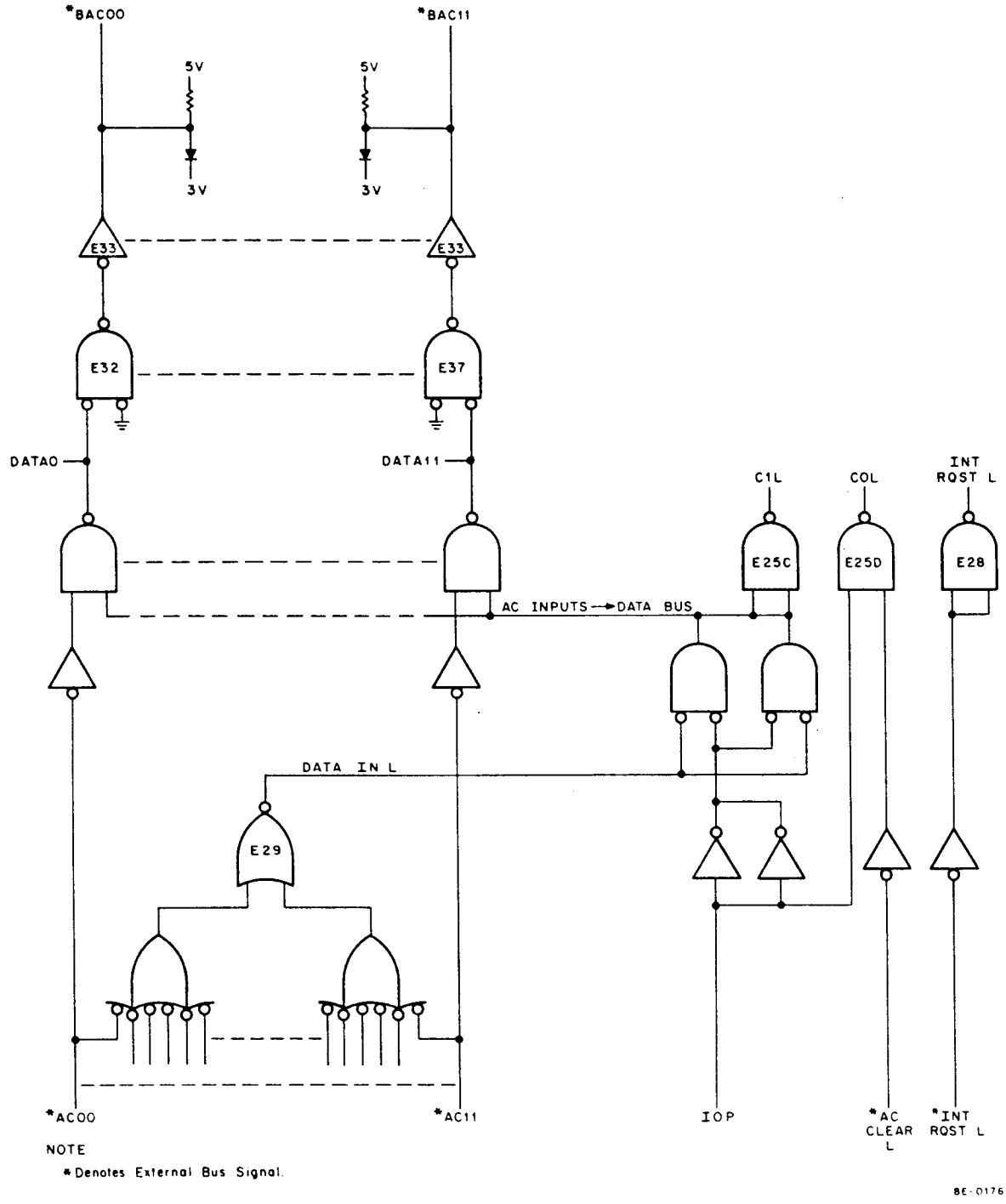


Figure 1-6 Data Gating Logic

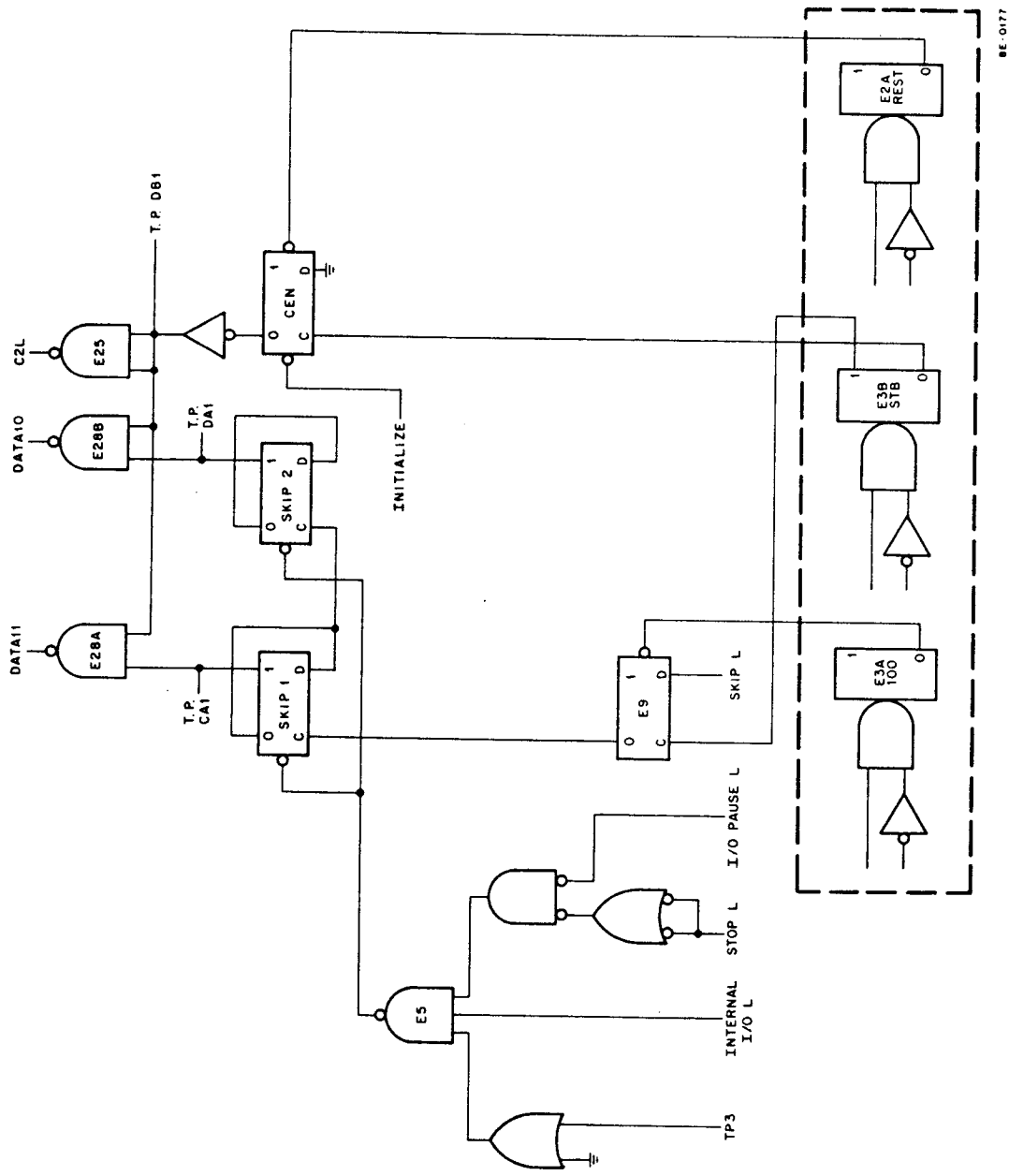


Figure 1-7 Skip Logic

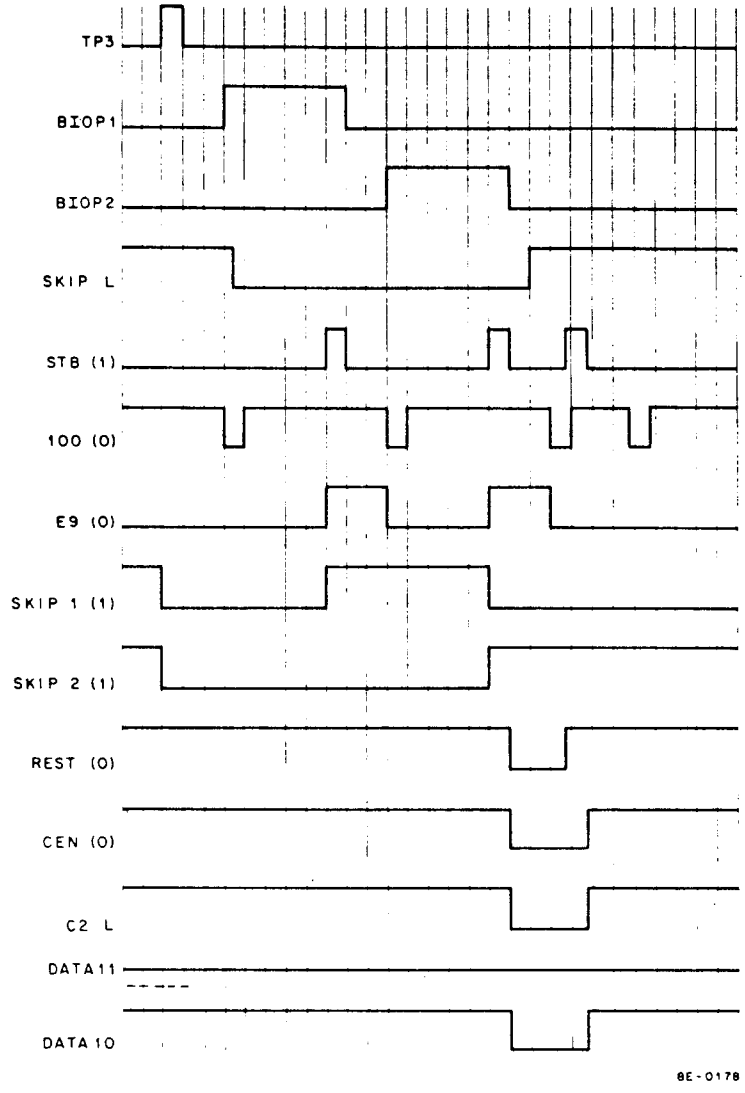


Figure 1-8 Timing, Skip Logic Application

to be skipped. SKIP 2 is set at the second triggering of STB. The C-line enable (CEN) flip-flop is dc-set by the REST one-shot, enabling NAND gates E25 and E28B (note that CEN is clocked by STB at the same time that it is dc-set by REST; the dc-input takes precedence in such a case). The assertion of C2 L, while C1 L and C0 L remain negated, provides a path for DATA10 through major register gating to the PC Register. C2 L and BUS STROBE (generated when REST times out) assert PC LOAD L and DATA10 is added to the contents of the PC Register, updating it by two. Note that the SKIP line must be negated before STB is triggered by the trailing edge of REST (0). If not, the binary counter is erroneously clocked one more time.

SECTION 4 MAINTENANCE

There are no specific maintenance procedures for the KA8-E itself. Each DEC peripheral that connects to the KA8-E has an associated MAINDEC or exerciser program that enables the technician to maintain both the option and the KA8-E interface. Because all of these peripherals use the one interface, a fault in the interface can be isolated by running a number of MAINDEC programs. If all programs result in errors, one can reasonably conclude that the KA8-E is at fault.

General information concerning corrective maintenance is included in Volume 1, Chapter 4. The technician will find this material helpful. The interface schematic, E-CS-M8350, indicates important test points, IC locations, and pin numbers and should be used whenever maintenance is being performed.

The KA8-E connects directly to a single peripheral via three cables that are supplied with the interface (refer to the *PDP-8/E & PDP-8/M Small Computer Handbook*, Chapter 10, for cabling rules and suggestions). Each cable connects to the interface with a 40-pin Berg connector and to the peripheral with a DEC M953A cable connector. From-To information for the cable is given in Table 1-1 (the cables are identical). (Refer to the *PDP-8/E & PDP-8/M Small Computer Handbook* for details concerning cable connections.)

Table 1-1
KA8-E Cable Information

From (M953A Cable Conn.)	To (Berg Conn.)	From (M953A Cable Conn.)	To (Berg Conn.)
Gnd	A	Gnd	Y
Gnd	B	M2	Z
Gnd	C	Gnd	AA
B1	D	L1	BB
Gnd	E	Gnd	CC
D2	F	P2	DD
Gnd	H	Gnd	EE
D1	J	M1	FF
Gnd	K	Gnd	HH
E2	L	S2	JJ
Gnd	M	Gnd	KK
E1	N	P1	LL
Gnd	P	Gnd	MM
H2	R	T2	NN
Gnd	S	Gnd	PP
H1	T	S1	RR
Gnd	U	Gnd	SS
K2	V	V2	TT
Gnd	W	Gnd	UU
J1	X	Gnd	VV

Pins A2, B2, U1, and V1 on M953A not used.
Pins A1, C1, F1, K1, N1, R1, T1, C2, F2, J2, L2, N2, R2, and U2 on M953A are ground pins.

SECTION 5 SPARE PARTS

Table 1-2 lists recommended spare parts for the KA8-E. These spare parts can be obtained from any local DEC office or from DEC, Maynard, Massachusetts.

Table 1-2
KA8-E Recommended Spare Parts

DEC Part No.	Description	Quantity
15-03100	Transistor, DEC 3009B	1
19-09705	IC DEC 8881	1
19-10010	IC DEC 2501	1
19-09971	IC DEC 6380	1
19-09921	IC DEC 7417	1
19-09928	IC DEC 7416	1
19-09686	IC DEC 7404	1
19-09373	IC DEC 9601 (M835 only)	1
19-09486	IC DEC 384	1
19-09004	IC DEC 7402	1
19-05578	IC DEC 7430	1
19-05577	IC DEC 7420	1
19-05576	IC DEC 7410	1
19-05575	IC DEC 7400	1
19-05547	IC DEC 7474	1
11-00114	Diode D664	4
11-00113	Diode D662	2
BC08J-10	Cable, 10 ft.	1
	IC DEC 74123 (M8350 only)	1

CHAPTER 2
KD8-E DATA BREAK INTERFACE

SECTION 1 INTRODUCTION

The KD8-E Data Break Interface is used by peripherals to transfer large blocks of data between the peripheral and memory. This interface cannot provide all the necessary signals for such a data transfer. Consequently, the positive I/O bus interface must also be used in the system. The concept of data transfers and the interrelationship of the data break interface, the positive I/O bus interface, and the OMNIBUS are explained in Chapters 6 and 10 of the *PDP-8/E & PDP-8/M Small Computer Handbook*, DEC 1972. A detailed discussion of CPU operation during a data break transfer is presented in Volume 1, Chapter 3, Section 6. The reader should be thoroughly familiar with this referenced information to benefit from the detailed logic discussion presented in Section 3.

SECTION 2 BLOCK DIAGRAM

Figure 2-1 is a functional block diagram of the KD8-E Data Break Interface. OMNIBUS signals are indicated by asterisks (on the block diagram only). When an interface receives a BRK RQST L signal from its peripheral, the request accept logic uses the next INT STROBE to assert signals that indicate acceptance of the request. These signals are used by the CPU and the peripheral in preliminary operations and by the interface priority network. The priority network compares the priority ranking of a peripheral with that of all other peripherals that make a break request at the same time. The interface of the highest ranking peripheral generates a PRIORITY signal that allows its CP Control logic to assert CP control lines. This action enables the peripheral to assume control of the CP Major Register gating and to directly address, via the BKMA Register logic, memory locations associated with the data transfer. The direction of transfer and the type of transfer are controlled by the interface data transfer logic. When the cycle select logic indicates that the true BREAK (BK) cycle is in progress, the data word is transferred to, or from, the address indicated by the BKMA Register logic. If the data transfer is from the peripheral, the data word is placed on the DATA 0–11 lines of the OMNIBUS by the data transfer logic.

SECTION 3 DETAILED LOGIC

2.1 CP REGISTER CONTROL LOGIC

Figure 2-2 shows the CP Register control logic. The NRB flip-flop determines if the interface can assert the CP Register control lines in response to a break request from the peripheral. This determination is based on the state of the NEW BRK OK L signal, which is asserted within the interface when conditions allow a data transfer (the NEW BRK OK L signal is discussed fully in Paragraph 2.2). If NEW BRK OK L has been asserted by the interface and the BRK RQST L signal has been asserted by the peripheral, the NBR flip-flop is set by the INT STROBE

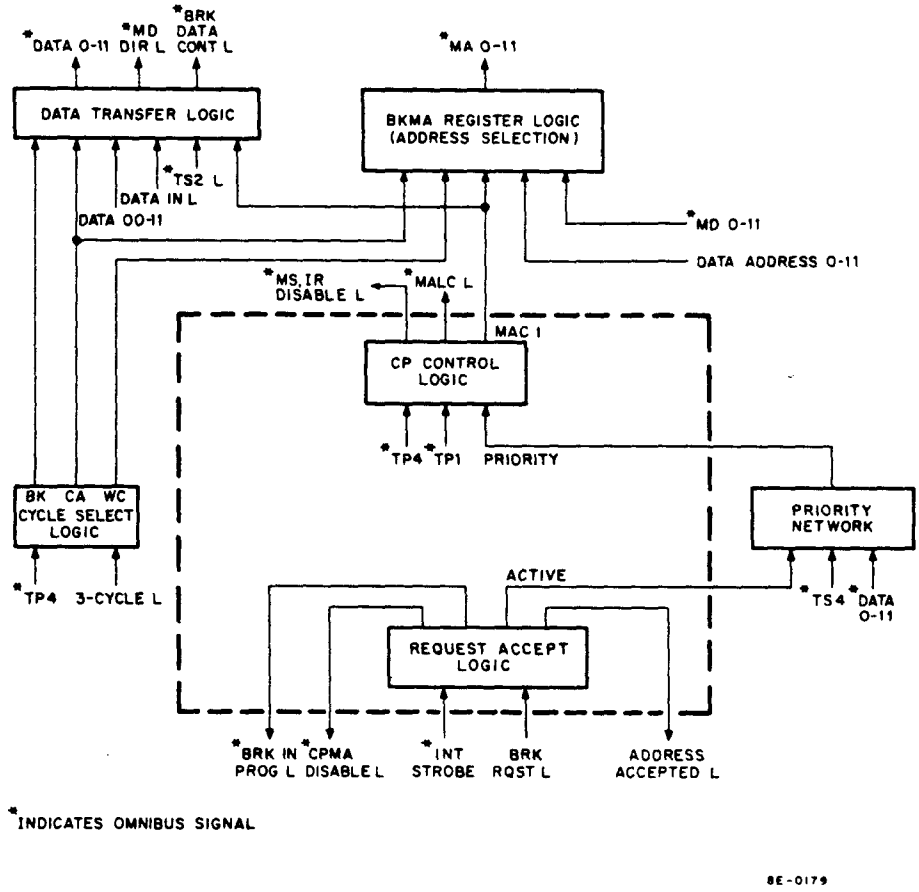


Figure 2-1 Data Break Interface, Block Diagram

signal (Figure 2-2). The 0-output of NBR then sets the ACTIVE flip-flop, which asserts the BRK IN PROG L and CPMA DISABLE L signals. The CPMA DISABLE L signal conditions a flip-flop on the Major Register Control module (Volume 1, Figure 3-110) so that TP4 can clear the flip-flop; the resulting signal, MAC L, removes the CPMA Register outputs from the MA lines. The BRK IN PROG L signal, which can be displayed on the programmer's console, ensures that only data break devices place priority information on the DATA lines during TS4.

When TS4 is entered, the 1-output of the ACTIVE flip-flop asserts the priority signal for this (*our*) interface. If other peripherals have made break requests at INT STROBE time, each peripheral's interface asserts a priority signal at TS4. The priority network (Paragraph 2.3) in each active interface examines these signals to determine if it has the highest priority of all the devices currently attempting to use the data break system. If our peripheral is not of sufficiently high priority, it must wait until the next TS4 signal; at that time the priority signals are again compared. If *our* peripheral has highest priority, the D-inputs of the MAC1 and MAC2 flip-flops are taken to a positive voltage; the flip-flops are then set at TP4. The 1-output of MAC1 not only asserts the MS, IR DISABLE L signal, which places the CP in the DMA state, but also conditions the MALC flip-flop so that it can be set when the TP1 pulse occurs. The 1-output of MALC then asserts the MALC L signal, which ensures that the CPMS Register and the CPMA Register will resume normal operation in the correct major state and at the correct memory address, respectively.

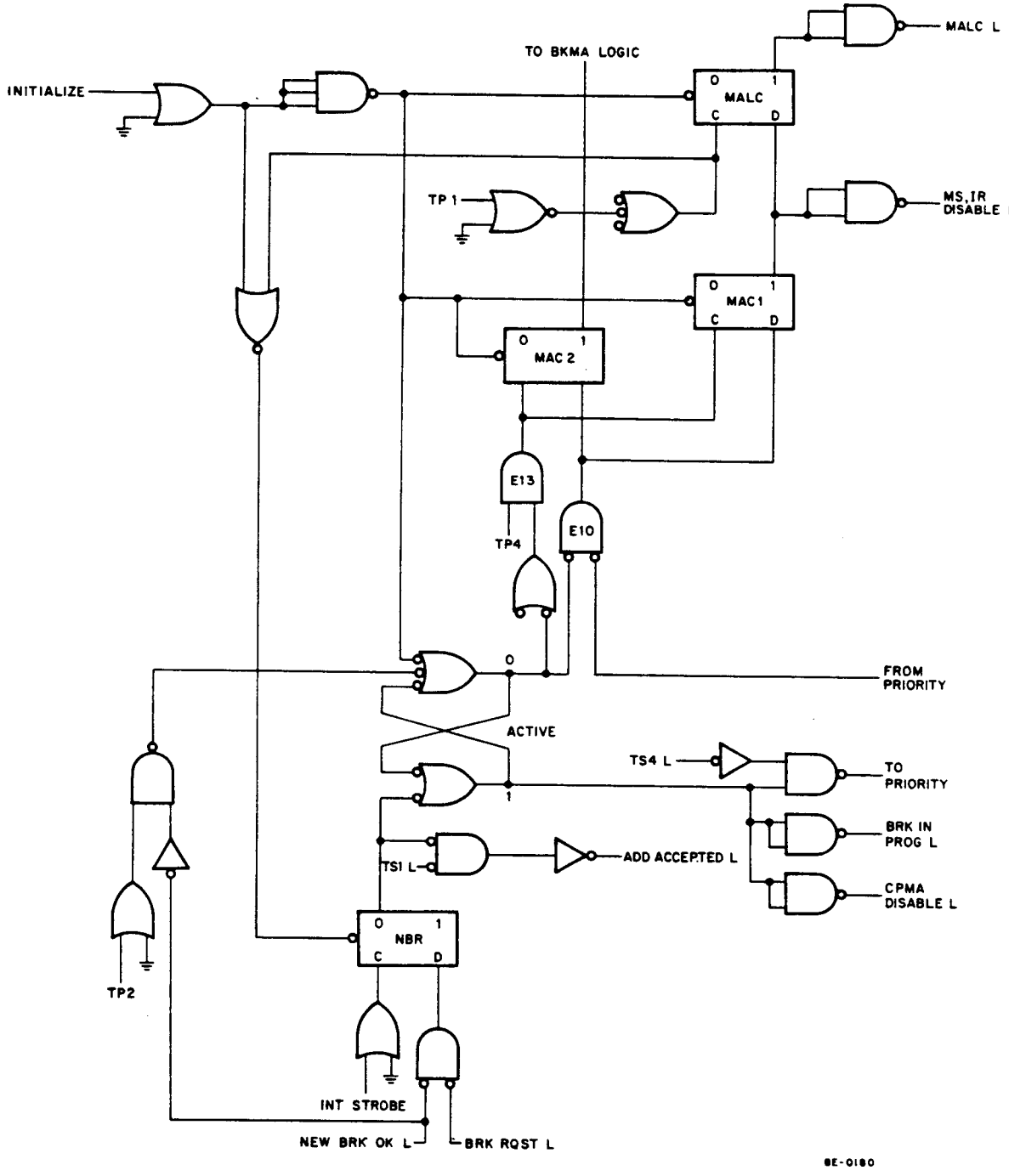


Figure 2-2 CP Register Control Logic

Note that ADD ACCEPTED L is asserted during TS1 of the first cycle following INT STROBE, regardless of the outcome of the priority check. This signal clears the break request flip-flop in the peripheral, allowing the peripheral to make another request when it is ready. At TP1, the NBR flip-flop is cleared, also regardless of what occurs in the priority network. Thus, this flip-flop is active for only the short time necessary to indicate acceptance of the break request. In contrast, the ACTIVE flip-flop is cleared only at TP2 of a true break cycle (defined and explained in Paragraph 2.2), which can be delayed for some time by priority considerations. Both NBR and ACTIVE are used extensively as control signals in other functional sections of the interface.

2.2 CYCLE SELECT LOGIC

After *our* interface takes control of the CP, a data transfer can be made. The CP is in the DMA state and remains in this state as long as MS, IR DISABLE L remains low. Each timing cycle (a "slow" cycle of 1.4 μs) that occurs during the DMA state is used by the interface/peripheral to accomplish tasks necessary for the data transfer. The actual data word transfer takes place during the Break (BK) cycle of operation. For 1-cycle peripherals only the BK cycle is necessary; however, 3-cycle devices require a Word Count (WC) cycle and a Current Address (CA) cycle before the BK cycle. This section describes the method of selecting each of the three cycles of operation; the details of what occurs during each cycle are presented in succeeding sections, except that certain BK cycle operations are detailed here.

Figure 2-3 shows the cycle select logic. When one of the three flip-flops shown (WC, CA, and BK) is set at TP4, the respective operation cycle is entered. If the peripheral is a 3-cycle device, the 3 CYCLE line is wired to ground within the peripheral. Thus, pin 2 of the DEC 8271 IC is positive voltage (high). This high is gated to the D-input of the WC flip-flop, providing the 8271 load (L) input is also high and the shift (S) input is low (see Volume 1, Appendix A, for details about the 8271 IC). This provision is met each time the interface accepts a break request from the peripheral (the 1-output of NBR goes high at INT STROBE time). The WC flip-flop is set at TP4 – the same TP4 at which MAC1 and MAC2 are set (because the D-input of both the CA and BK flip-flops is low, TP4 clears these flip-flops). Note that TP4 is NANDed with the output of a NOR gate (E18) that can be enabled by the 0-output of the ACTIVE flip-flop. This means that the WC flip-flop can be set even though access to the CP has been claimed by another peripheral during TS4 (the ACTIVE flip-flop is set prior to the priority check and remains set until TP2 of the BK cycle). If this happens, the operations that normally occur during the WC cycle are suspended for at least one cycle. One of these normal operations is the clocking of the 8271 flip-flops at TP4. To suspend this clocking process, the 8271 is placed in the "hold" mode by the NBR and MALC flip-flops (Table 2-1). The NBR flip-flop is cleared at TP1 of the suspended cycle, while the MALC flip-flop remains in the clear state (MALC is set at TP1 of a normal cycle). The "hold" condition remains in effect until *our* peripheral has priority; at this time a normal WC cycle is entered.

At TP1 of the normal WC cycle NBR is cleared and MALC is set (NBR remains clear until a new break request is accepted). As Table 2-1 shows, the 8271 IC is placed in the right-shift mode. In this mode, the three flip-flops comprise a shift register that is right-shifted by clock pulses. Thus, TP4 of the WC cycle causes the high at the 1-output of WC to be shifted into the CA flip-flop (CA is set, while WC is cleared). The CA flip-flop, also, can be set regardless of the results of the TS4 priority check (as before, the 0-output of ACTIVE enables TP4 to clock the flip-flop). The normal CA cycle operations are then suspended for at least one timing cycle. At TP1 of the suspended cycle, MALC is cleared; the 8271 is placed in the "hold" mode, preventing TP4 of the suspended CA cycle from clocking the flip-flops. When *our* peripheral has priority, the normal CA cycle is entered, MALC is set at TP1 time, and the 8271 IC is again placed in the right-shift mode. The CA cycle operations are carried out and, at TP4, the BK flip-flop is set, while the CA flip-flop is cleared.

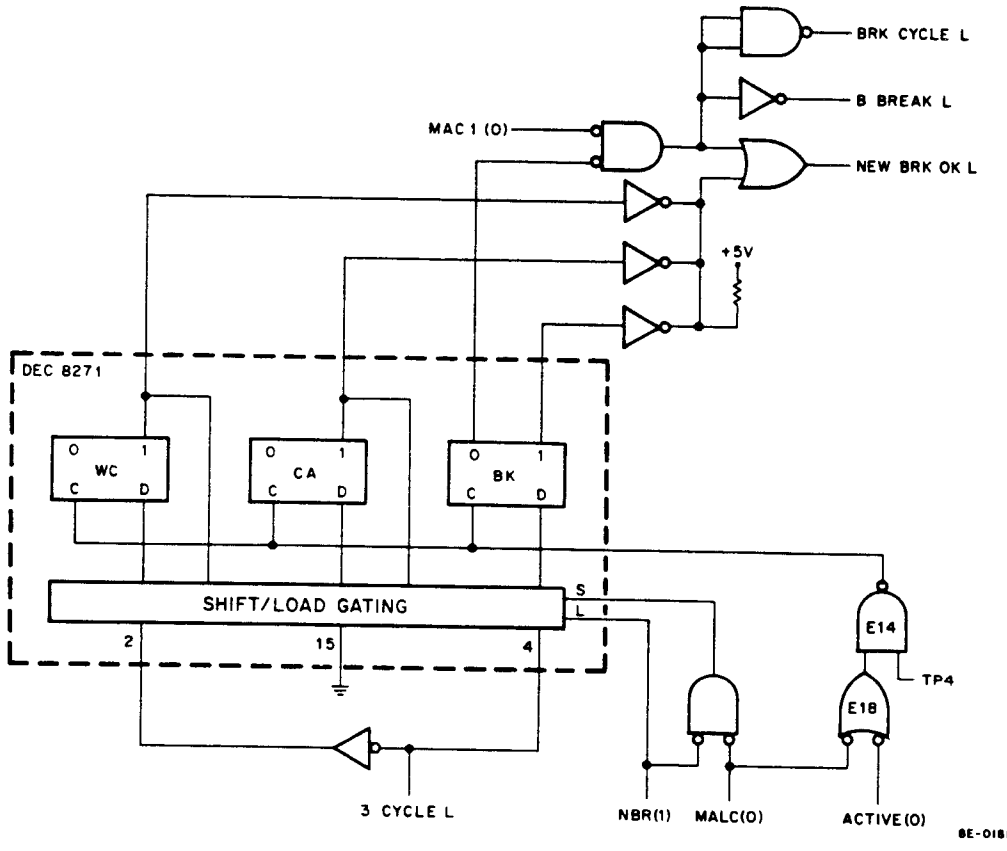


Figure 2-3 Cycle Select Logic

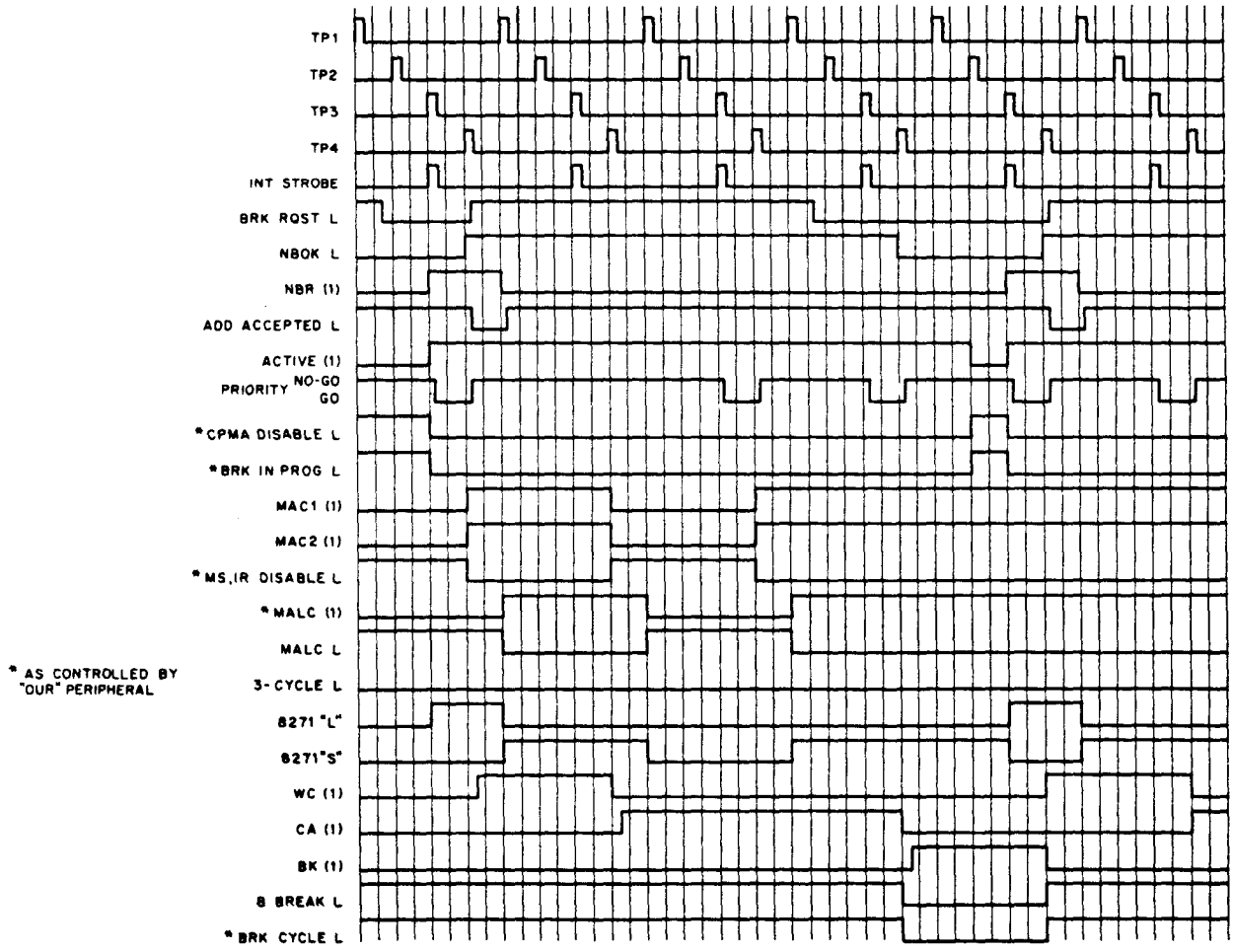
Table 2-1
8271 IC Control Signals

NBR F/F	MALC F/F	S	L	8271 IC Control State
Clear	Clear	Low	Low	Hold
Set	–	Low	High	Parallel Load
Clear	Set	High	Low	Right Shift

The BK flip-flop, too, is set regardless of priority. If another peripheral has priority, the normal BK cycle operations are suspended and the 8271 IC is placed on the "hold" condition for at least one cycle. When *our* peripheral has priority, the normal BK cycle is entered at TP4. The 0-output of BK is NANDed with the 0-output of MAC1 to assert NEW BRK OK L, BRK CYCLE L, and B BREAK L (Figure 2-3). Because MAC1 is cleared at TP4 if another peripheral has priority, these signals are asserted only during a normal break cycle. NEW BRK OK L tells the NBR flip-flop that data is about to be transferred and that a break request can be accepted at the next INT STROBE time; BRK CYCLE L is applied to the programmer's console display to indicate the normal or "true break" cycle; B BREAK L clocks the data into or out of the peripheral's buffer register, depending upon the direction of transfer. At TP2 of the true BK cycle the ACTIVE flip-flop is cleared, negating the CP Register

control lines. If the peripheral has not asserted the BRK RQST L signal before INT STROBE time of this cycle, NBR and ACTIVE remain clear and the CP Register control lines remain negated. MAC1, MAC2, and BK are cleared at TP4, while MALC is cleared at TP1 of the next timing cycle (because ACTIVE is clear when this TP4 occurs, the 0-output of MALC is used to enable TP4 to clock the BK flip-flop). If a break request was made before INT STROBE time, the WC flip-flop is set at the same time that the BK flip-flop is cleared; the break operation is repeated as many times as necessary.

Figure 2-4 is a timing diagram relating the signals discussed in this section and in the preceding section, CP Register Control Logic (the time scale does not reflect true processor timing; refer to Volume 1, Chapter 3, for timing information).



NOTE:
3-Cycle device xfer showing 1 word xfer with a priority break during CA cycle; WC cycle is shown for second word xfer.

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Figure 2-4 Timing, Register Control and Cycle Select Logic

2.3 PRIORITY LOGIC

Figure 2-5 shows the priority logic. Each peripheral interface contains a nearly identical circuit; differences exist only in the placement of jumper wires, which are designated A0–A11 and B0–B11 in Figure 2-5. The priority of a peripheral is established on the interface by removing a particular A jumper (all A jumpers are wired in place during production of the interface) and installing the corresponding B jumper. For example, to establish a "0" priority for *our* peripheral, remove A0 and install jumper B0. Note that this action disables all 12 NAND gates (ICs E17, E34, and E49). Thus, the output from NOR gate E18 is low. When the interface accepts a break request from the peripheral, the ACTIVE flip-flop is set at INT STROBE time. The 0-output of ACTIVE enables NAND gate E10 to assert the PRIORITY signal; therefore, *our* interface/peripheral begins the data break operation. Because *our* peripheral has only to request a break for that request to be granted, *our* peripheral has been assigned highest priority. No other interface can have its A0 jumper removed, or its B0 jumper connected.

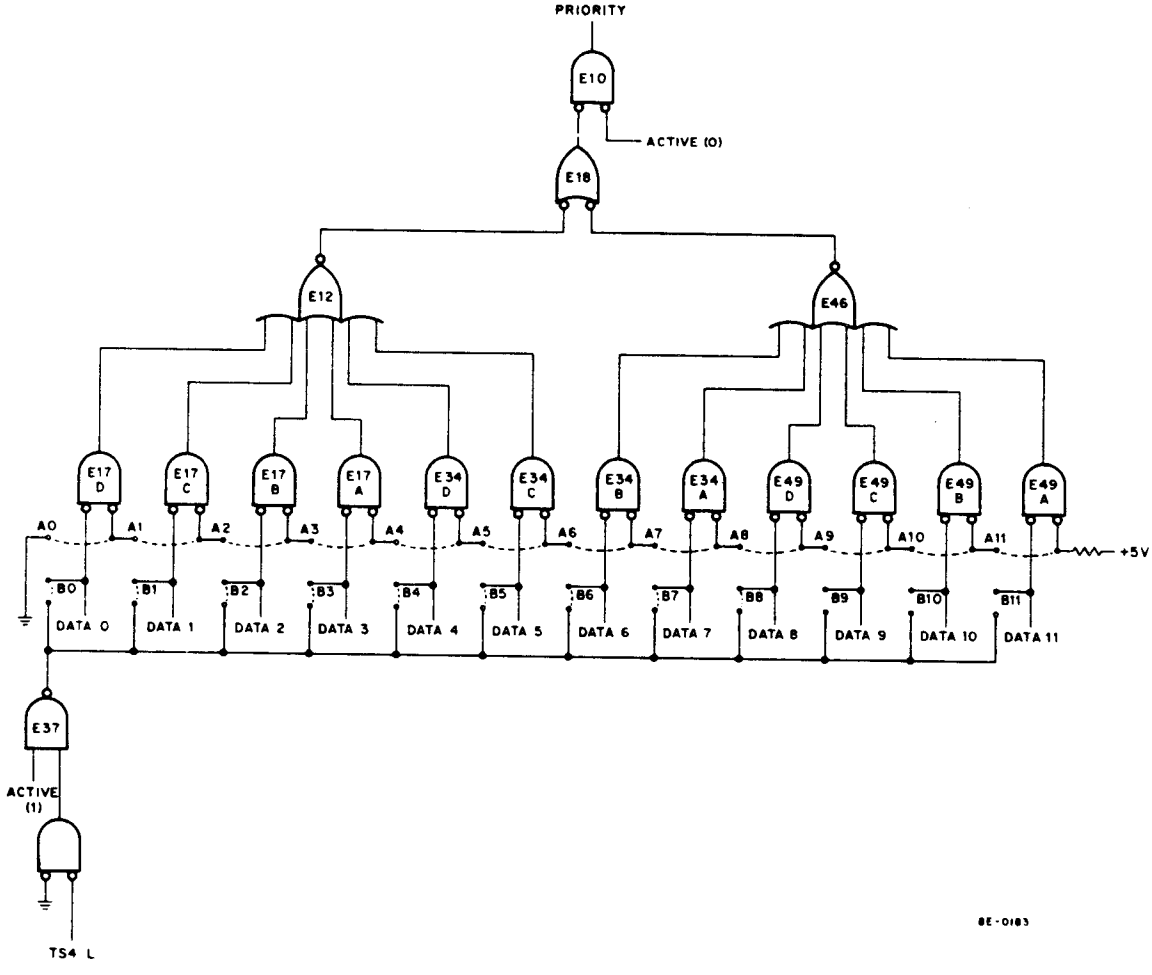

Figure 2-5 Priority Logic

As many as 11 other peripherals can have a break request accepted by their respective interfaces at INT STROBE time. No matter what priority has been established for these peripherals, each of the 11 interfaces has an A0 jumper in place. Note that when *our* interface ACTIVE flip-flop is set, NAND gate E37 brings the DATA 0 line low (*our* B0 jumper is in place) during TS4. Because all interfaces monitor the DATA lines, NAND gate E17D of each other interface is enabled. Thus, these interfaces cannot assert their PRIORITY signals as long as *our* peripheral requests data breaks.

As another example, consider what happens if *our* peripheral ranks only third highest in the peripheral priority structure. This priority is established on *our* interface by removing jumper A2 and connecting jumper B2. Because jumpers A0 and A1 are left in place, two other interfaces can keep *our* peripheral from beginning a data break operation. If the second highest priority peripheral has a break request accepted at the same time *our* peripheral's request is accepted, its interface brings the DATA 1 line low during TS4 time. NAND gate E17C on our interface is enabled and the PRIORITY signal remains negated. Until this other peripheral has completed the data break operation, our peripheral remains inactive. As has been implied, priority decreases from left to right, i.e., the lower the priority of the peripheral, the higher the number of the A jumper removed and B jumper installed. Thus, to establish priority on the lowest ranking peripheral's interface, remove jumper A11 and install jumper B11.

2.4 BKMA REGISTER LOGIC

Figure 2-6 shows the BKMA Register logic. This logic enables the peripheral to reference memory locations associated with the data break transfer. A peripheral that has made a break request must provide its interface with a memory address via the DATA ADDRESS 0–11 lines (Figure 2-6). This address is gated through DEC 8266 (refer to Volume 1, Appendix A, for details of this IC) to the parallel-load inputs of the 8271 ICs (the gating for bits 0 through 10 is identical; thus, the description and the illustration detail events for only bit 0 and bit 11). When the interface accepts the peripheral's request at INT STROBE time, the 0-output of the NBR flip-flop enables NOR gate E15, placing the 8271 ICs in the "load" condition (Table 2-1). At the same time, one input of NAND gate E14 is sent high by the 0-output of the ACTIVE flip-flop. At TP4, E14 is enabled and the BKMA Register flip-flops are loaded with the address on the DATA ADDRESS lines. If the peripheral has priority, the MAC2 flip-flop is set, also at TP4; the 1-output of the flip-flop enables NAND gate E1, placing DATA ADDRESS bit 0 on the MA0 line. If the peripheral does not have priority, the address is retained in the BKMA Register but not gated onto the MA lines until MAC2 is set at a later TP4 time. The NBR flip-flop is cleared at TP1, regardless of the outcome of the priority check, and NOR gate E15 places the 8271 ICs in "hold".

If the peripheral is a 1-cycle device, the address placed on the MA lines at TP4 is that of the memory location to or from which the data word is to be transferred. Note that NAND gate E26 is enabled in this situation (the BK flip-flop of the cycle select logic is set, the WC flip-flop is clear). Thus, the full 12- or 15-bit address supplied by the peripheral is placed on the MA lines. However, if the peripheral is a 3-cycle device, the WC cycle is entered first after a break request is accepted. NAND gate E26, disabled during the WC cycle, in turn disables NAND gate E40. Thus, DATA ADDRESS bit 11 is not gated onto the MA11 line; rather, MA11 is high, logic 0, during the cycle. The address placed on the MA lines during the WC cycle is that of the memory location containing the peripheral's WC Register; this address is hard-wired in the peripheral and is even (bit 11 is logic 0) so that the CA Register can be easily referenced during the next timing cycle, as is explained in the following paragraph.

During the WC cycle, the count in the WC Register is transferred from memory to the CP, incremented, and returned to the register. At TP4, the WC flip-flop is cleared and the CA flip-flop is set. If the peripheral still has priority, NAND gate E37 is enabled, pulling the MA11 line low. The MA0–10 lines carry the same address as during the WC cycle. Thus, the peripheral's hard-wired address is incremented and the new address is that of the memory location containing the peripheral's CA Register.

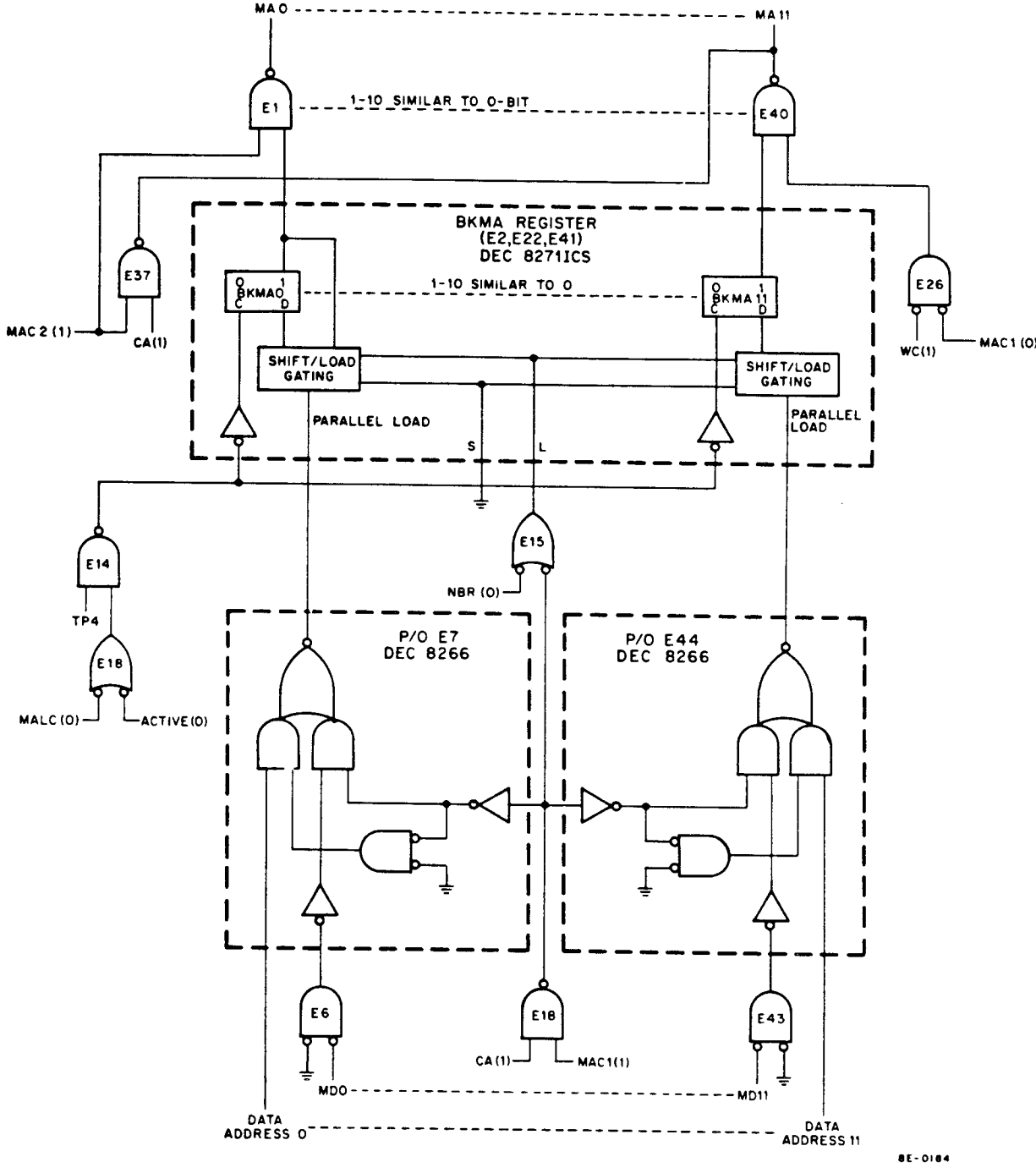

Figure 2-6 BKMA Register Logic

At the same time (TP4) that the CA Register address is placed on the MA lines, the CA flip-flop enables NAND gate E18. This gate, in turn, enables NOR gate E15, which places the BKMA Register in the "load" condition. Also, NAND gate E18 removes the DATA ADDRESS lines from the parallel-load inputs of the BKMA Register, substituting the MD0–11 lines. Note that these actions do not take place prior to the negative transition at the BKMA Register flip-flop clock inputs. Thus, the BKMA Register retains the WC Register address until TP4 of the CA cycle.

During the CA cycle, the address in the CA Register is transferred from memory to the CP, incremented, and returned to the register. The address, after incrementation (the current address), is that of the location to or from which the data is to be transferred. Thus, this current address must be placed in the BKMA Register, and transreffed from there to the MA lines at the beginning of the BK cycle. The current address is sent via the MD lines to the CP where it is incremented. At TP2, the result is returned to the MD lines and remains on these lines for the latter portion of the CA cycle. Therefore, at TP4 of the CA cycle, the BKMA Register parallel-load inputs reflect the current address. Because the BKMA Register is in the "load" condition, the current address is loaded into the register. At approximately the same time, the BK flip-flop is set, while the CA flip-flop is cleared. Because E37 is disabled and E26 is enabled, the contents of BKMA0–11 are placed on the MA0–11 lines.

Also at TP4, NAND gate E18 is disabled. This action removes the MD lines from the parallel-load inputs, selects the DATA ADDRESS lines, and places the BKMA Register in "hold". Note that the MALC flip-flop keeps NOR gate E18 enabled throughout the BK cycle (ACTIVE is cleared at TP2), if the peripheral has priority. These two gates ensure that the BKMA Register is ready to begin a new transfer, if the interface accepts a break request at INT STROBE time of the BK cycle.

During the BK cycle, the data word is transferred to or from the location specified by the current address. The logic that accomplishes this transfer through the interface is covered in the following section, which also details the special operations of all three cycles.

2.5 DATA TRANSFER LOGIC

The data transfer logic (Figure 2-7) controls the direction and type of data transfer. Table 2-2 shows the relationship between the type and direction of transfer and the signal levels of the various control lines. The table should be used with Figure 2-7 for a good understanding of the logic details.

If the transfer is to be from the memory to the peripheral, a 12-bit data word is transferred from the addressed location via the positive I/O bus interface. The Data Break Interface asserts the MD DIR L signal so that the data word is rewritten in the memory location during the write half of the timing cycle. NAND gate E8B (Figure 2-7) is used to ground the MD DIR line. The BK (1) and MAC1 (1) signals ensure that the true break cycle is in progress. The third input to E8B is high because NAND gate E10A is enabled. E10A is controlled by the DI (Data In) and INC (INCrement) flip-flops, which are set and cleared respectively at TP1 time of an output (from memory) transfer.

Note that the peripheral need not assert any control lines for an output transfer. However, if an input (to memory) transfer is to be carried out, the peripheral usually grounds the DATA IN line (exceptions are noted in the discussion). The DI flip-flop is set at TP1 of the first cycle of the data break. If the peripheral is a 3-cycle device, this first cycle is a WC cycle. Since the BK flip-flop is clear, NAND gate E13 is disabled (note that the DI flip-flop is significant in the operation of E13 only during the BK cycle; thus, the decision to set or clear this flip-flop, by asserting or negating the DATA IN L signal, nned not be made during either the WC or CA cycles). One input of NAND gate E8A is high. If this is a normal WC cycle (this interface's peripheral has priority), E8A is enabled during TS2 by NAND gate E10B, pulling the DATA 11 line low. This signal bit of data is transferred to the CP and added to the word count, which is brought to the CP from the WC Register, providing the BRK DATA CONT L

signal is asserted by the interface. NAND gate E23 is used to assert this signal. Because this is a WC cycle, NAND gate E15 is disabled, enabling E23 (MAC1 is set because the peripheral has priority). Therefore, the word count is incremented. Because the MD DIR L signal is negated (both E8C and E8B are disabled during the WC cycle), this new word count is placed in the WC during the write half of the memory cycle.

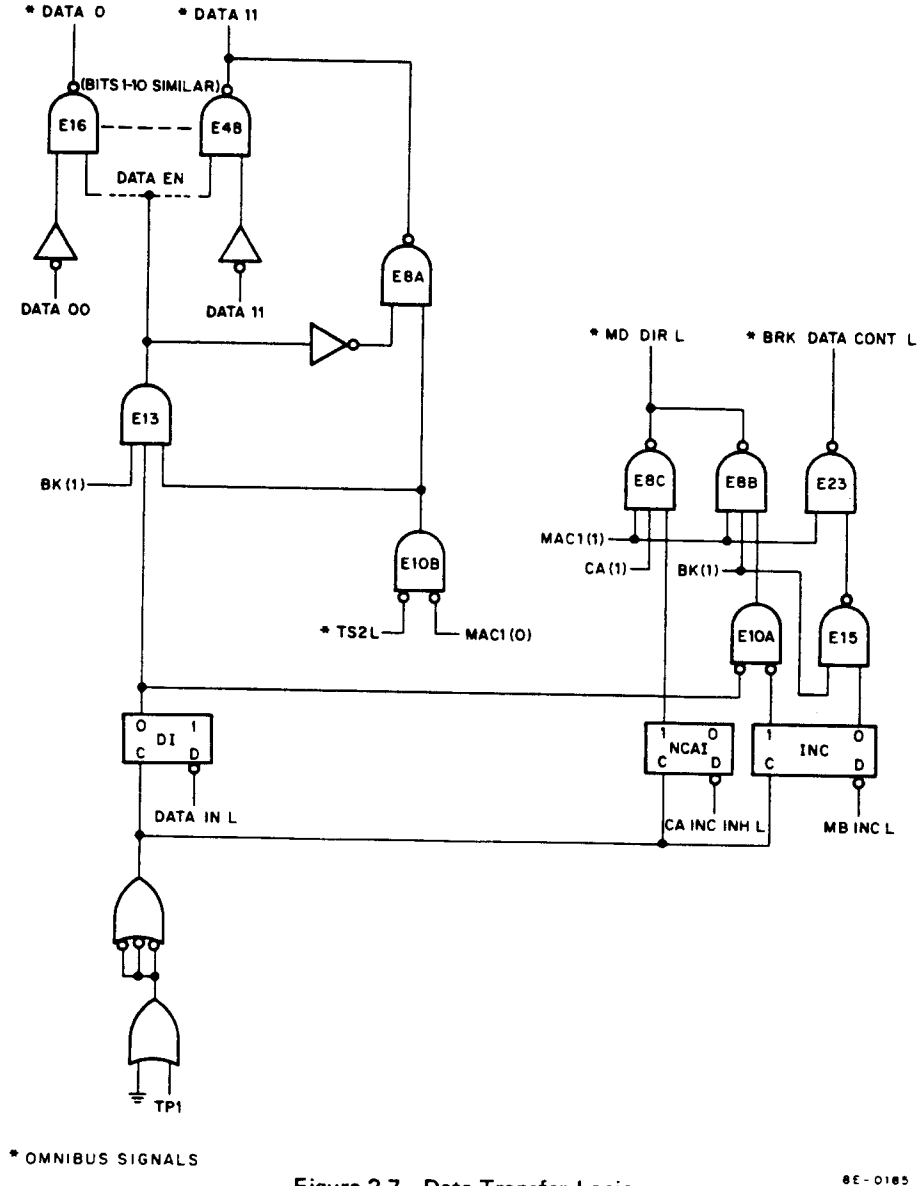

Figure 2-7 Data Transfer Logic

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During the CA cycle of the 3-cycle transfer, the current address is incremented in much the same way as the word count. Again, DATA 11 is pulled low by E8A during TS2 if the peripheral has priority. E23 asserts the BRK DATA CONT L signal, which enables DATA 11 and the current address to be added in the CP. If the MD DIR L signal is negated, the new address is sent to the CA Register during the write half of the cycle. Note that the MD DIR L signal is negated only if the NCAI (No Current Address Increment) flip-flop is clear. This flip-flop is

clocked at TP1 of a timing cycle and is normally clear. However, the peripheral can ground the CA INC INH line, causing the NCAI flip-flop to be set at TP1. NAND gate E8C then asserts the MD DIR L signal during the CA cycle. Thus, although the current address is incremented as usual, the original address (the one that was in the CA Register at the beginning of the cycle) is returned to the CA Register during the memory write.

Table 2-2
Control Signals, Cycle, Type, and Direction of Transfer

Cycle	WC	CA		BR			
Direction of Transfer	In	In		In			Out
Type of Transfer	Word Count Increment	Current Address Increment	No Current Address Increment	MB Increment	ADM	12-Bit Data Word	12-Bit Data Word
MD DIR L	High	High	Low	High	High	High	Low
BRK DATA CONT L	Low	Low	Low	Low	Low	High	High
DATA IN L	Low	Low	Low	High	Low	Low	High
MB INC L	High	High	High	Low	Low	High	High
CA INC INH L	High	High	Low	High	High	High	High

During the BK cycle of operation, whether of a 1- or 3-cycle operation, an input or output transfer can take place. As described at the beginning of this section, there is only one type of output data transfer, i.e., the transfer of a 12-bit data word from the addressed location. However, there are three types of input transfers that can be carried out. One of these is similar to the transfer that takes place during the WC and CA cycles, and is designated MB Increment. To accomplish this transfer, the peripheral grounds DATA IN and the MB INC lines. At TP1 the INC flip-flop is set, while the DI flip-flop is set. NAND gates E10A and E15 are disabled by the INC flip-flop. Thus, E23 asserts the BRK DATA CONT L signal and, because E8C is disabled during the BK cycle, E8B negates the MD DIR L signal. During TS2 the DATA 11 line is pulled low by E8A. This single bit is transferred to the CP, where it is added to the data word that is brought from the addressed memory location. The incremented data is then sent back to the addressed location during memory write.

Another type of input transfer, similar to the MB Increment, is designated Add to Memory (ADM). The peripheral grounds the MB INC line only so that both the DI flip-flop cleared and the INC flip-flop is set at TP1. During TS2 of the true break cycle, a 12-bit data word carried on the peripheral's DATA 00—11 lines is gated through the interface to the OMNIBUS DATA lines. This data is added in the CP to the data brought from the addressed memory location, and the result is rewritten in the memory location.

The third type of input transfer is that of a 12-bit data word to the addressed memory location. The peripheral grounds neither line; thus, TP1 clears the DI flip-flop and the INC flip-flop. NAND gate E15 is enabled and causes NAND gate E23 to negate the BRK DATA CONT L signal. NAND gate E10A is disabled by the 0-output of DI and, in turn, disables E8B. Because E8C is also disabled, the MD DIR L signal is again high. During TS2, a 12-bit data word is placed on the OMNIBUS DATA lines and transferred to the addressed memory location.

2.6 WC OVERFLOW LOGIC AND EMA REGISTER LOGIC

Figure 2-8 shows the WC Overflow logic and the EMA Register logic. The WC OVERFLOW L signal is generated by the interface during either a normal WC cycle or a true BK cycle if the OMNIBUS OVERFLOW L signal is asserted by the CP. OVERFLOW L is asserted during a WC cycle to indicate that the last word of a block is about to be transferred. WC OVERFLOW L is then used by the peripheral to terminate the data break operation. During a BK cycle the OVERFLOW L signal is asserted to indicate that an input transfer has resulted in assertion of the CP CARRY OUT L signal. In this case, WC OVERFLOW L is used in the peripheral as directed by the program.

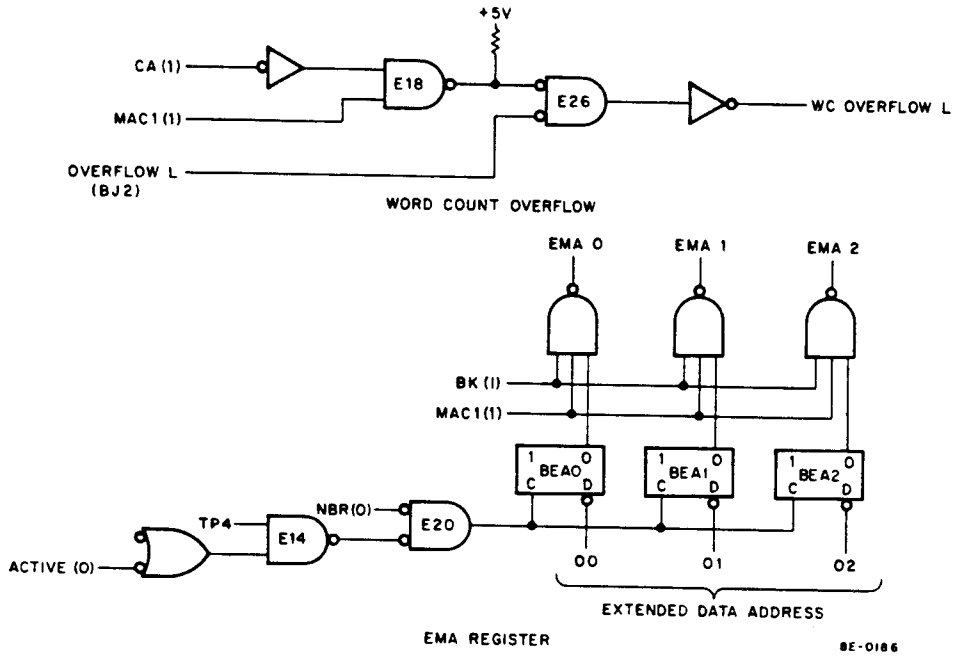

Figure 2-8 Word Count Overflow and EMA Register Logic

The EMA Register logic is used to specify the complete 15-bit memory address to or from which data is to be transferred. EMA0 is the MSB of the 15-bit address, while MA11 is the LSB (see Chapters 9 and 10 of the *PDP-8/E & PDP-8/M Small Computer Handbook* for definitions of OMNIBUS and External bus signals relating to extended memory). If the computer contains only the basic 4K memory, EMA 0, EMA 1, and EMA 2 are logic 0. When memory is extended (up to 32K, if desired), these three most significant bits are used to indicate which memory field is to take part in the data transfer. The peripheral specifies the memory field via the External bus Extended Data Address 00–02 lines (Figure 2-8). This field address is loaded into the BEA (Break Extended Address) register at TP4 of the first cycle of the break operation (Figure 2-4). If the peripheral is a 3-cycle device, the first cycle is the WC cycle. However, note that BEA Register information is placed on the EMA lines only during a true BK cycle. Thus, for a 3-cycle device the WC and CA Registers must be located in memory field 0, the basic 4K. The location to or from which data is to be transferred can be contained in an extended memory field.

SECTION 4 MAINTENANCE

There are no specific maintenance procedures for the KD8-E itself. Each DEC peripheral has an associated MAINDEC or exerciser program that enables the technician to maintain both the option and the KD8-E Interface.

General information concerning corrective maintenance is included in Volume, Chapter 4. The technician will find this material helpful. The interface schematic, E-CS-M8360-0-1, indicates important test points, IC locations, and pin numbers; it should be used when maintenance is being performed.

The KD8-E connects directly to a single peripheral via two cables that are supplied with the interface (refer to *PDP-8/E & PDP-8/M Small Computer Handbook,* Chapter 10, for cabling rules and suggestions). Each cable connects to the interface with a 40-pin Berg connector and to the peripheral with a DEC M953A cable connector. From-To information for the cable is given in Table 2-3 (the cables are identical; refer to Chapter 10 of the *PDP-8/E & PDP-8/M Small Computer Handbook* for details concerning proper connection of the cables).

Table 2-3
KD8-E Cable Information

From (M953A Cable Conn.)	To (Berg Conn.)	From (M953A Cable Conn.)	To (Berg Conn.)
Gnd	A	Gnd	Y
Gnd	B	M2	Z
Gnd	C	Gnd	AA
B1	D	L1	BB
Gnd	E	Gnd	CC
D2	F	P2	DD
Gnd	H	Gnd	EE
D1	J	M1	FF
Gnd	K	Gnd	HH
E2	L	S2	JJ
Gnd	M	Gnd	KK
E1	N	P1	LL
Gnd	P	Gnd	MM
H2	R	T2	NN
Gnd	S	Gnd	PP
H1	T	S1	RR
Gnd	U	Gnd	SS
K2	V	V2	TT
Gnd	W	Gnd	UU
J1	X	Gnd	VV

Pins A2, B2, U1 and V1 on M953A not used.

Pins A1, C1, F2, K1, N1, R1, T1, C2, F2, J2, L2, N2, R2, and U2 on M953A are ground pins.

SECTION 5 SPARE PARTS

Table 2-4 lists recommended spare parts for the KD8-E. These spare parts can be obtained from any local DEC office or from DEC, Maynard, Massachusetts.

Table 2-4
KD8-E Recommended Spare Parts

DEC Part No.	Description	Quantity
10-01610	Capacitor 0.01 μF, 100V, 20%	2
11-00113	Diode D662	1
19-05575	IC DEC 7400	1
19-05579	IC DEC 7440	1
19-09004	IC DEC 7402	1
19-09057	IC DEC 74H10	1
19-09267	IC DEC 74H11	1
19-09971	IC DEC 6380	1
19-09486	IC DEC 384	1
19-09615	IC DEC 8271	1
19-09667	IC DEC 74H74	1
19-09686	IC DEC 7404	1
19-09972	IC DEC 6314	1
19-09973	IC DEC 97401	1
19-09928	IC DEC 7416	1
19-09934	IC DEC 8266	1
19-09955	IC DEC 7412	1
19-10010	IC DEC 2501	1

HOW TO OBTAIN SOFTWARE INFORMATION

Announcements for new and revised software, as well as programming notes, software problems, and documentation corrections are published by Software Information Service in the following newsletters.

Digital Software News for the PDP-8 Family
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Software Information Service
Digital Equipment Corporation
146 Main Street, Bldg. 3-5
Maynard, Massachusetts 01754

These forms, which are available without charge from the Program Library, should be fully filled out and accompanied by teletype output as well as listings or tapes of the user program to facilitiate a complete investigation. An answer will be sent to the individual and appropriate topics of general interest will be printed in the newsletter.

New and revised software and manuals, Software Trouble Report forms, and cumulative Software Manual Updates are available from the Program Library. When ordering, include the document number and a brief description of the program or manual requested. Revisions of programs and documents will be announced in the newsletters and a price list will be included twice yearly. Direct all inquiries and requests to:

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146 Main Street, Bldg. 1-2
Maynard, Massachusetts 01754

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☐ LINC-8 ☐ PDP-11 ☐ PDP-15
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