CHAPTER 6

CONSOLE OPERATION

6.1 INTRODUCTION

There are two types of consoles for the PDP-8/A—the operator's panel and the programmer's console. The operator's panel is supplied with each PDP-8/A. The programmer's console is optional.

6.2 OPERATOR'S PANEL

The operator's panel (Figure 6-1) contains the necessary switches to apply power and bootstrap the computer, and also contains the necessary indicators—POWER ON, RUN, and BATTERY CHARGING—to determine whether or not the computer is operating. Table 6-1 describes the function of the various switches on the panel. A PANEL LOCK switch is provided to prevent the accidental modification of memory contents or system operation by inappropriate use of switches on the programmer's console.

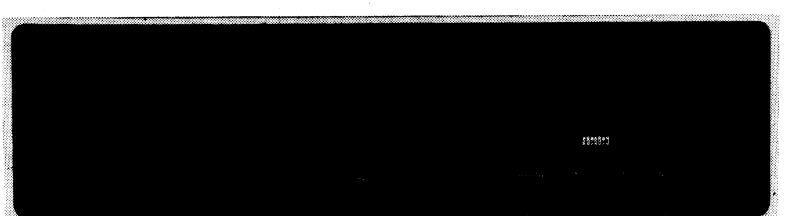

Figure 6-1 PDP-8/A Operator's Panel

6.3 PROGRAMMER'S CONSOLE

The key pad switches and indicators on the PDP-8/A programmers' console (Figure 6-2) augment the operator's panel by allowing manual control of computer operation and presenting a convenient indication of system conditions. PDP-8/A program execution can be started, stopped, monitored, or switched between various modes of operation by use of the keys. The key pad switches also provide a means of selecting a memory location or major register for examination and allow selective modification of read/write memory. Table 6-2 describes the indicators and functions relating to the programmer's console.

Table 6-1 PDP-8/A Operator's Console Controls and Indicators

CONTROL OR INDICATOR	FUNCTION
POWER ON/OFF	In the up position, this switch applies power to the computer and all controls and indicators. Power is removed by moving the switch down.
PANEL LOCK	In the up position, this switch prevents the removal of power from the computer and disables all key pad switches except switch register (SR) and the read functions.
BOOT	When this switch is down, the Omnibus SW line is disabled (voltage level high). When it is up, the SW line is asserted (low). This switch is used to start programmable read only memory (PROM) and bootstrap loader programs. The key pad BOOT switch on the programmer's console has the same function.
POWER	This indicator is lit when ac power is applied to the computer.
BATTERY CHARGING	This indicator is lit when the battery back-up supply is charging.
RUN	This indicator is lit when the RUN flip-flop is set.

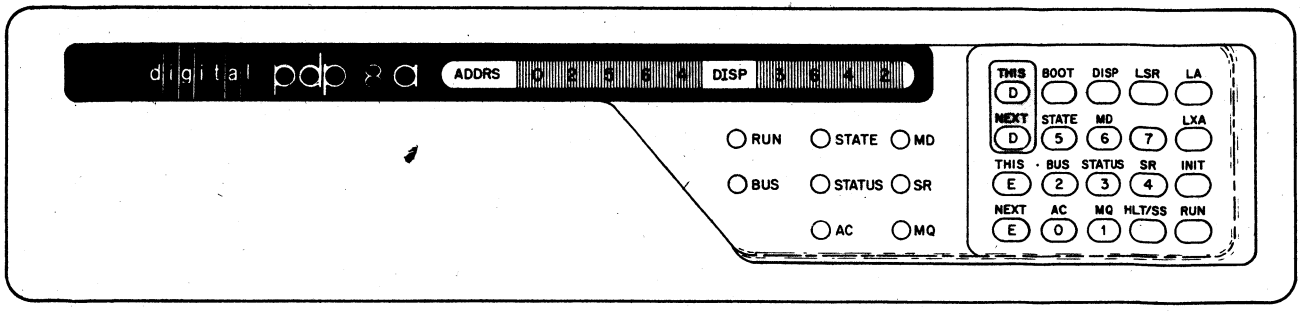

Figure 6-2 PDP-8/A Programmer's Console

Table 6-2 PDP-8/A Programmer's Console Controls and Indicators

CONTROL OR INDICATOR	FUNCTION
ADDRS (Octal Readout)	ADDRS is a 5 character octal readout that displays the content of the 3-bit extended memory address (EMA) register and the 12-bit memory address (MA) register. The five characters (digits) show the address of the memory to be accessed next.
DISP (Octal Readout)	DISP is a 4 character octal readout that displays the content of the register that has been selected for display. The accumulator (AC), multiplier quotient (MQ), STATUS register, switch register (SR), STATE, memory data (MD), or data bus (BUS), contents may be read. To select one of these for display, first depress the appropriate key pad switch (i.e., AC) and then press DISP. One of the LED indicators to the left of the key pad will be lit indicating which data is displayed in the readout. If none of the indicators are lit, the content of the entry register is displayed.
RUN	This indicator is lit when the RUN flip-flop is set.
Key Pad Switches AC (0)	When key pad AC and then DISP are depressed, the content of the AC is displayed in the 4 character octal readout. The AC indicator to the left of the key pad will also light.
MQ (1)	When key pad MQ and then DISP are depressed, the content of the MQ register is displayed in the 4 character octal readout. The MQ indicator to the left of the key pad will also light.
BUS (2)	When key pad BUS and then DISP are depressed, the content of the DATA BUS (DATA 0–11) is displayed in the 4 character octal readout. The BUS indicator to the left of the key pad will also light.
STATUS (3)	When key pad STATUS and then DISP are depressed, the contents of the STATUS register is displayed in the 4-bit octal readout (Figure 6-3). The STATUS indicator to the left of the key pad will also light. The six most significant bits of the status register (bits 0–5) indicate either a set or cleared condition (logical one or logical zero). Thus, the octal readout for

Table 6-2 (Cont.)
PDP-8/A Programmer's Console Controls and Indicators

CONTROL OR INDICATOR	FUNCTION
	these digits must be decoded to determine whether the bit is set or cleared.

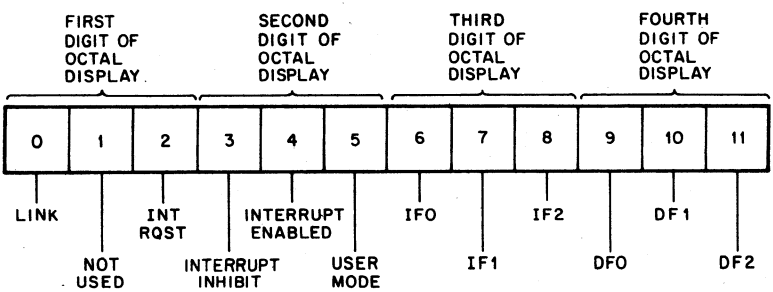

Figure 6-3 Status Register

First Digit Position	An octal 4 or 5 indicates that the link is set. An octal 1 or 5 indicates that the Omnibus interrupt request line is asserted.
Second Digit	An octal 4, 5, 6, or 7 indicates that the interrupt inhibit flip-flop is set. The interrupt inhibit flip-flop is located in the memory extension and timeshare option. An octal 2, 3, 6, or 7 indicates that the interrupt system is enabled. An octal 1, 3, 5, or 7 indicates that the USER MODE line is asserted. Signal USER MODE originates in the memory extension and timeshare option on the KM8-A option board to disable execution of all OSR, LAS, HLT and IOT instructions when the computer is operating in timeshare mode.
Third Digit	Displays the content of the 3-bit instruction field register (IF0–2) contained in the memory extension and timeshare option on the KM8-A option board.
Fourth Digit	Displays the content of the 3-bit data field register (DF0–2) contained in the memory extension and timeshare option on the KM8-A option board.
SR (4)	When key pad switch SR and then DISP are depressed, the content of the SR (switch register) will be displayed in the 4 character octal readout. The SR indi-

Table 6-2 (Cont.)
PDP-8/A Programmer's Console Controls and Indicators

CONTROL OR INDICATOR	FUNCTION
	cator to the left of the key pad will also light.
STATE (5)	When key pad switch STATE and then DISP are depressed, the condition of the major states, 3 bits of the instruction register (IR0–2), and 6 major Omnibus signals are displayed in the 4 character octal readout (Figure 6-4). The STATE indicator to the left of the key pad will also light. The octal readout must be decoded to determine if the individual bits are in a set or cleared condition (a logical one or a logical zero).

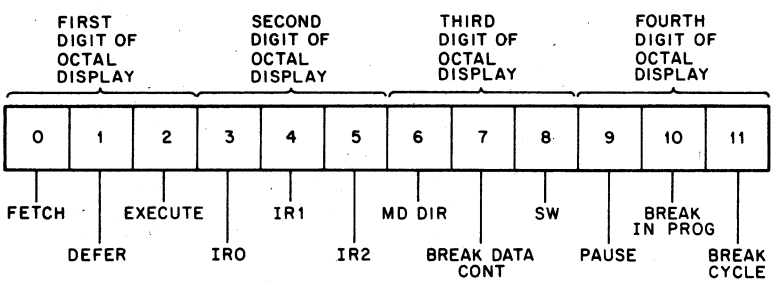

Figure 6-4 Major States Register

First Digit	A zero indicates that the processor is in the DMA state.
	An octal 1 indicates that the processor is in the EXECUTE major state.
	An octal 2 indicates that the processor is in the DEFER major state.
	An octal 4 indicates that the processor is in the FETCH major state.
Second Digit	Displays the content of the 3-bit instruction register (IR0–2).
Third Digit	An octal 4, 5, 6, or 7 indicates that the MD DIR line on the Omnibus is asserted (low). Signal MD DIR is low and bit 6 is a logical one during operations that read data from memory. MD DIR is high and bit 6 is a logical 0 during operations that write data into memory.

Table 6-2 (Cont.)
PDP-8/A Programmer's Console Controls and Indicators

CONTROL OR INDICATOR	FUNCTION
	An octal 2, 3, 6, or 7 indicates that BREAK DATA CONT line on the Omnibus is asserted. BREAK DATA CONT is low and bit 7 is a logical one during some direct memory access (DMA) operation.
	An octal 1, 3, 5, or 7 indicates that the SW line on the Omnibus is asserted. This occurs only when BOOT on the programmer's console or the operator's panel is depressed.
Fourth Digit	An octal 4, 5, 6, or 7 indicates that the I/O PAUSE line on the Omnibus is asserted. Signal I/O PAUSE L is generated during execution of an IOT instruction.
	An octal 2, 3, 6, or 7 indicates that the BREAK IN PROG line on the Omnibus is asserted (one or more devices are requesting a data break). The highest priority device will begin a DMA operation at the beginning of the next cycle.
	An octal 1, 3, 5, or 7 indicates that the BREAK CYCLE line on the Omnibus is asserted, (a DMA operation is taking place).
MD (6)	When MD and then DISP are depressed, the data on the 12-bit MEMORY DATA bus (MD0–11) on the Omnibus are displayed in the four character octal readout. The bus normally carries the content of the last memory location addressed by the 15-bit memory address register.
LA	Depressing LA (load address) loads the contents of the entry into the central processor memory address (CPMA) register and enables the FETCH major state for the next processor cycle.
LXA	Depressing LXA (load extended address) loads the right most digit of the entry into the data field (DF) register and the next digit of the entry into the instruction field (IF) register.
INIT	Depressing INIT (Initialize) generates an INIT pulse that clears the AC, the LINK, all I/O device flags and registers, and all interrupt system flip-flops. This is equivalent to a programmed CAF instruction.

Table 6-2 (Cont.)
PDP-8/A Programmer's Console Controls and Indicators

CONTROL OR INDICATOR	FUNCTION
RUN	Depressing RUN generates a MEM START L signal, which sets the RUN flip-flop. The program starts executing at the address that is in the CPMA register.
LSR	Depressing LSR switch loads the entry into the switch register. The switch register serves as a 12-bit temporary storage register for data entries. The contents of the switch register can be read under program control by the OSR and LAS instruction.
BOOT	Depressing BOOT twice causes the SW flip-flop to assert and then negate the SW line on the Omnibus. The transition from assertion to negation of the SW line causes a bootstrap operation to be performed. The signal from this BOOT switch is ORed with the signal generated by BOOT on the operator's panel so that either switch can assert the SW signal on the Omnibus.
E THIS	Depressing E THIS (examine this) loads the contents of the memory location addressed by the CPMA register into the memory buffer (MB) register. The CPMA and PC are not incremented after this operation. To observe the contents of the MB, depress MD, then DISP.
E NEXT	Depressing E NEXT (examine next) loads the content of the memory location addressed by the CPMA into the memory buffer (MB) register and increments the CPMA and PC registers. This feature allows the operator to step through a program and observe the operation of one of the major registers, buses, etc., in the octal readout.
D THIS	Depressing D THIS (deposit this) loads the content of the entry into the MB register and into memory at the address specified by the CPMA register. The CPMA and PC are not incremented by this operation.
D NEXT	Depressing D NEXT (deposit next) loads the content of the entry into the MB register and into memory at the address

Table 6-2 (Cont.)
PDP-8/A Programmer's Console Controls and Indicators

CONTROL OR INDICATOR	FUNCTION
	specified by the CPMA register. At the end of the operation, the PC and CPMA registers are incremented.
HLT/SS	Depressing HLT/SS (halt/single step) while the machine is running will cause it to stop. If the machine is stopped, depressing HLT/SS causes the machine to execute one machine cycle.

6.3.1 Entering Data From the Programmer's Console

Data is entered into registers from the programmer's panel by depressing the numbered key pad switches corresponding to the octal number to be entered, followed by depressing the key pad switch corresponding to the register into which the data is to be entered. For example, to load an octal number 7000 into the switch register, depress 7, then depress 0 three times, and then depress LSR. The data entered will be transferred to the switch register. To read the data that was entered in the switch register, press SR and then DISP (Table 6-2) and the data is displayed in the 4 character octal readout.

6.3.2 Examining Memory Locations

To determine the content of a location in memory, enter the memory field and depress LXA, then enter the memory address and depress LA. Depress MD and then DISP. Now depress E THIS and the contents of this memory location will be displayed in the 4 character octal readout. If two or more consecutive memory locations are to be examined, depress E NEXT. The content and the next memory location will be displayed each time E NEXT is depressed.

6.3.3 Entering Data in Memory

To enter (deposit) data in a memory location, first enter the field into which data is to be deposited and depress LXA. Then, enter the address and depress LA. Now enter the data and depress D THIS. If data is to be entered into two or more consecutive memory locations, depress D NEXT after each entry is made.