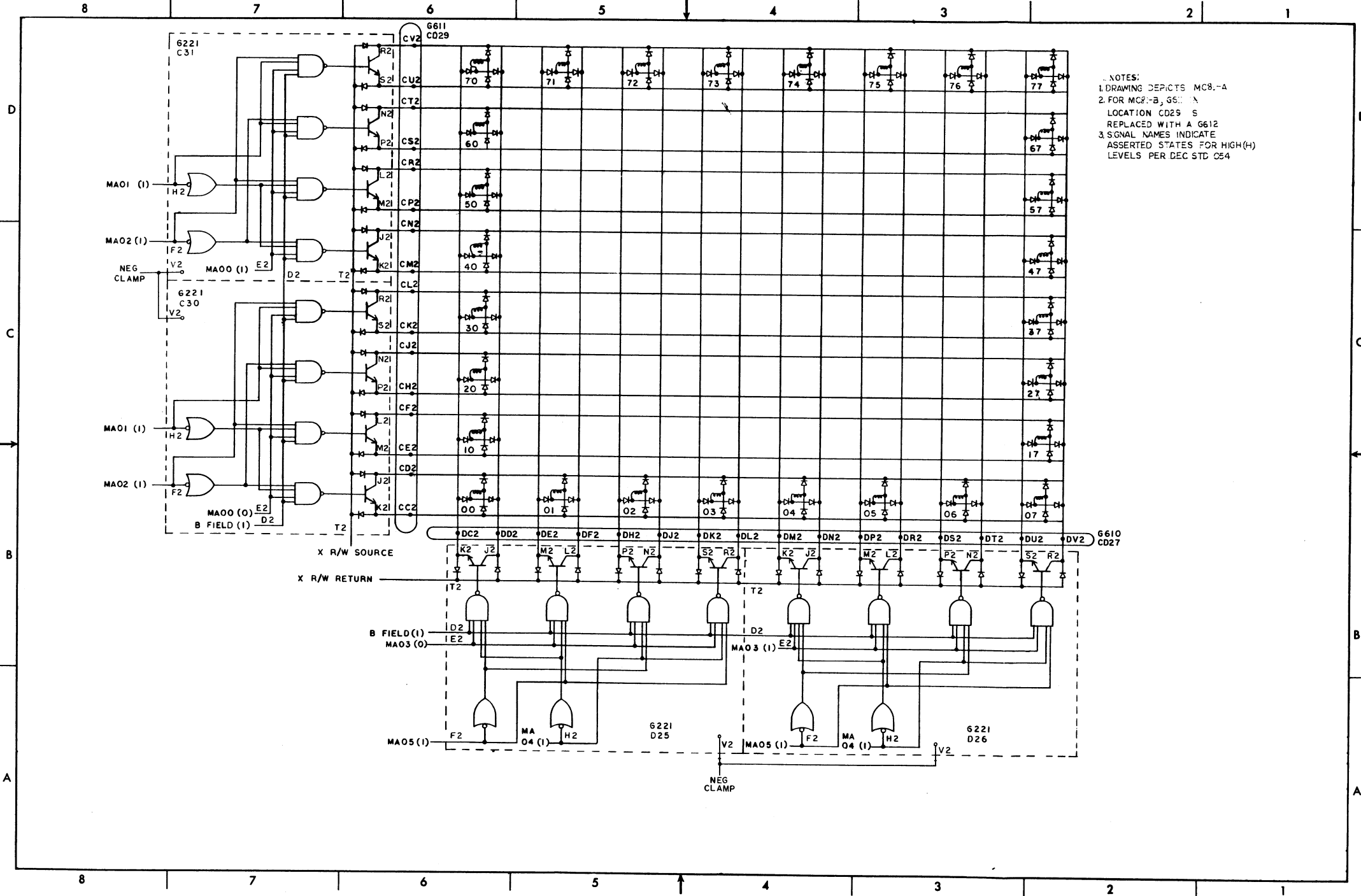


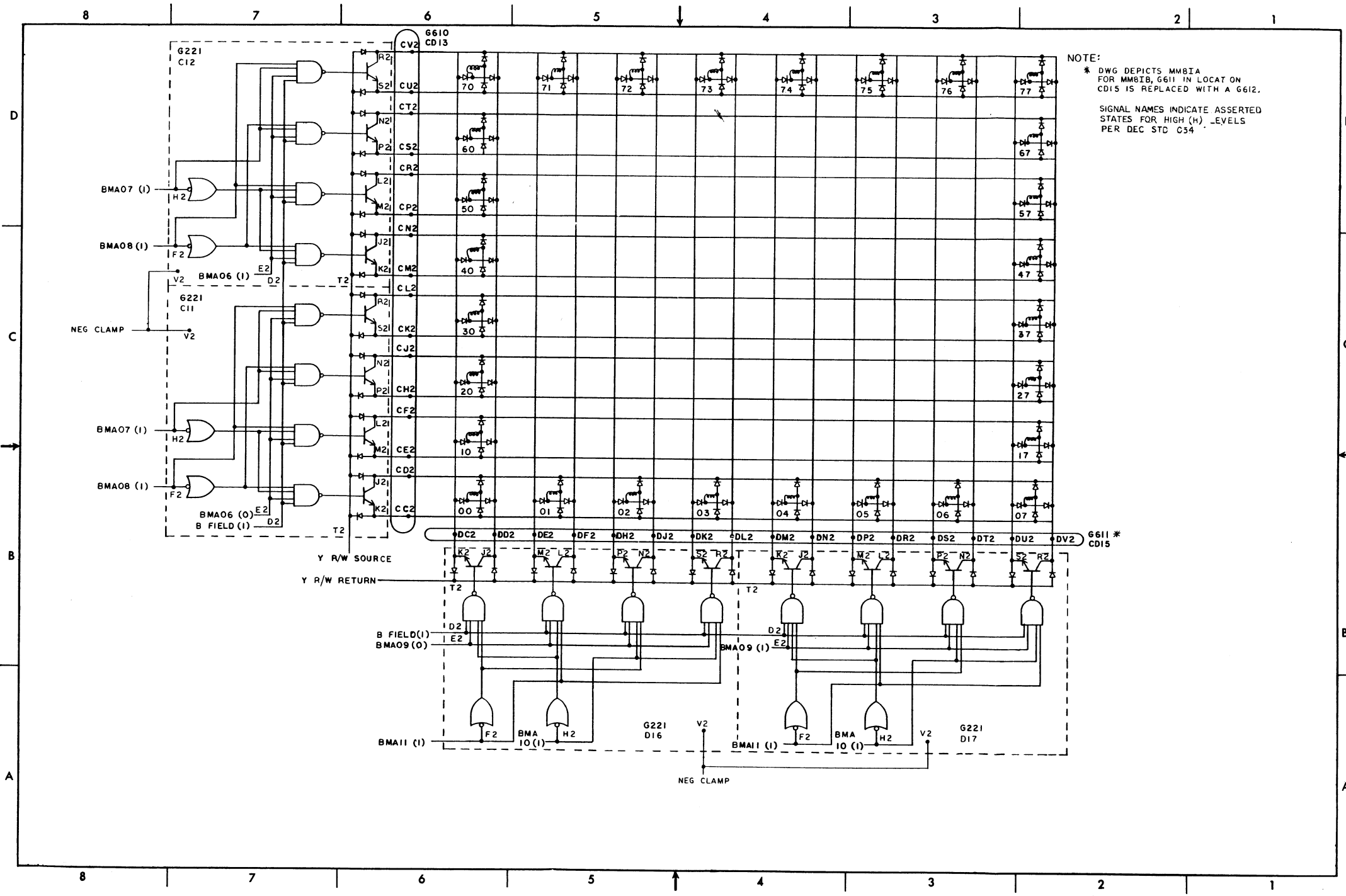
NOTES:
 1. DRAWING DEPICTS MC81-B
 2. FOR MC81-A REMOVE
 G228 IN LOCATION A37
 3. SIGNAL NAMES INDICATE
 ASSERTED STATES FOR HIGH (H)
 LEVELS PER DEC STD 054

D-BS-MC81-0-2 Inhibit Drivers



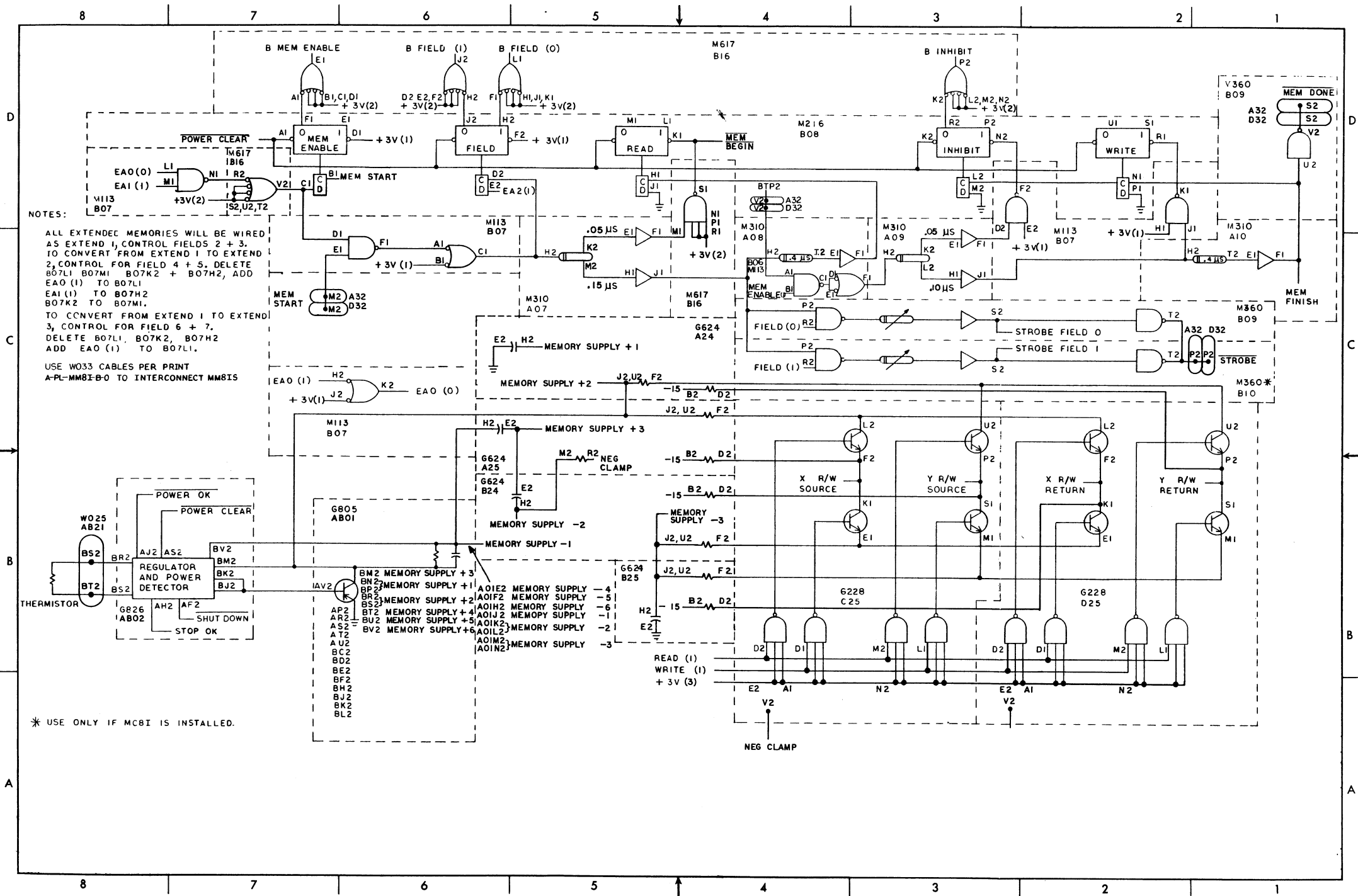
- NOTES:
 1. DRAWING DEPICTS MC8-A
 2. FOR MC8-B, G611 A
 LOCATION CD29 S
 REPLACED WITH A G612
 3. SIGNAL NAMES INDICATE
 ASSERTED STATES FOR HIGH(H)
 LEVELS PER DEC STD 054

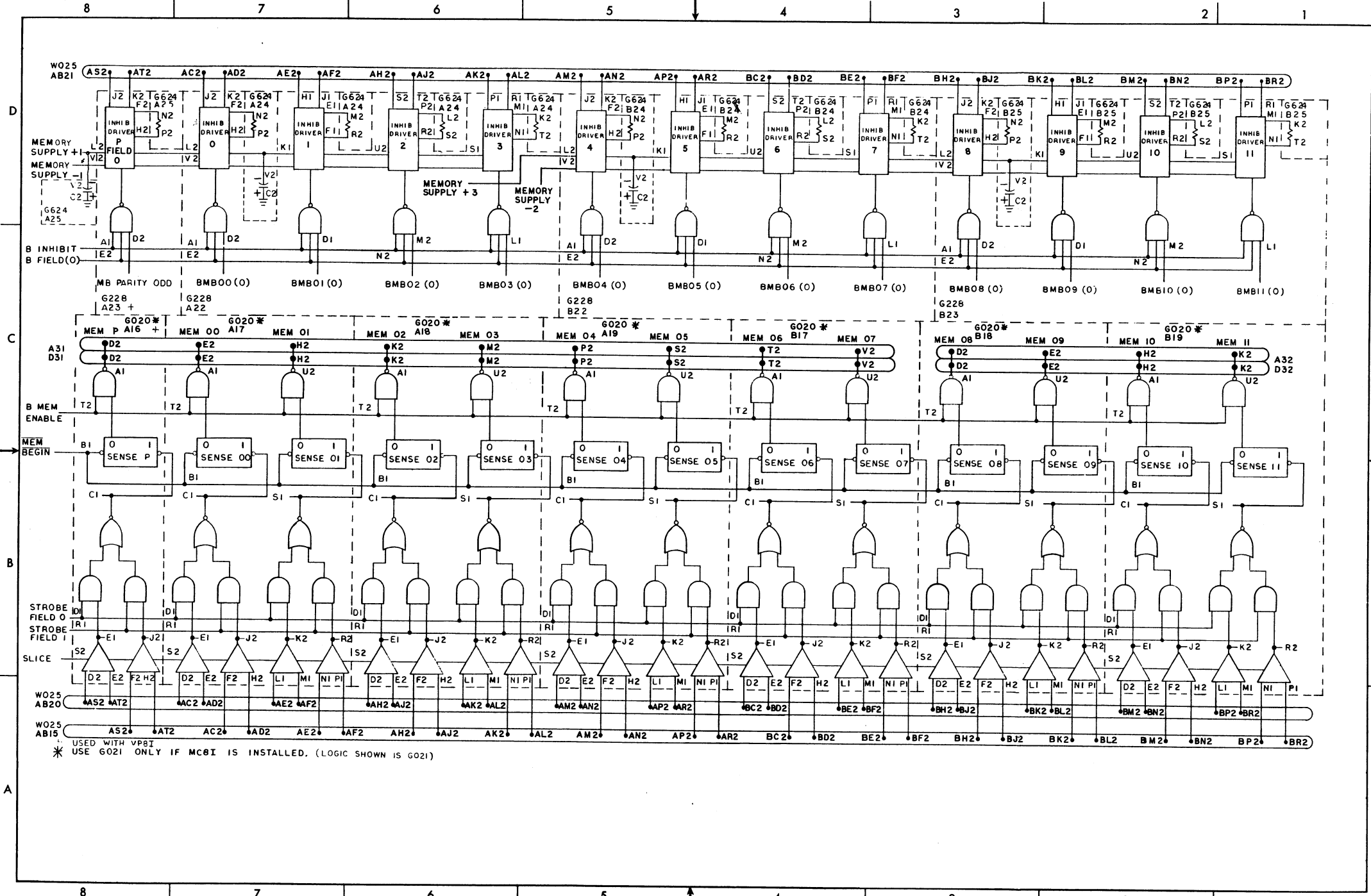
D-BS-MC8I-0-3 X Axis Selection



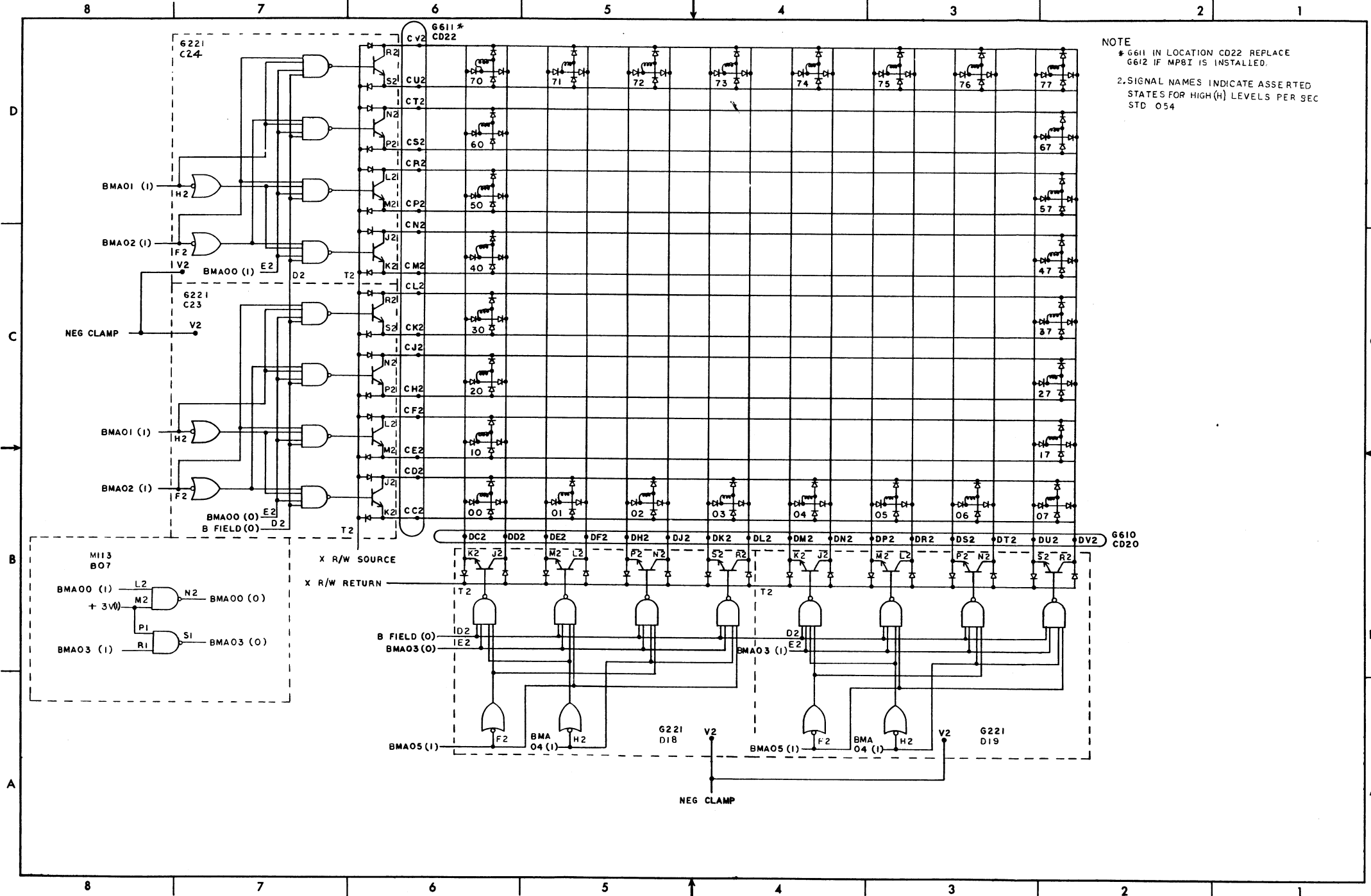
NOTE:
 * DWG DEPICTS MM8IA FOR MM8IB, G611 IN LOCAT ON CD15 IS REPLACED WITH A G612.
 SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH (H) LEVELS PER DEC STD G34

D-BS-MC8I-0-4 Y Axis Selection

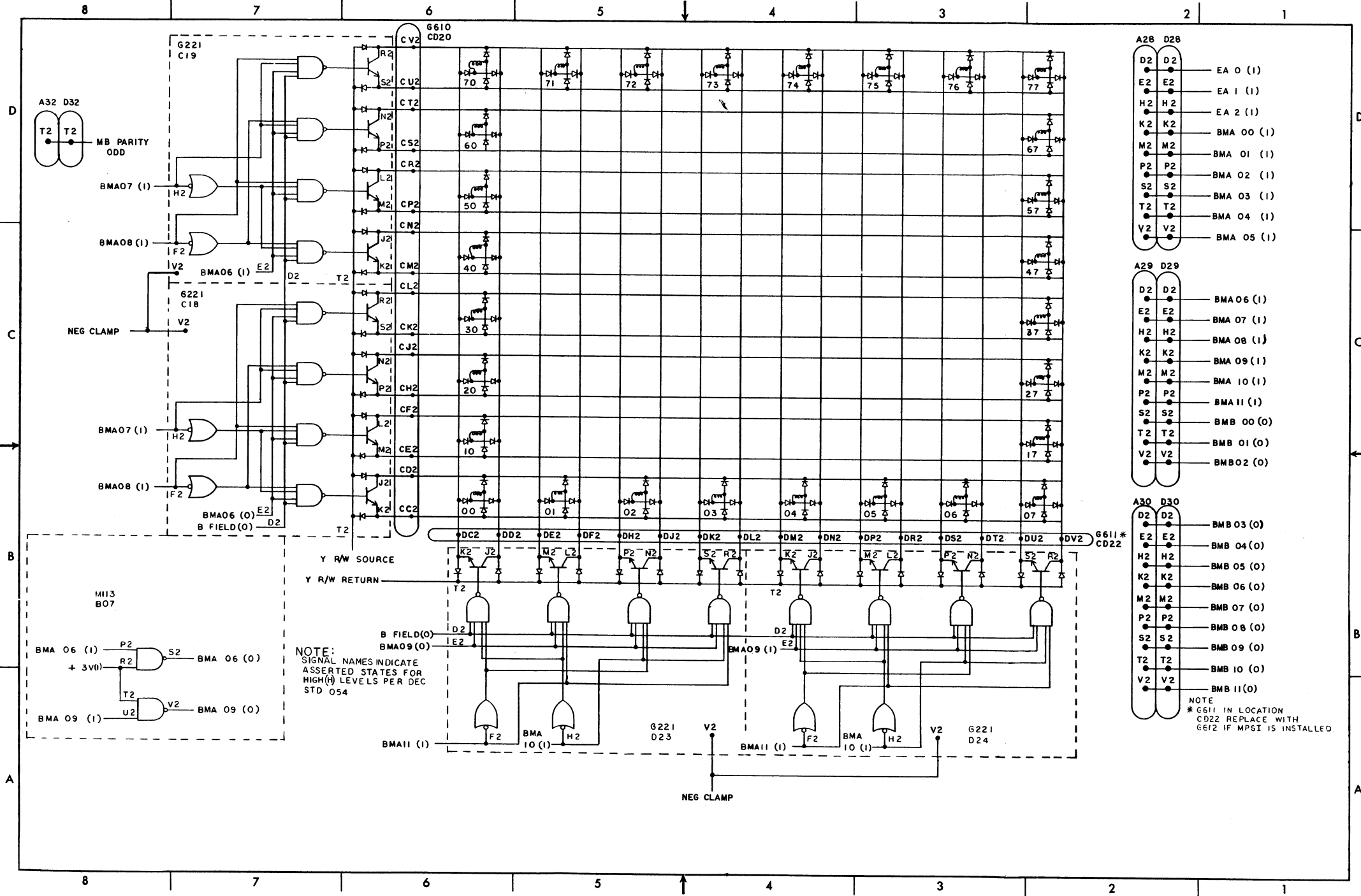




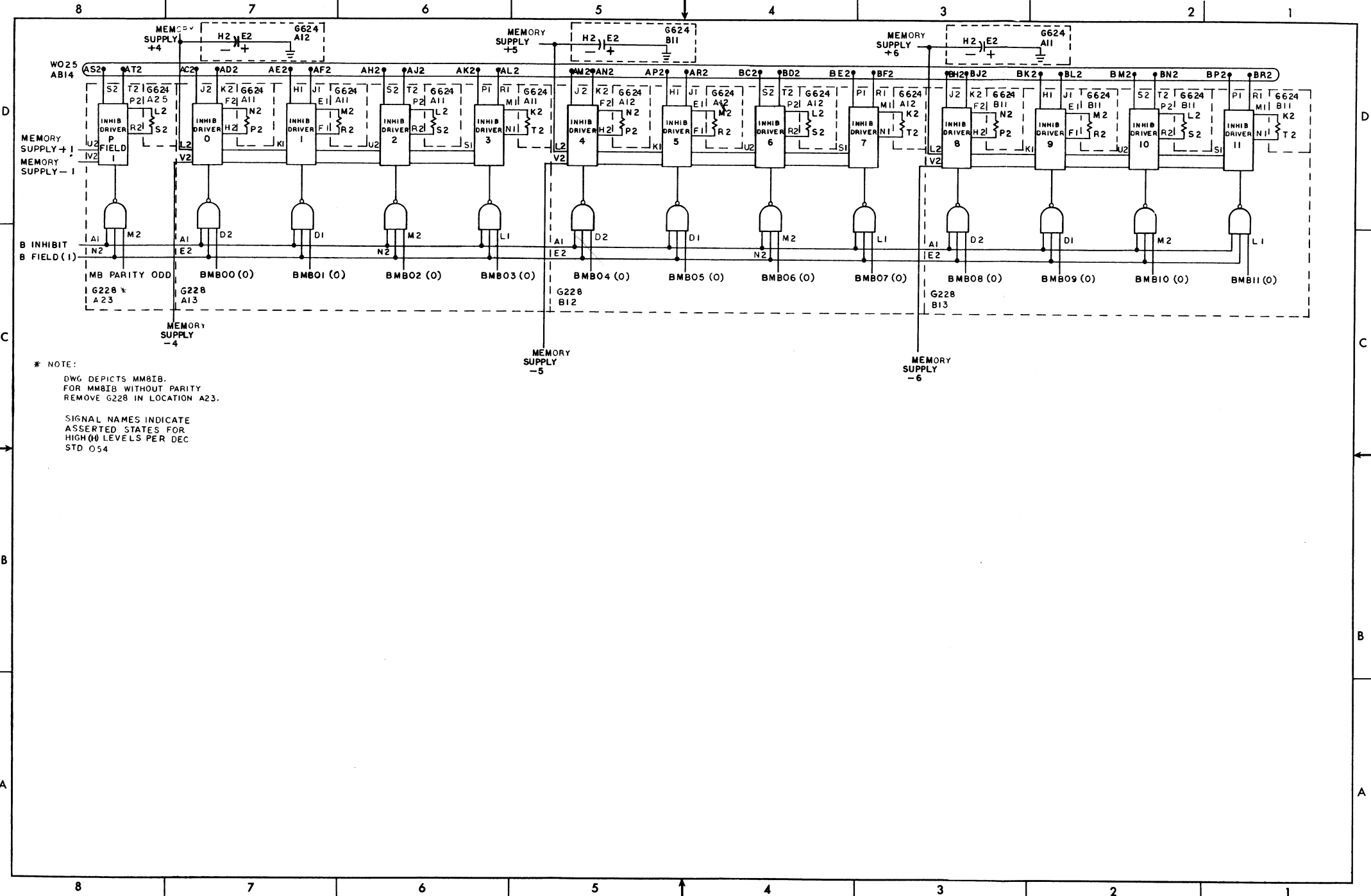
D-BS-MM8I-A-2 Sense Amplifiers and Inhibit Drivers



NOTE
 * 6611 IN LOCATION CD22 REPLACE
 6612 IF MP81 IS INSTALLED.
 2. SIGNAL NAMES INDICATE ASSERTED
 STATES FOR HIGH (H) LEVELS PER SEC
 STD 054

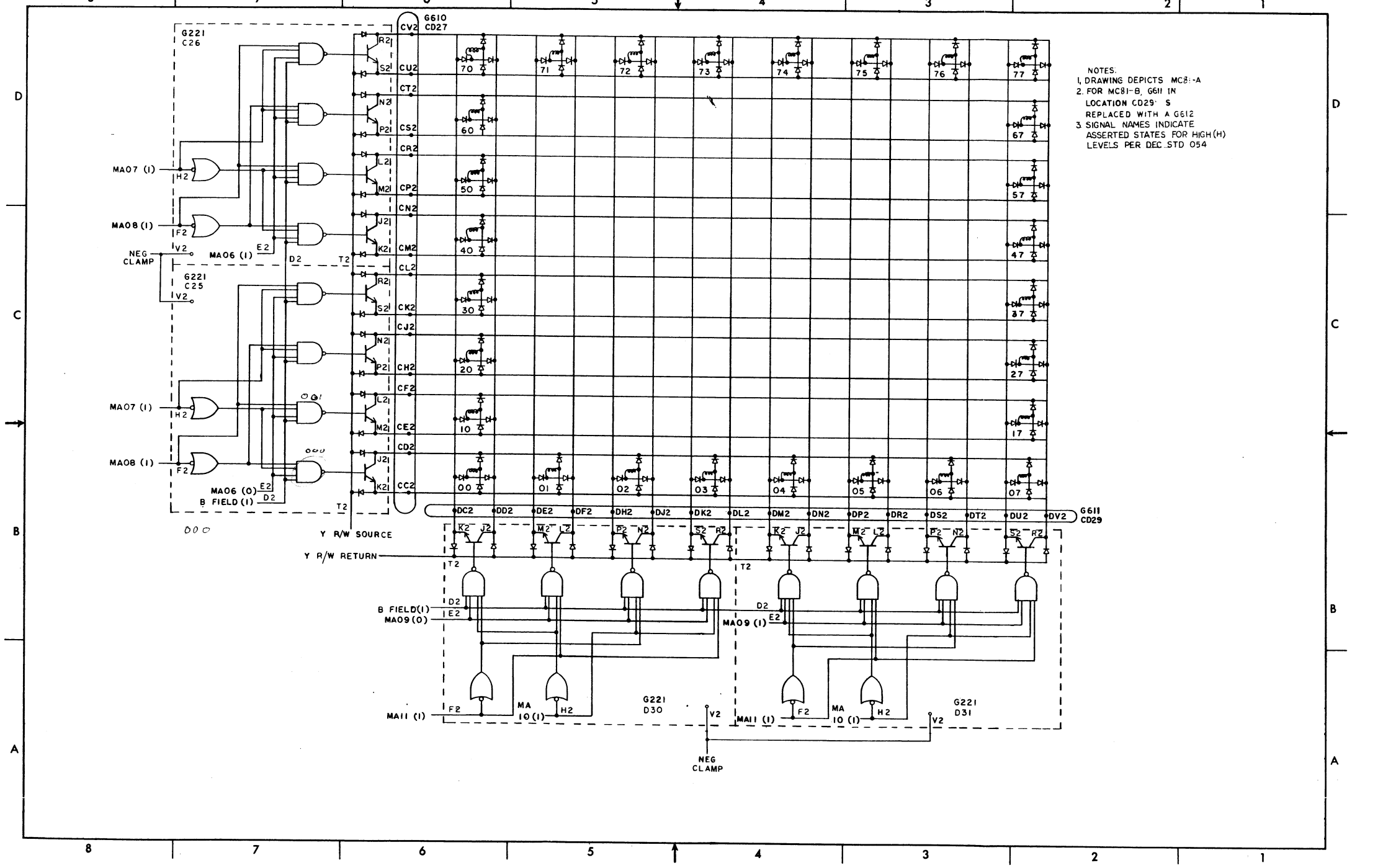


D-BS-MM81-A-4 Y Axis Selection, Field 0



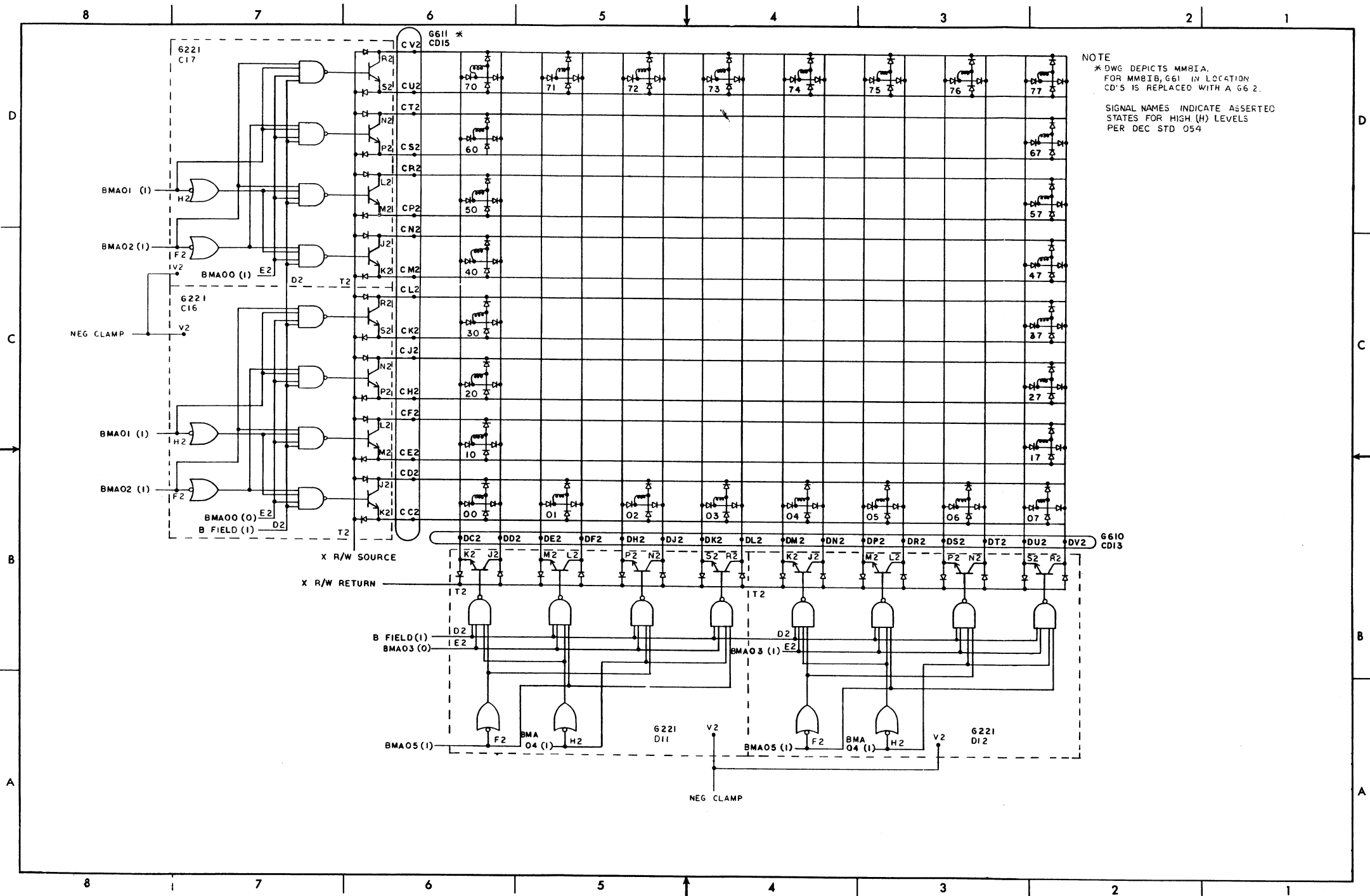
* NOTE:
 DWG DEPICTS MM8IB.
 FOR MM8IB WITHOUT PARITY
 REMOVE G228 IN LOCATION A23.

SIGNAL NAMES INDICATE
 ASSERTED STATES FOR
 HIGH (H) LEVELS PER DEC
 STD 054



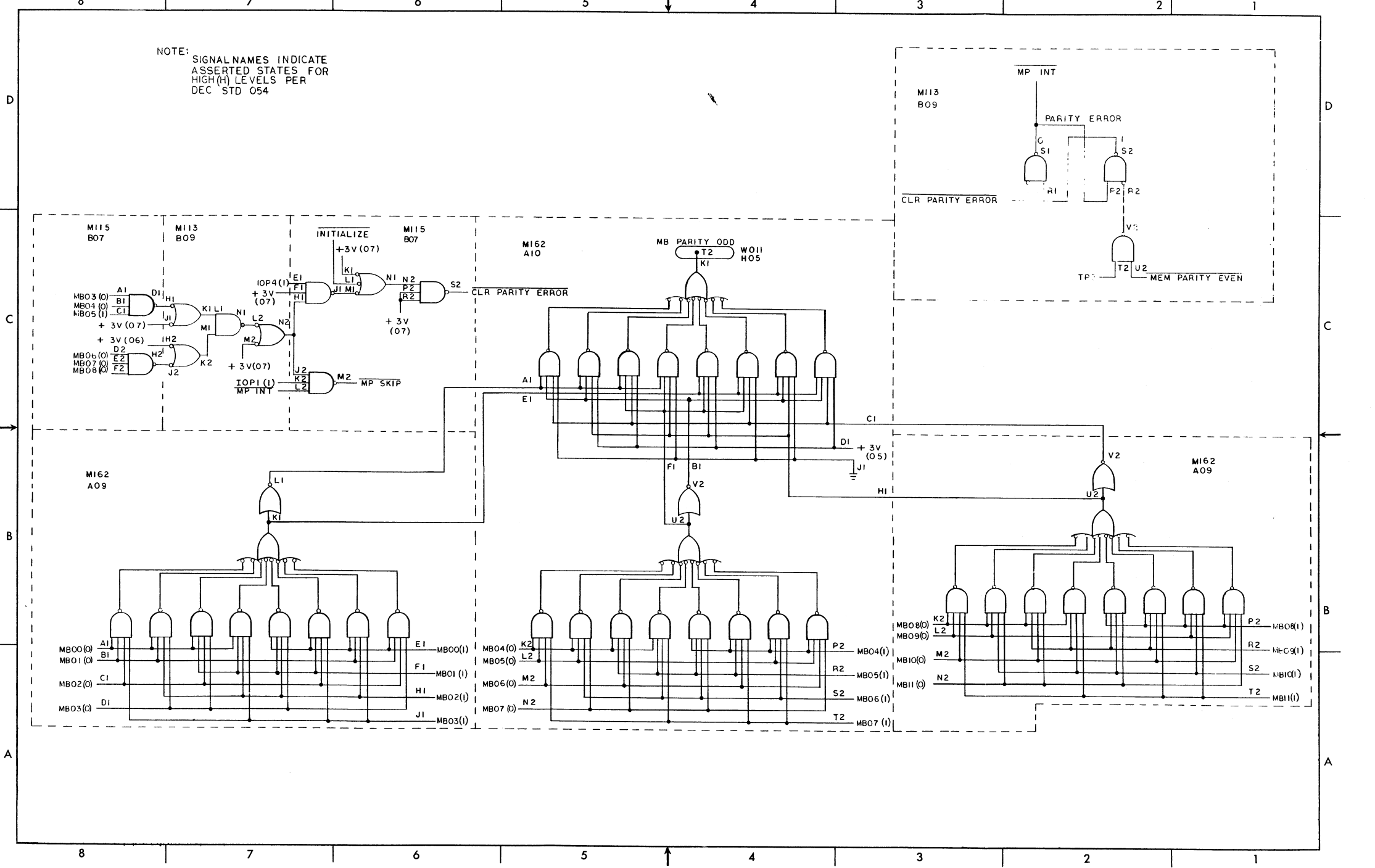
NOTES:
 1. DRAWING DEPICTS MC81-A
 2. FOR MC81-B, 6611 IN
 LOCATION CD29: S
 REPLACED WITH A 6612
 3. SIGNAL NAMES INDICATE
 ASSERTED STATES FOR HIGH (H)
 LEVELS PER DEC STD 054

D-BS-MM81-B-2 X Axis Selection, Field 1



NOTE
 * DWG DEPICTS MM8IA.
 FOR MM8IB, 661 IN LOCATION
 CD'5 IS REPLACED WITH A 662.
 SIGNAL NAMES INDICATE ASSERTED
 STATES FOR HIGH (H) LEVELS
 PER DEC STD 054

NOTE:
SIGNAL NAMES INDICATE
ASSERTED STATES FOR
HIGH(H) LEVELS PER
DEC STD 054



8 7 6 5 4 3 2 1

D

D

C

C

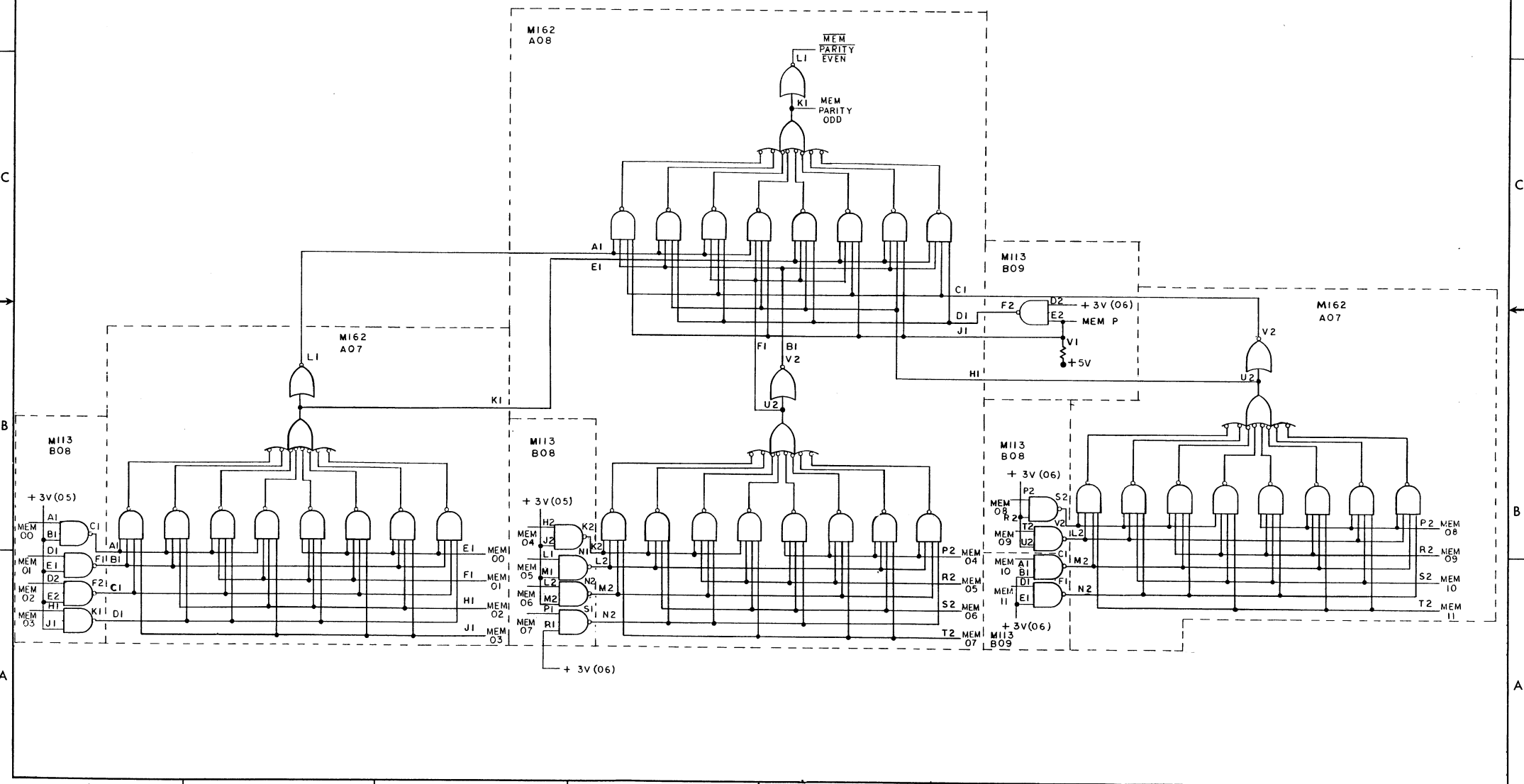
B

B

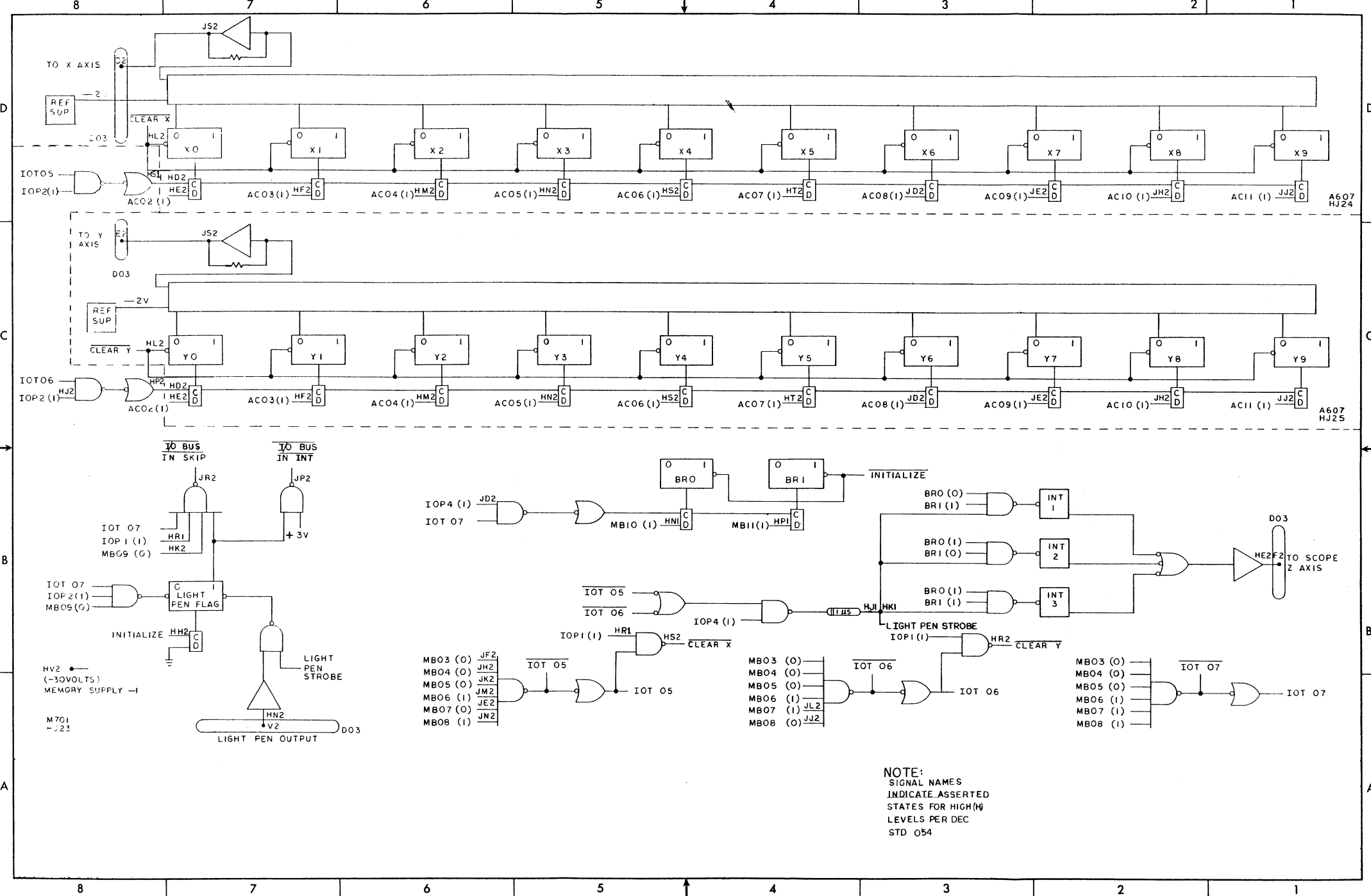
A

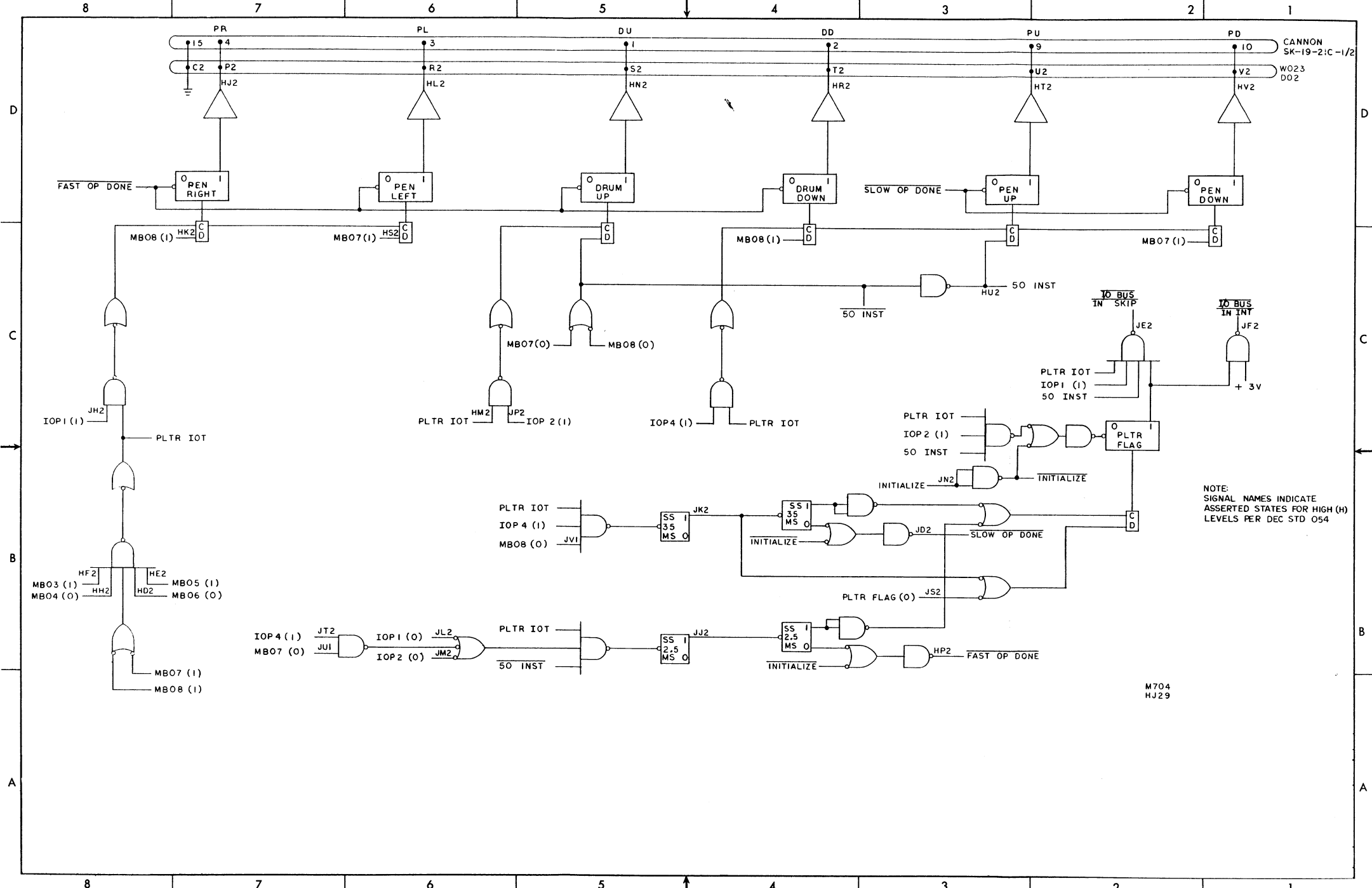
A

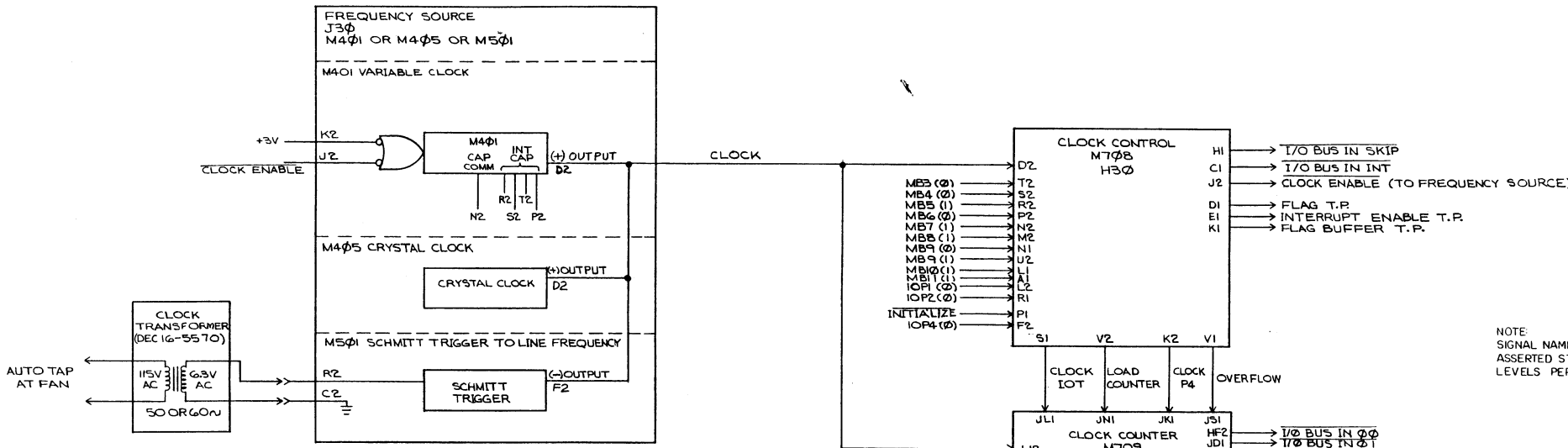
NOTE:
SIGNAL NAMES INDICATE ASSERTED STATES
FOR HIGH LEVELS PER DEC STD 054



8 7 6 5 4 3 2 1





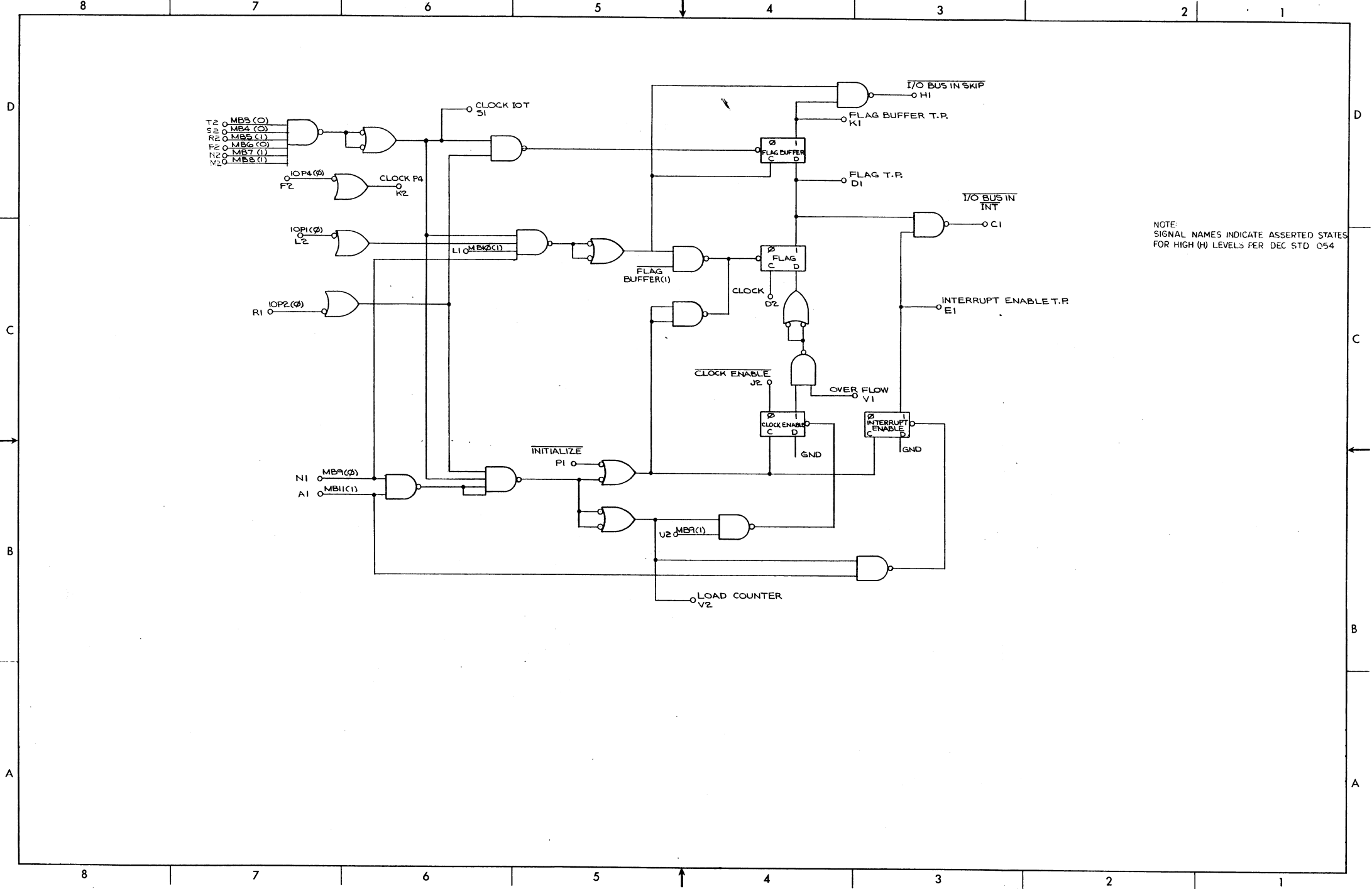


NOTE:
SIGNAL NAMES INDICATE
ASSERTED STATES FOR HIGH (H)
LEVELS PER DEC STD 054

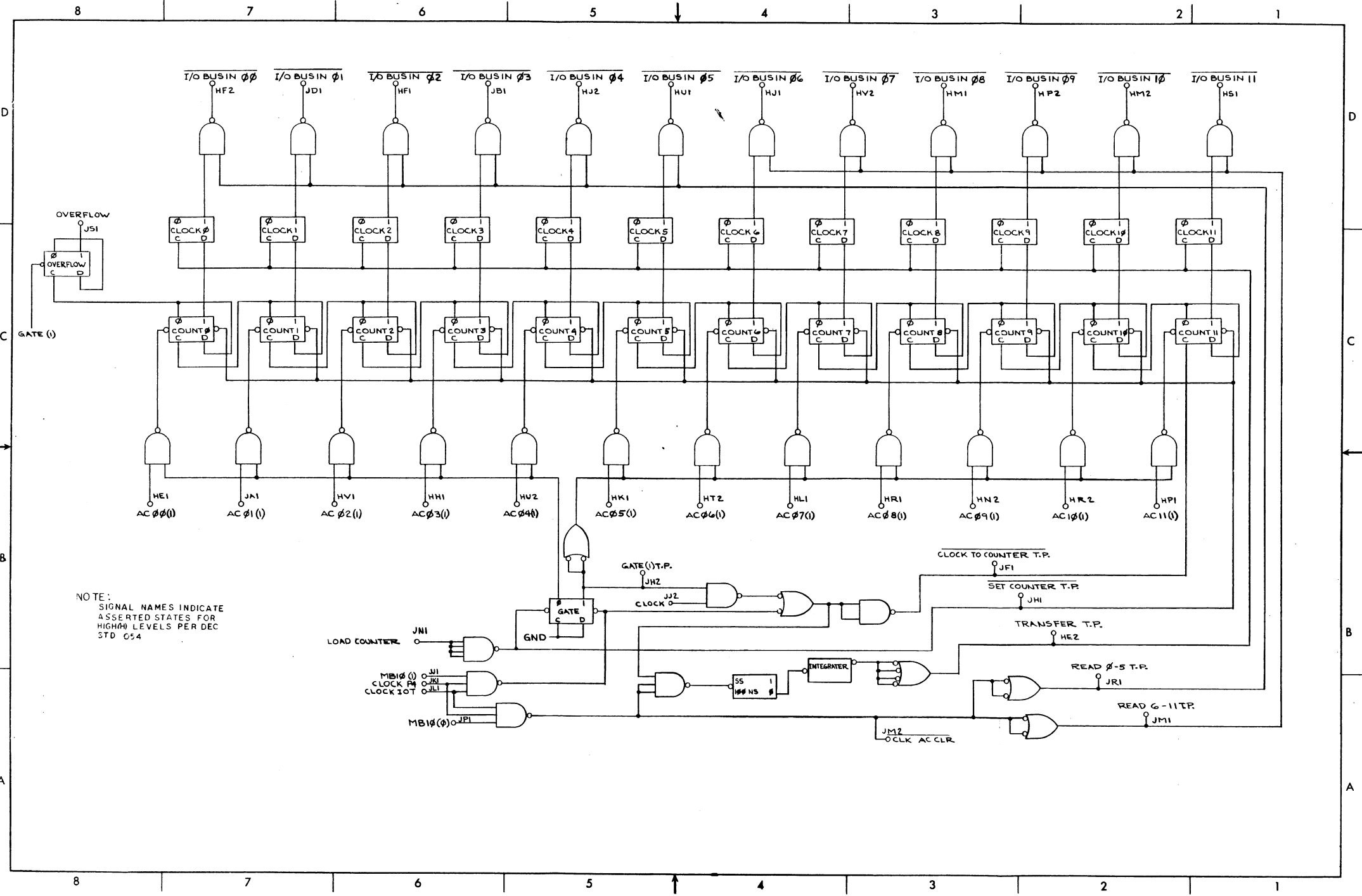
THE FOLLOWING CONFIGURATIONS OF THE REAL TIME CLOCK OPTION ARE POSSIBLE :

OPTION TYPE	DESCRIPTION	MODULES	LOCATION
KWBIA	LINE FREQUENCY INTERRUPT	M708 M501	H30 J30
		CLOCK TRANSFORMER	FAN BRACKET#
KWBIB	VARIABLE CLOCK INTERRUPT	M708 M401	H30 J30
KWBIC	CRYSTAL CLOCK INTERRUPT	M708 M405	H30 J30
KWBID	KWBIA WITH PRESET AND READOUT	M708 M709 M501	H30 HJ31 J30
		CLOCK TRANSFORMER	FAN BRACKET*
KWBIE	KWBIB WITH PRESET AND READOUT	M708 M709 M401	H30 HJ31 J30
KWBIF	KWBIC WITH PRESET AND READOUT	M708 M709 M405	H30 HJ31 J30

* MTG & WIRING INFORMATION ON PRINT * D-UA-KWBI-0-0

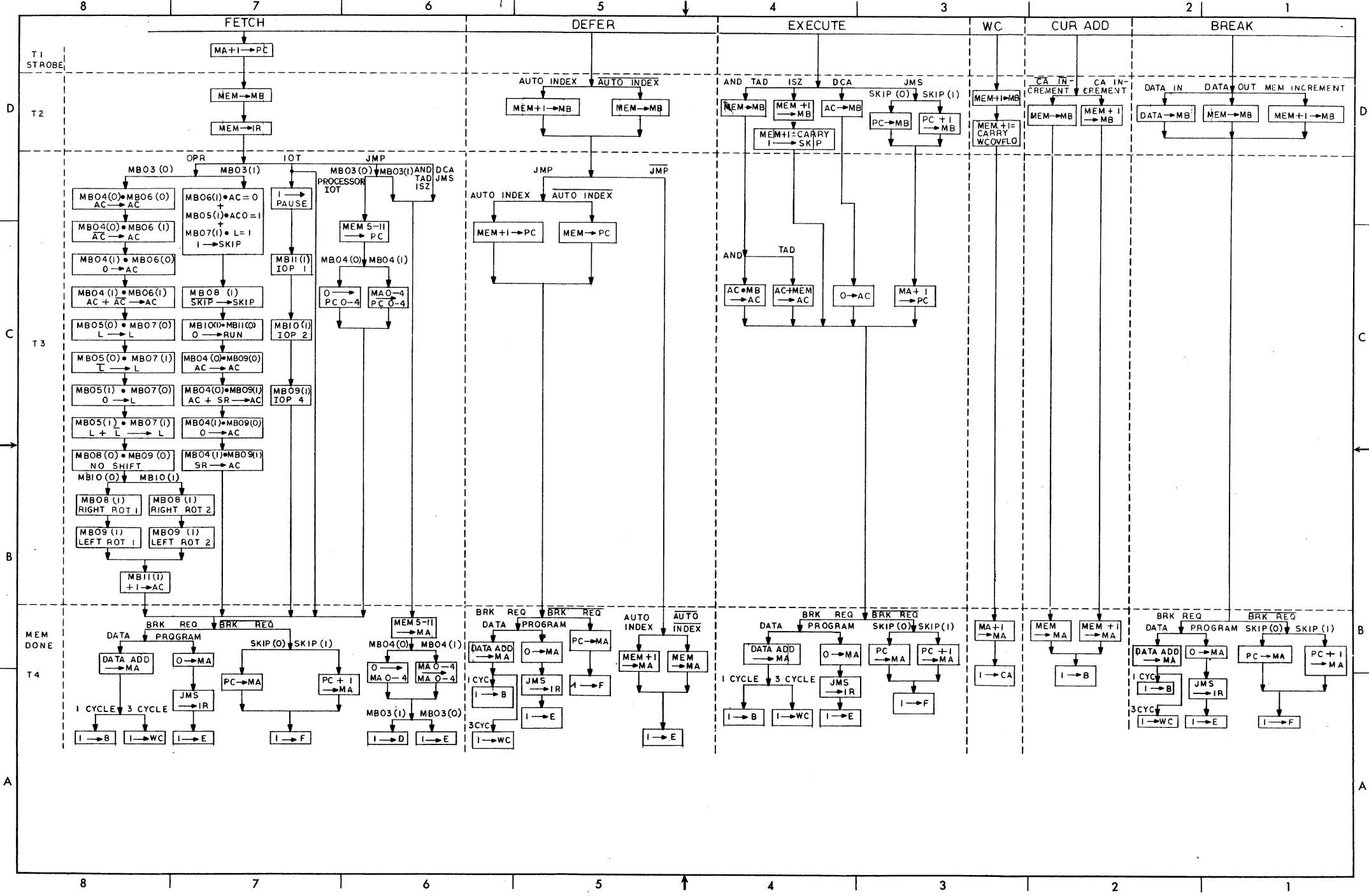


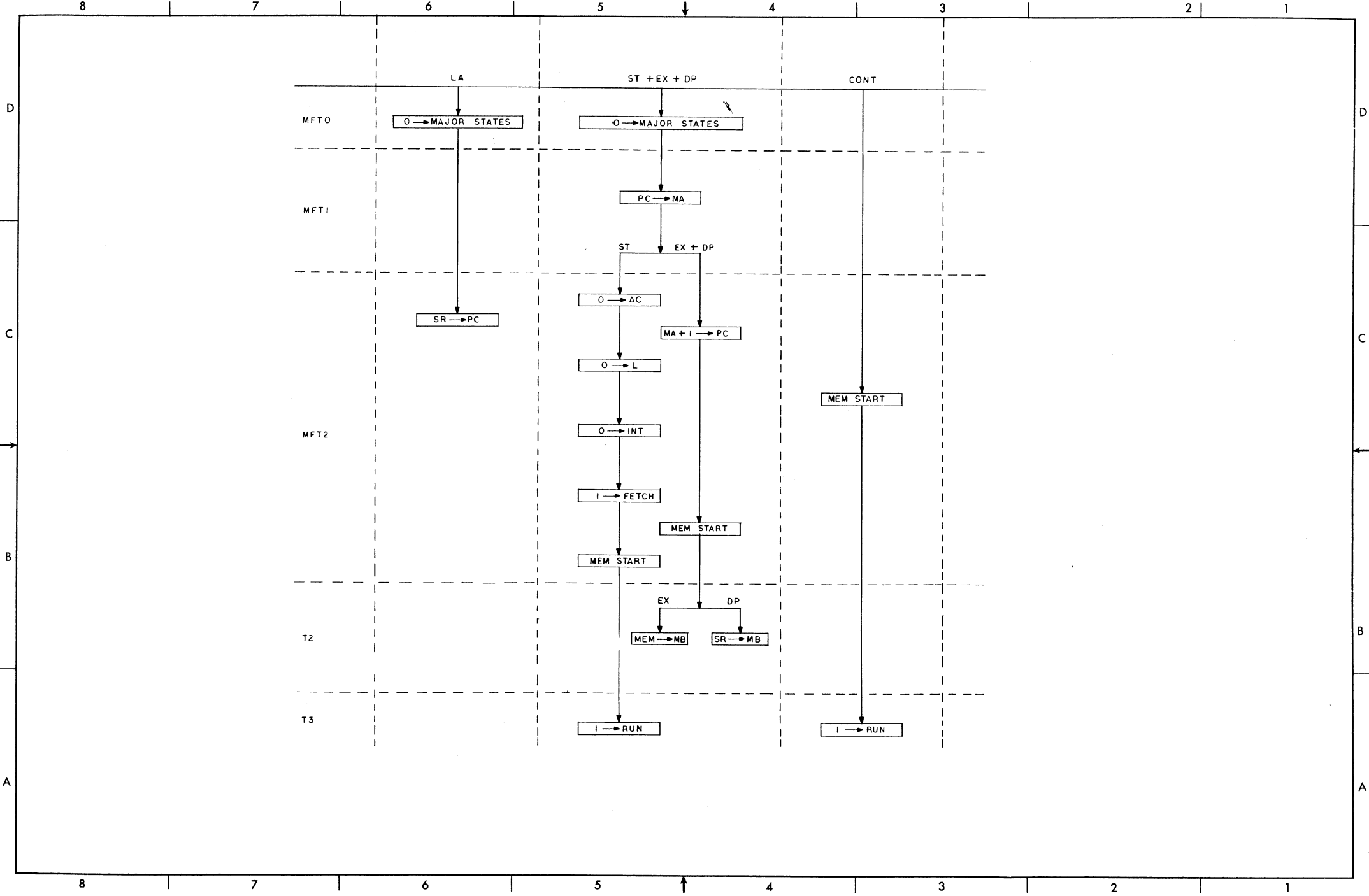
NOTE:
SIGNAL NAMES INDICATE ASSERTED STATES
FOR HIGH (H) LEVELS PER DEC STD 054

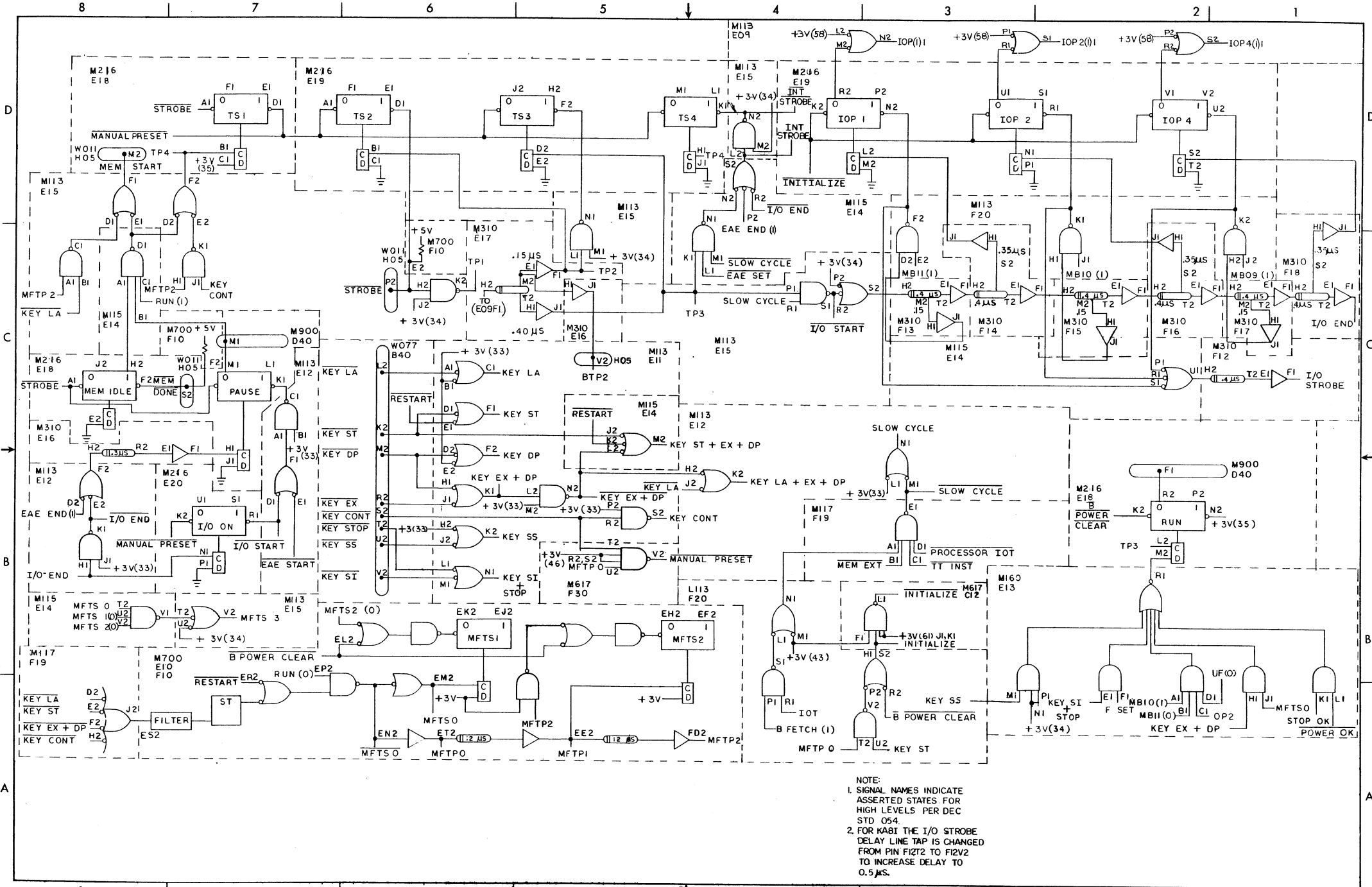


NOTE:
 SIGNAL NAMES INDICATE
 ASSERTED STATES FOR
 HIGH LEVELS PER DEC
 STD 054

D-BS-KW81-0-3 Clock Counter M709

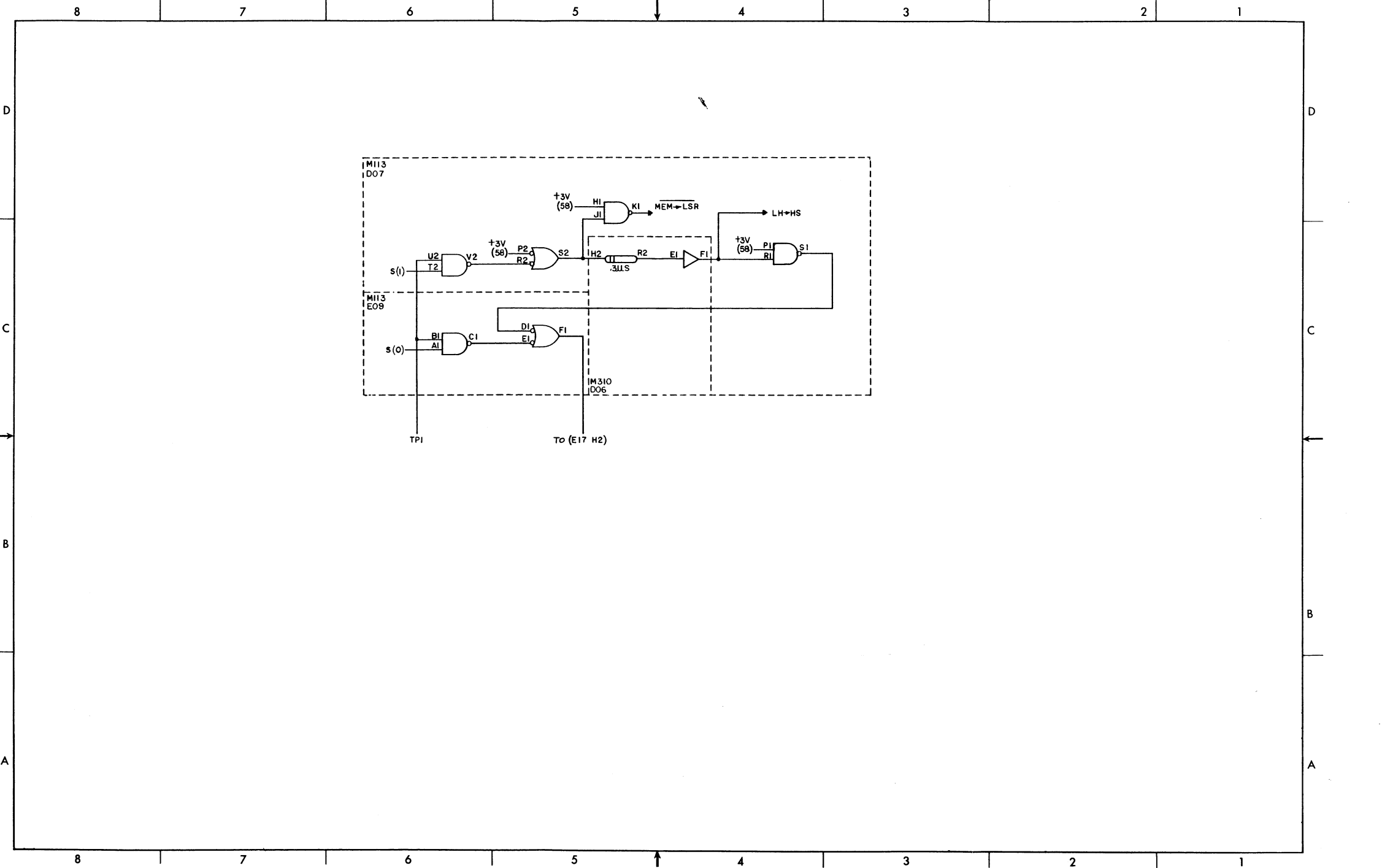


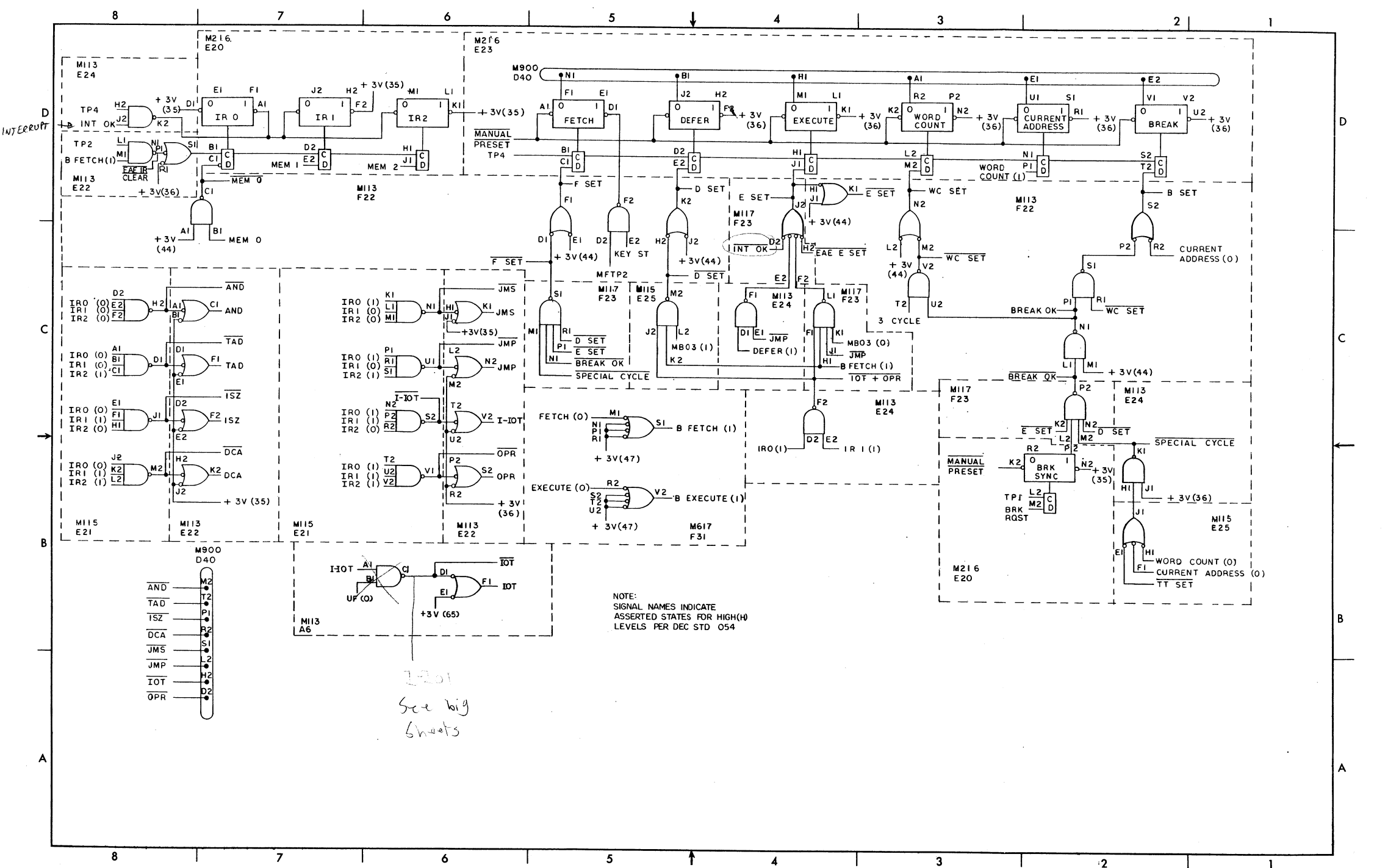


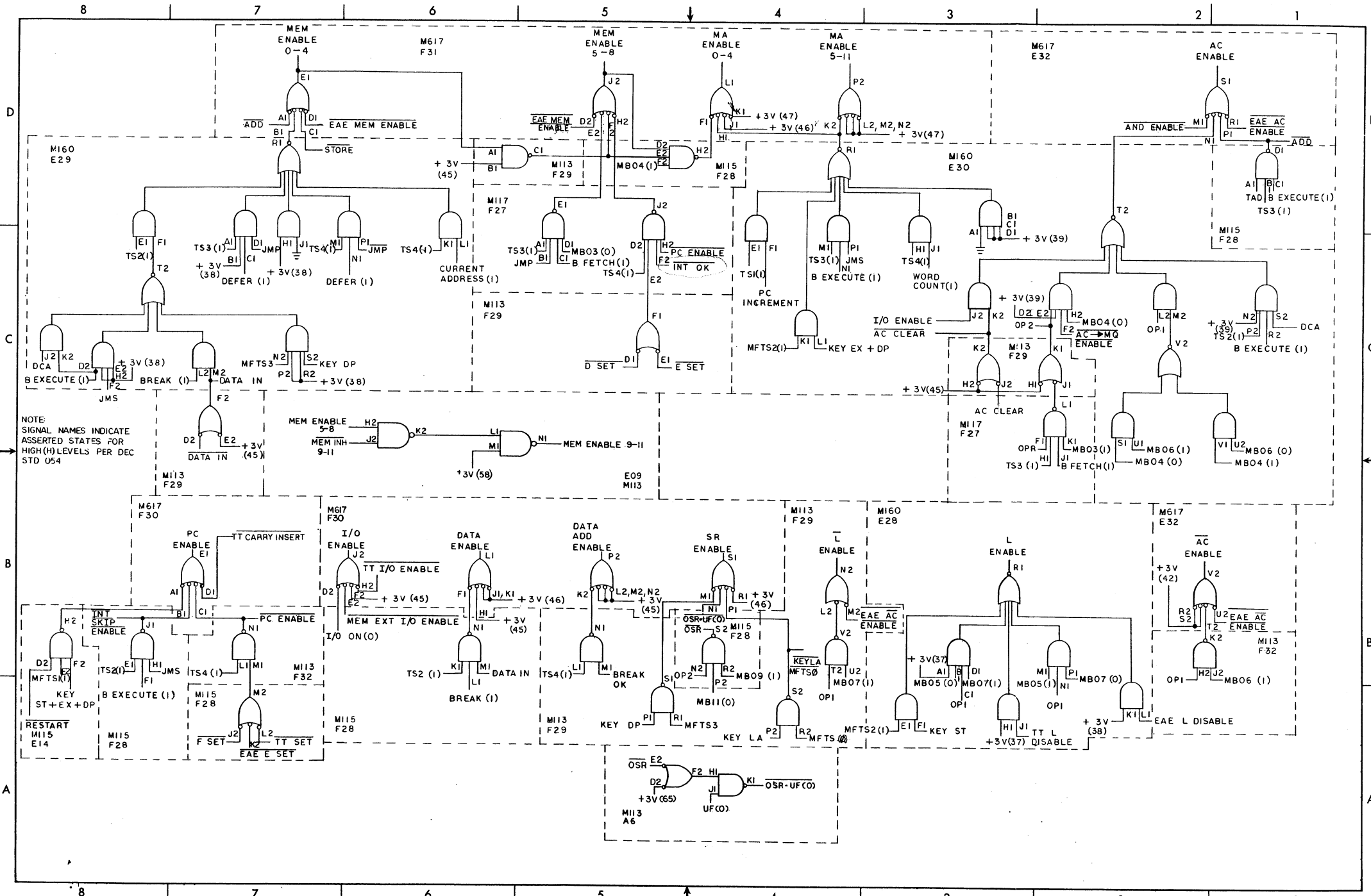


NOTE:
 1. SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH LEVELS PER DEC STD 054.
 2. FOR KABI THE I/O STROBE DELAY LINE TAP IS CHANGED FROM PIN F12T2 TO F12V2 TO INCREASE DELAY TO 0.5 μs.

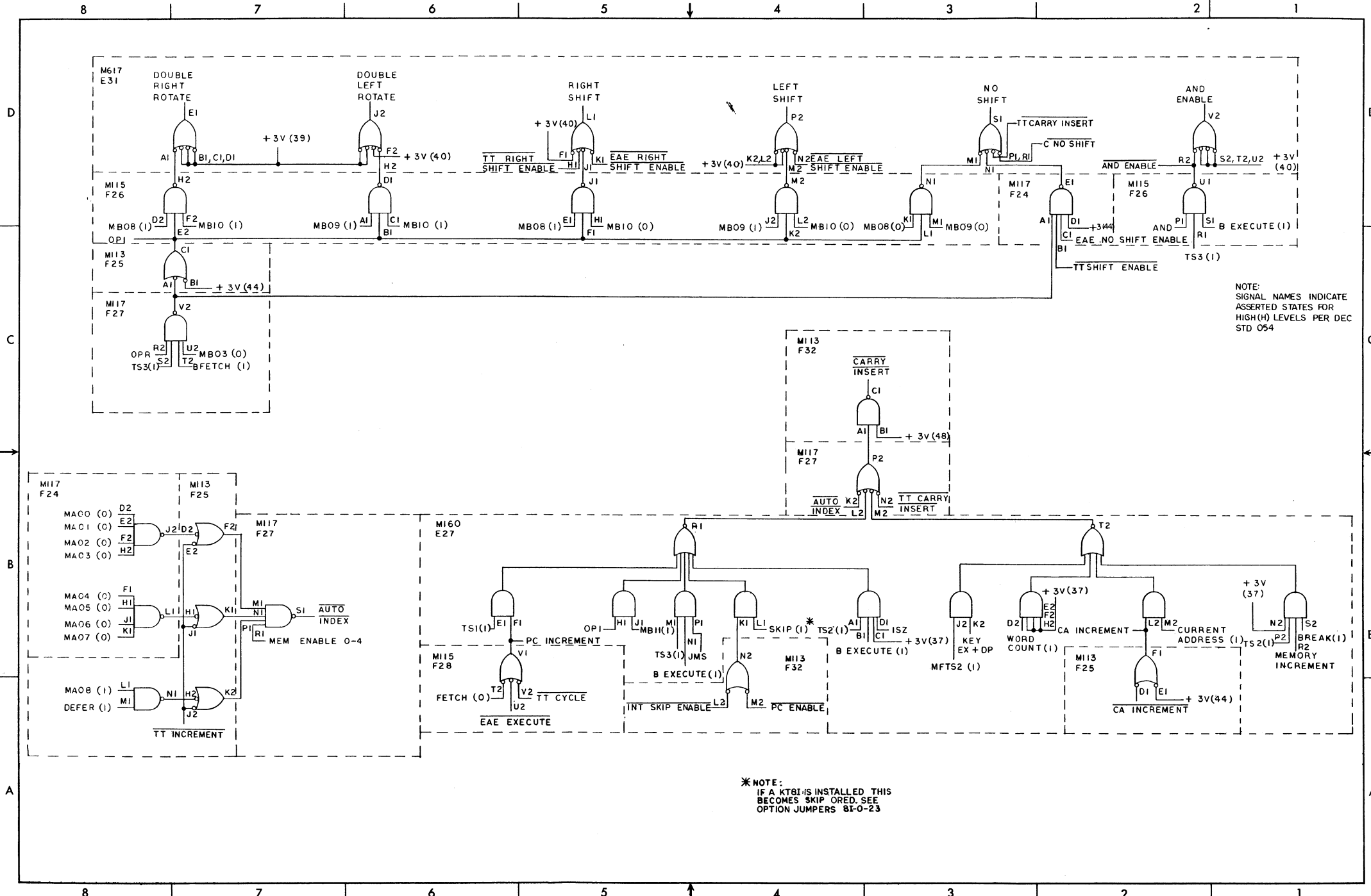
D-BS-81-0-2 Timing Manual Functions and Run (Sheet 1)



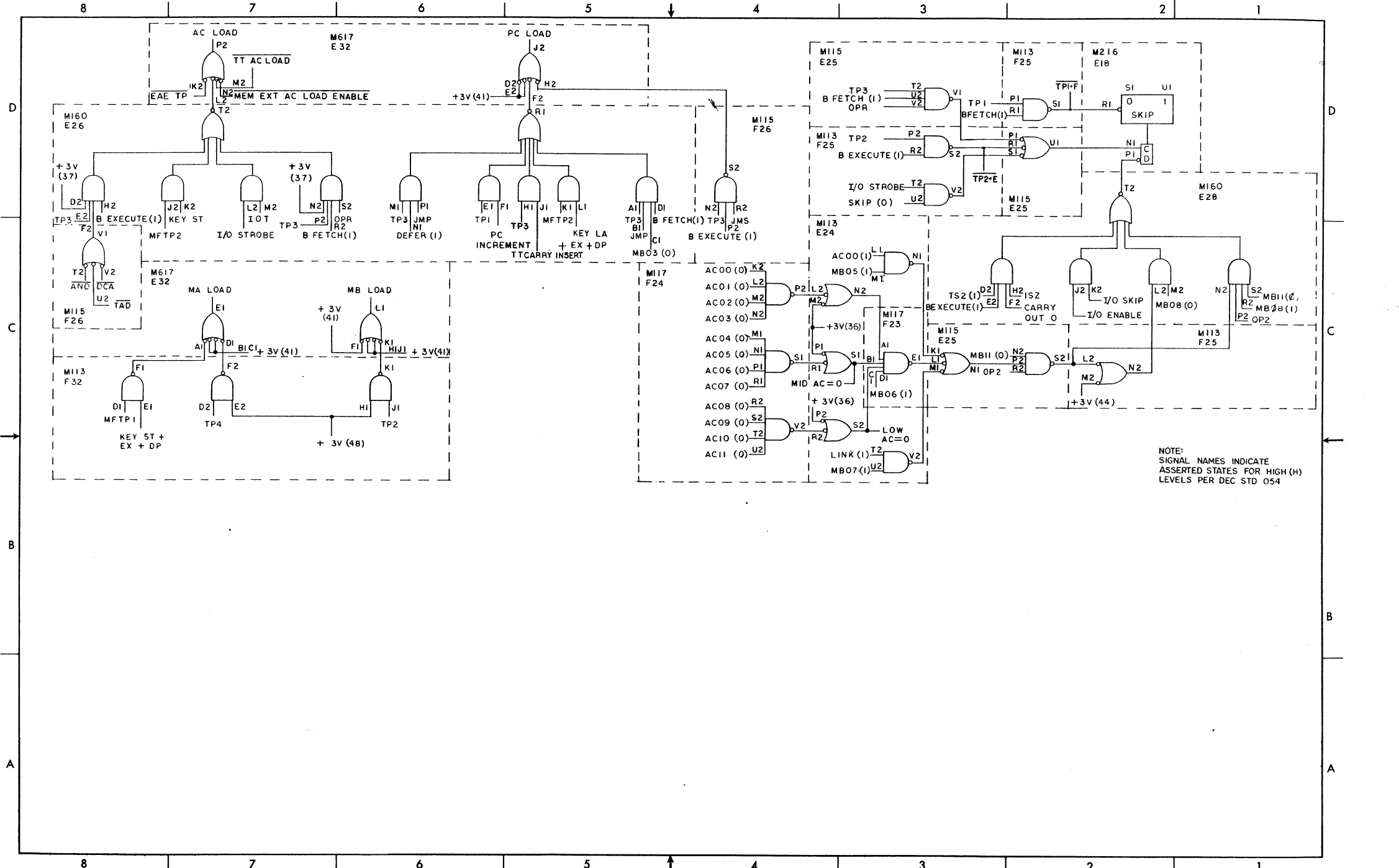




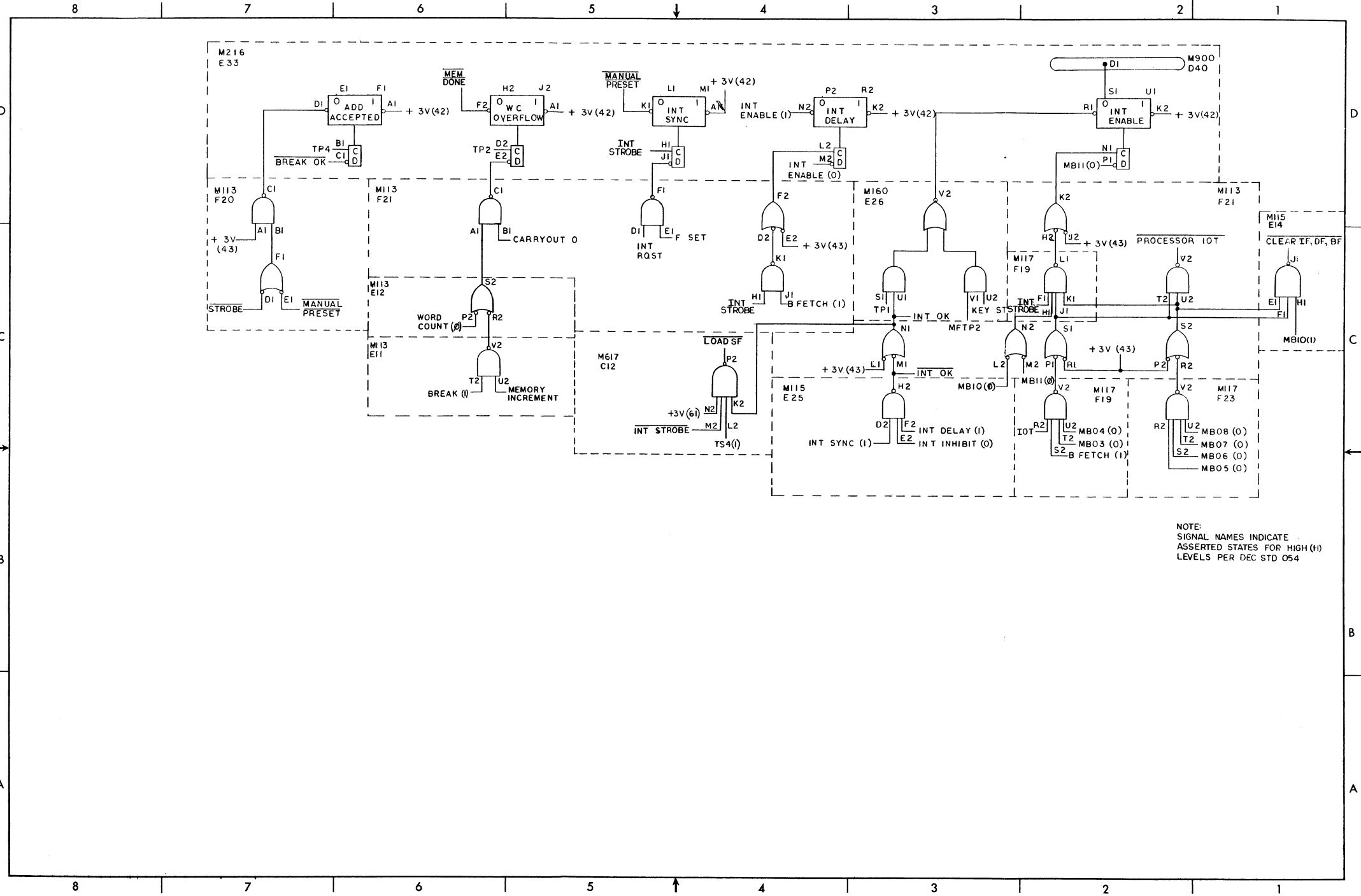
D-BS-8I-0-4 Register Output Gate Control



NOTE:
SIGNAL NAMES INDICATE
ASSERTED STATES FOR
HIGH(H) LEVELS PER DEC
STD 054

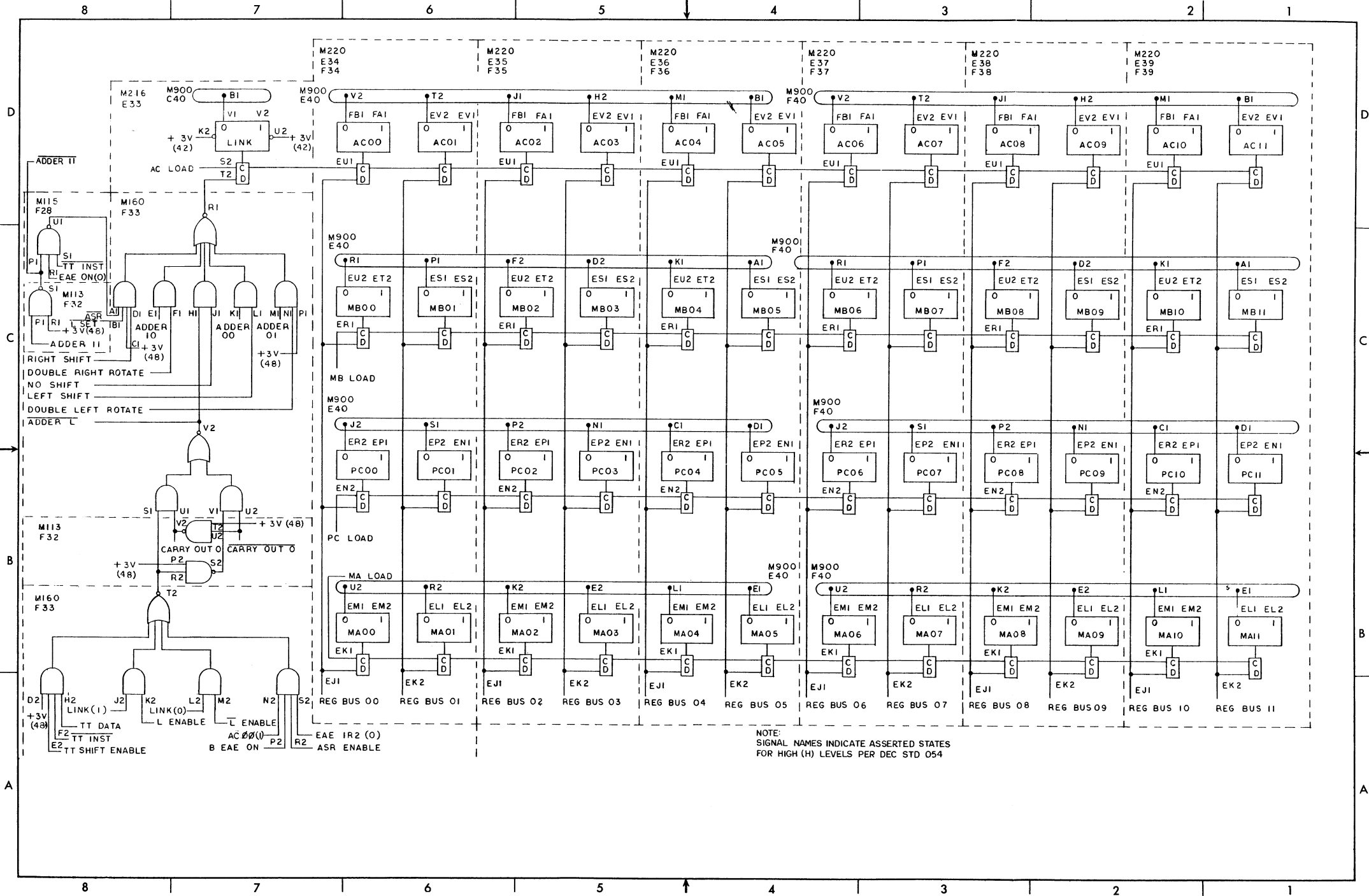


NOTE:
 SIGNAL NAMES INDICATE
 ASSERTED STATES FOR HIGH (H)
 LEVELS PER DEC STD 054

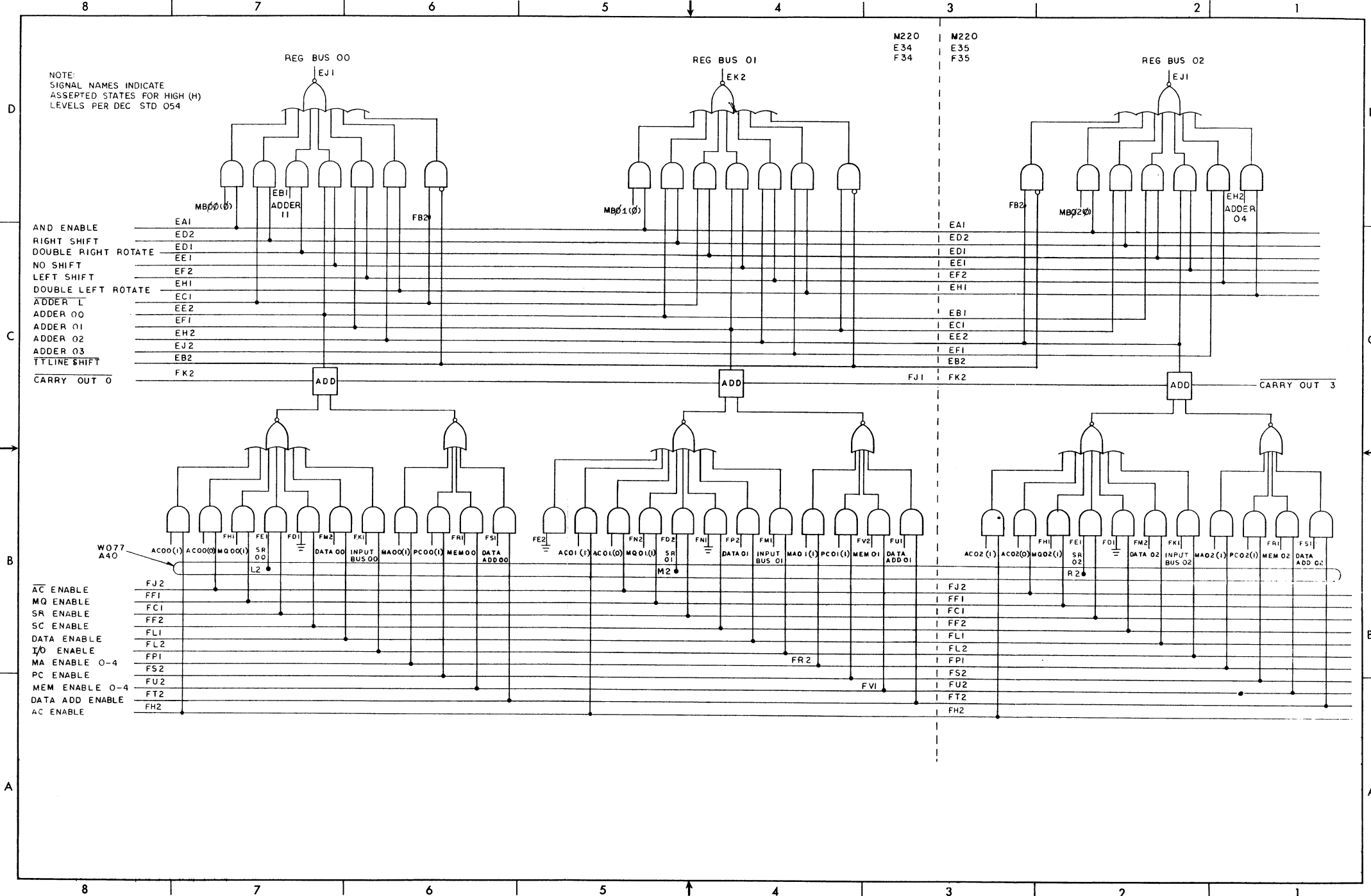


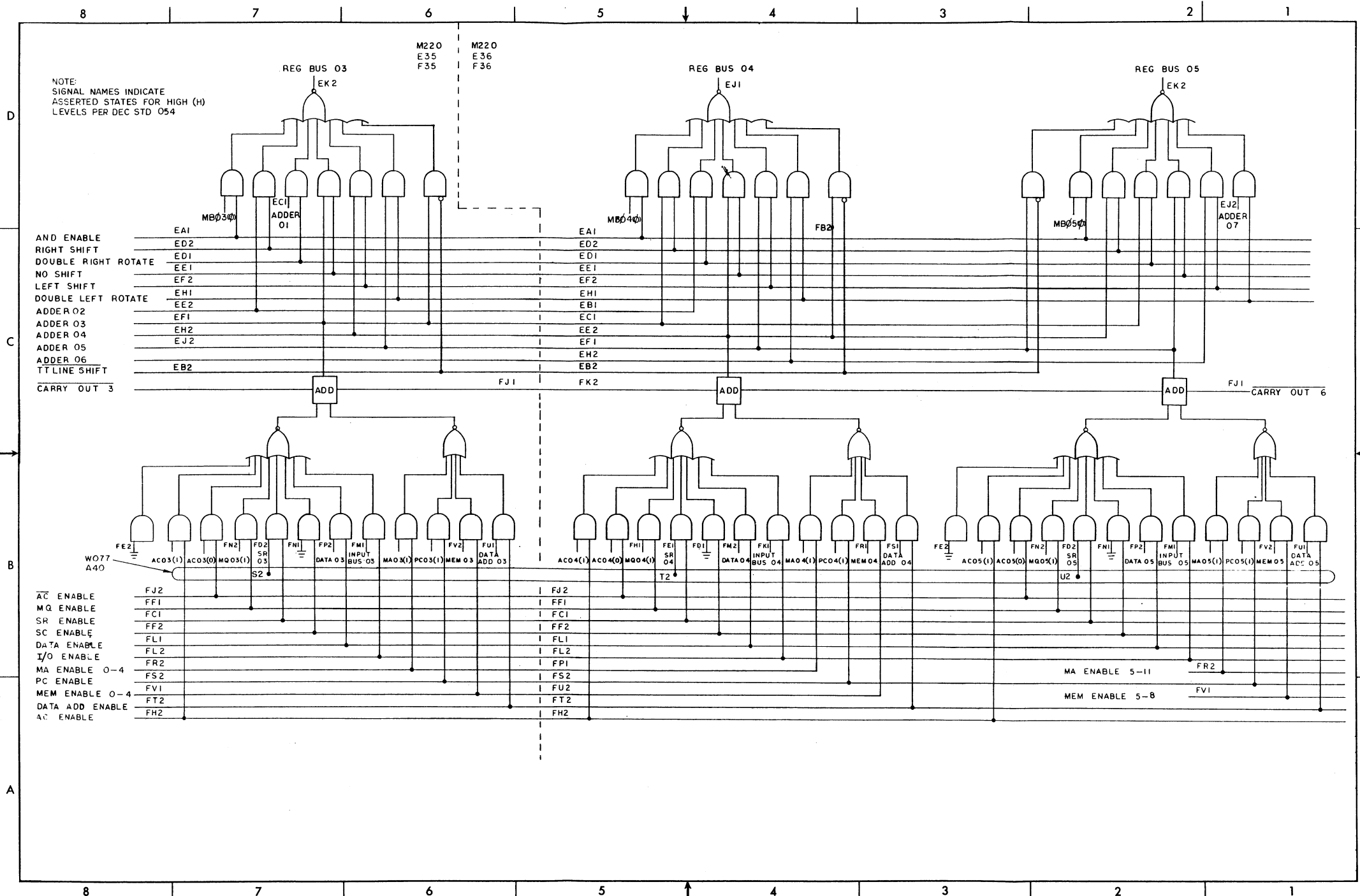
NOTE:
 SIGNAL NAMES INDICATE
 ASSERTED STATES FOR HIGH (H)
 LEVELS PER DEC STD 054

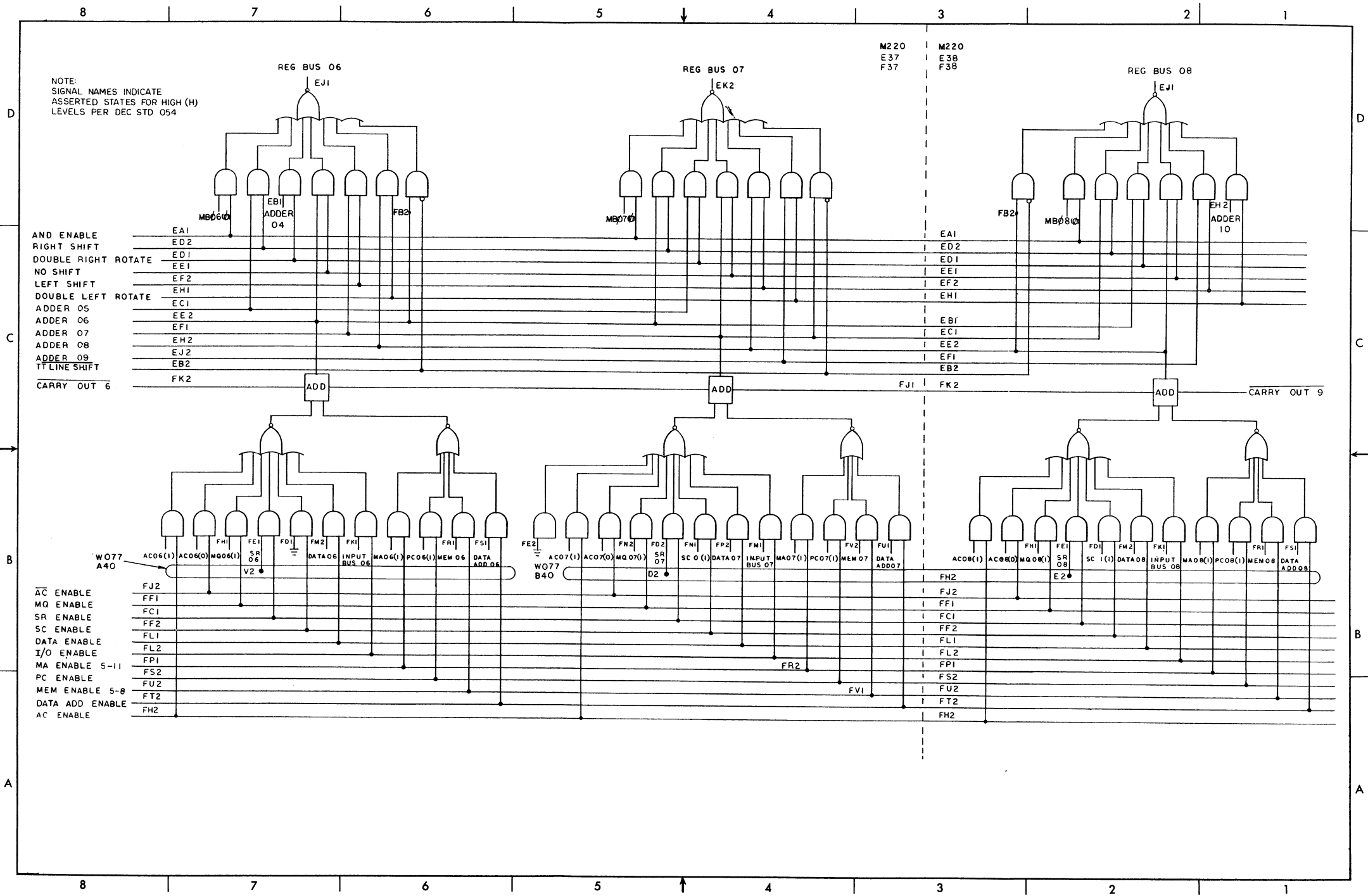
D-BS-8I-0-7 Interrupt and Break Control

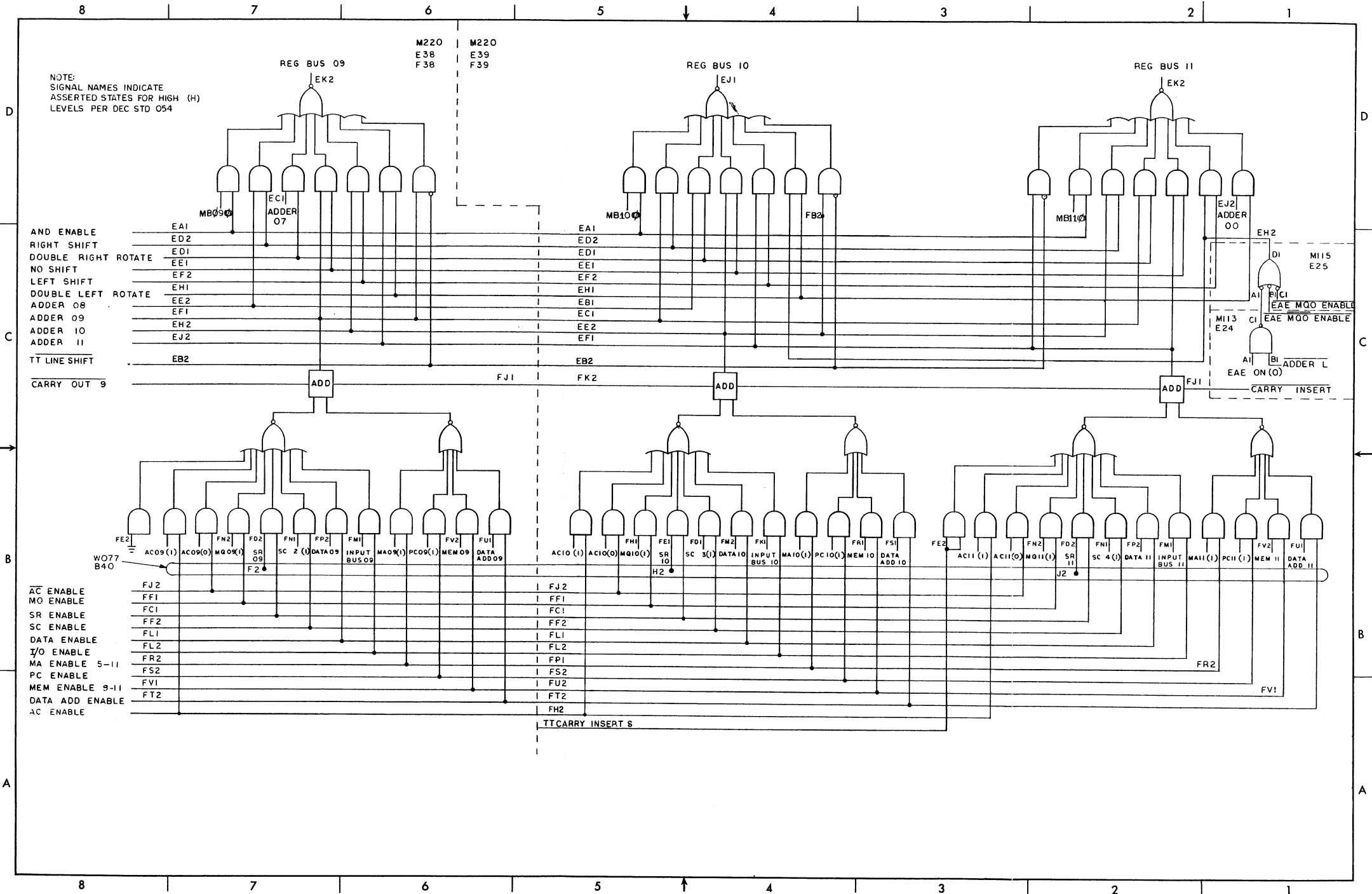


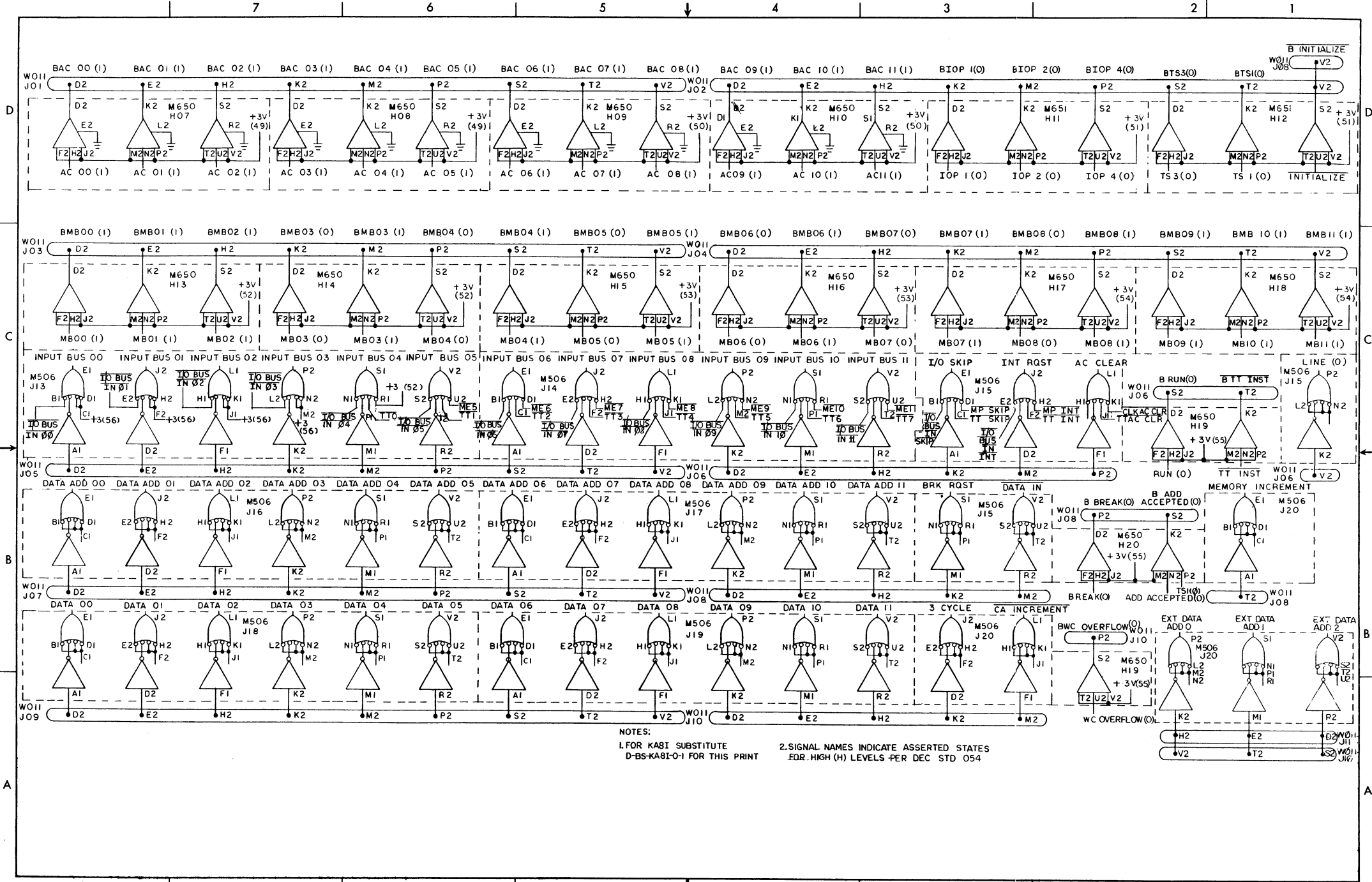
D-BS-8I-0-8 Major Registers







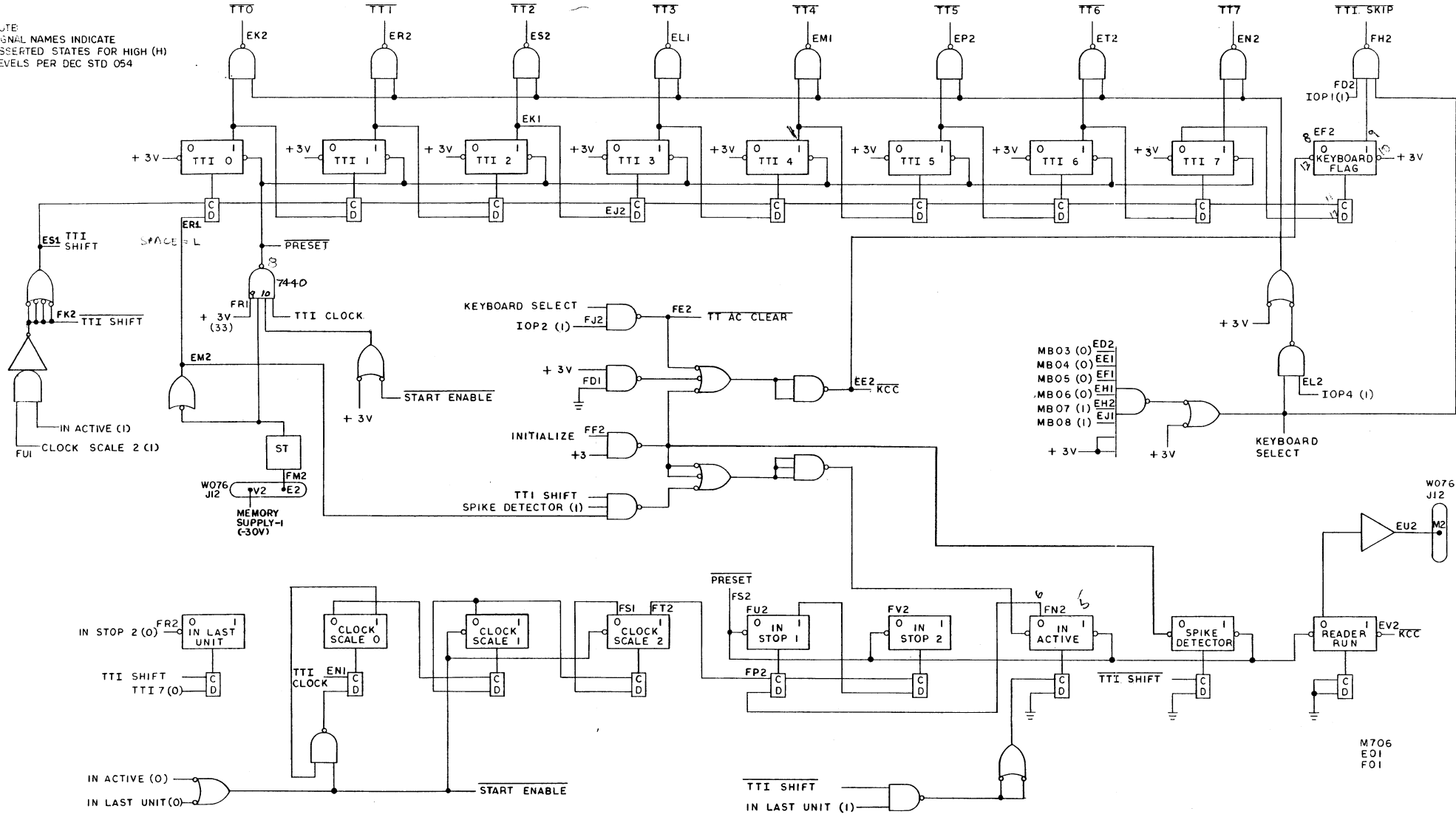


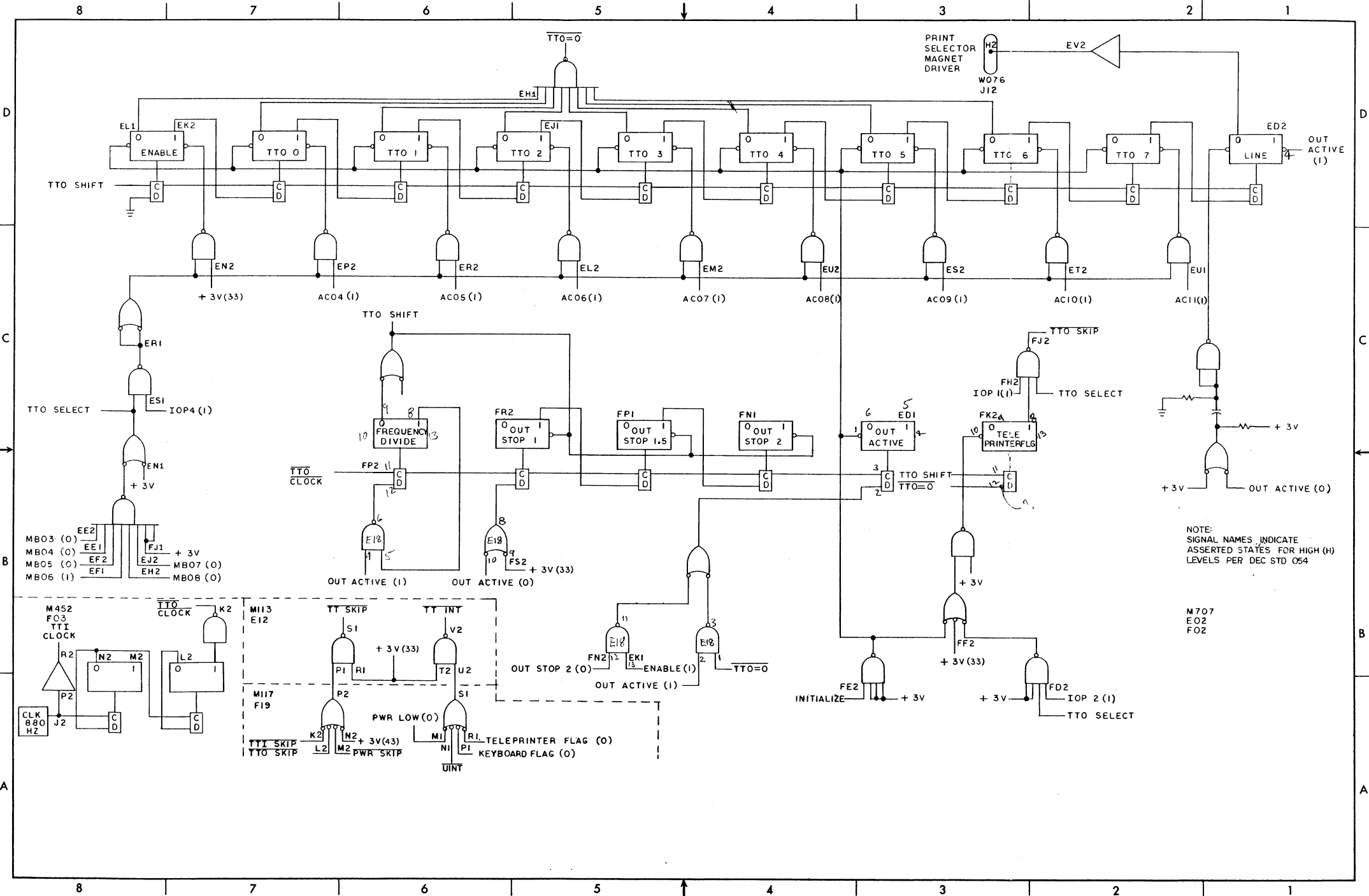


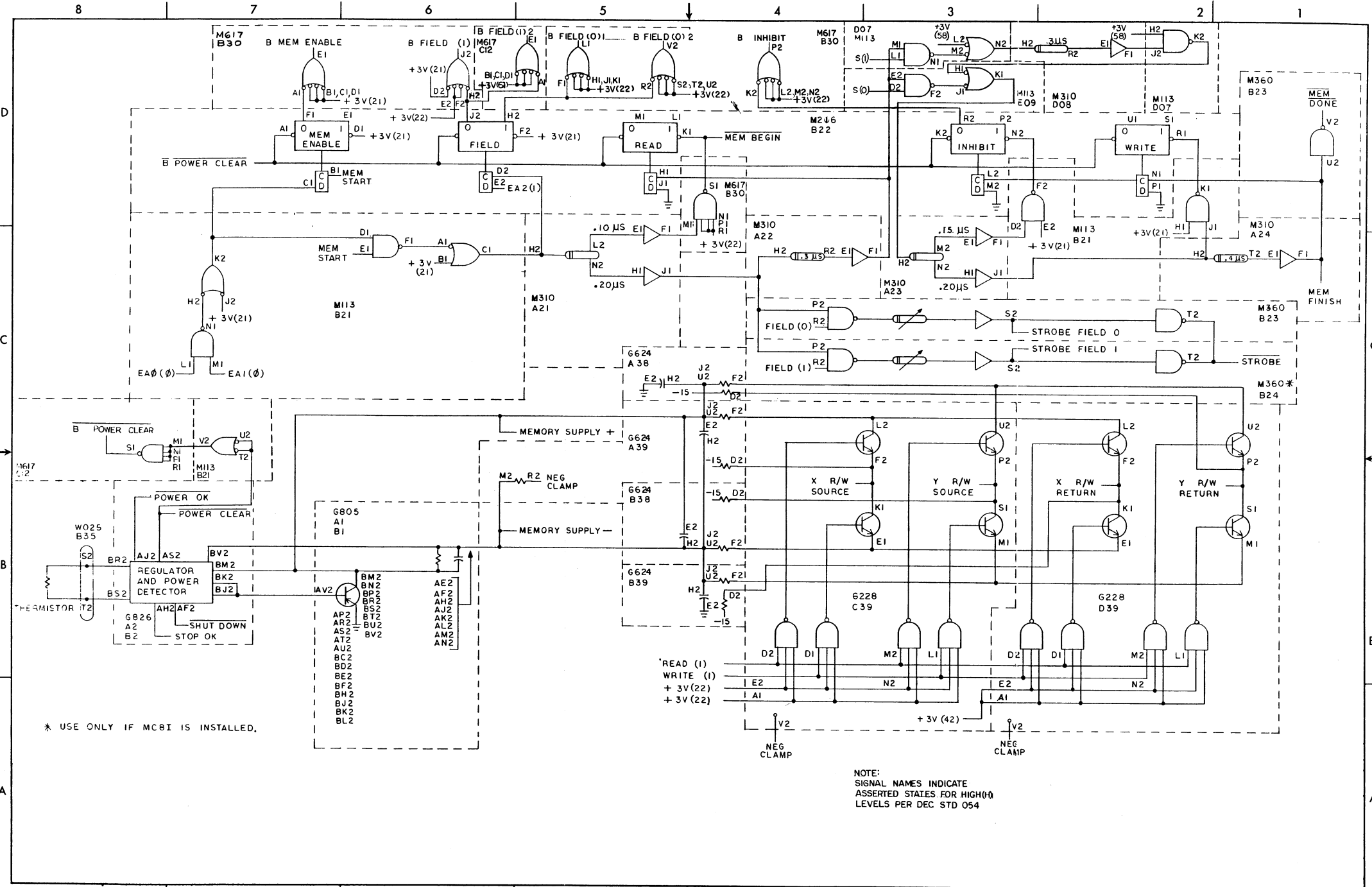
NOTES:
 1. FOR KABI SUBSTITUTE
 D-BS-KABI-0-1 FOR THIS PRINT
 2. SIGNAL NAMES INDICATE ASSERTED STATES
 FOR HIGH (H) LEVELS PER DEC STD 054

8 7 6 5 4 3 2 1

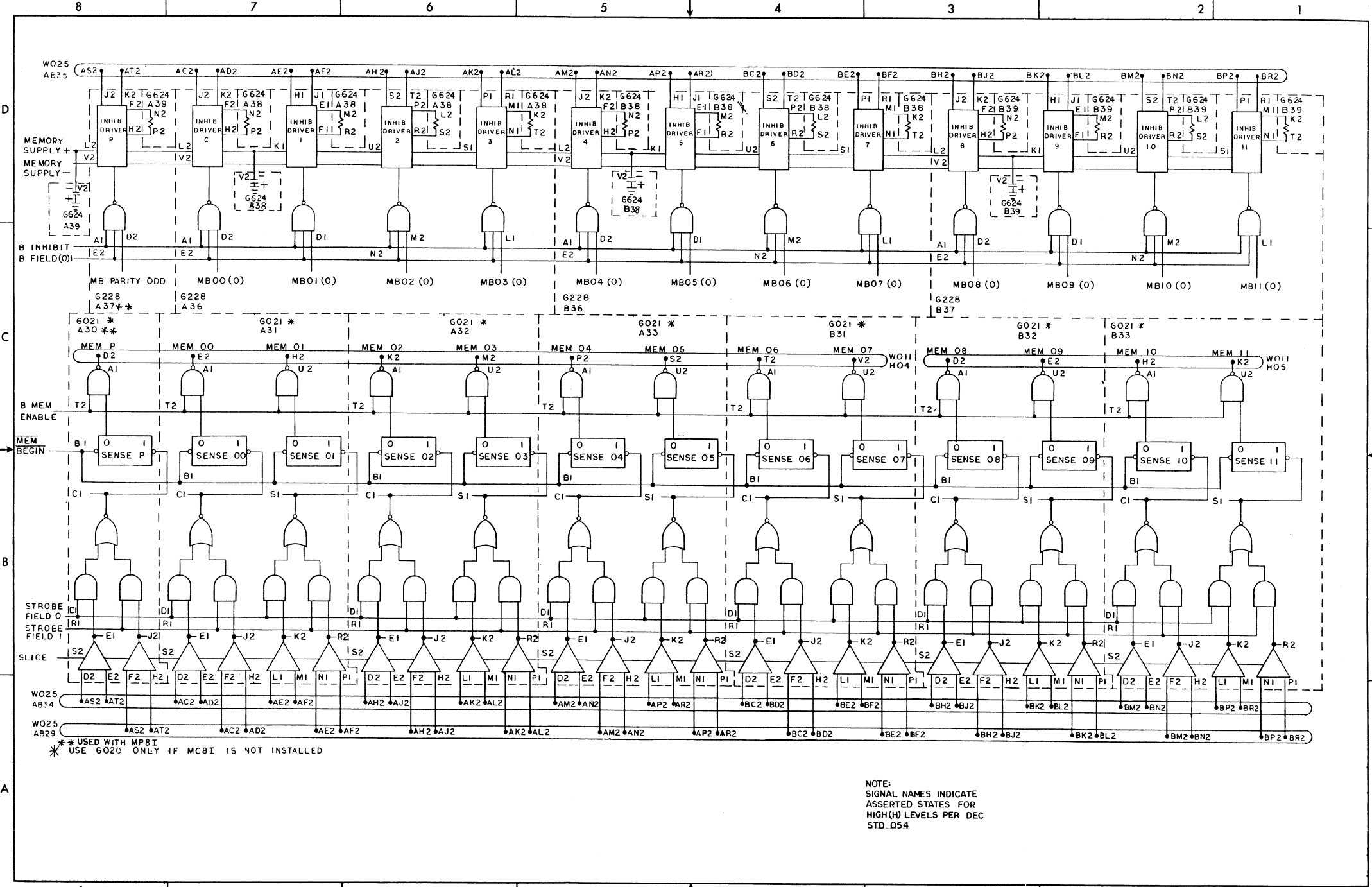
NOTE:
SIGNAL NAMES INDICATE
ASSERTED STATES FOR HIGH (H)
LEVELS PER DEC STD 054



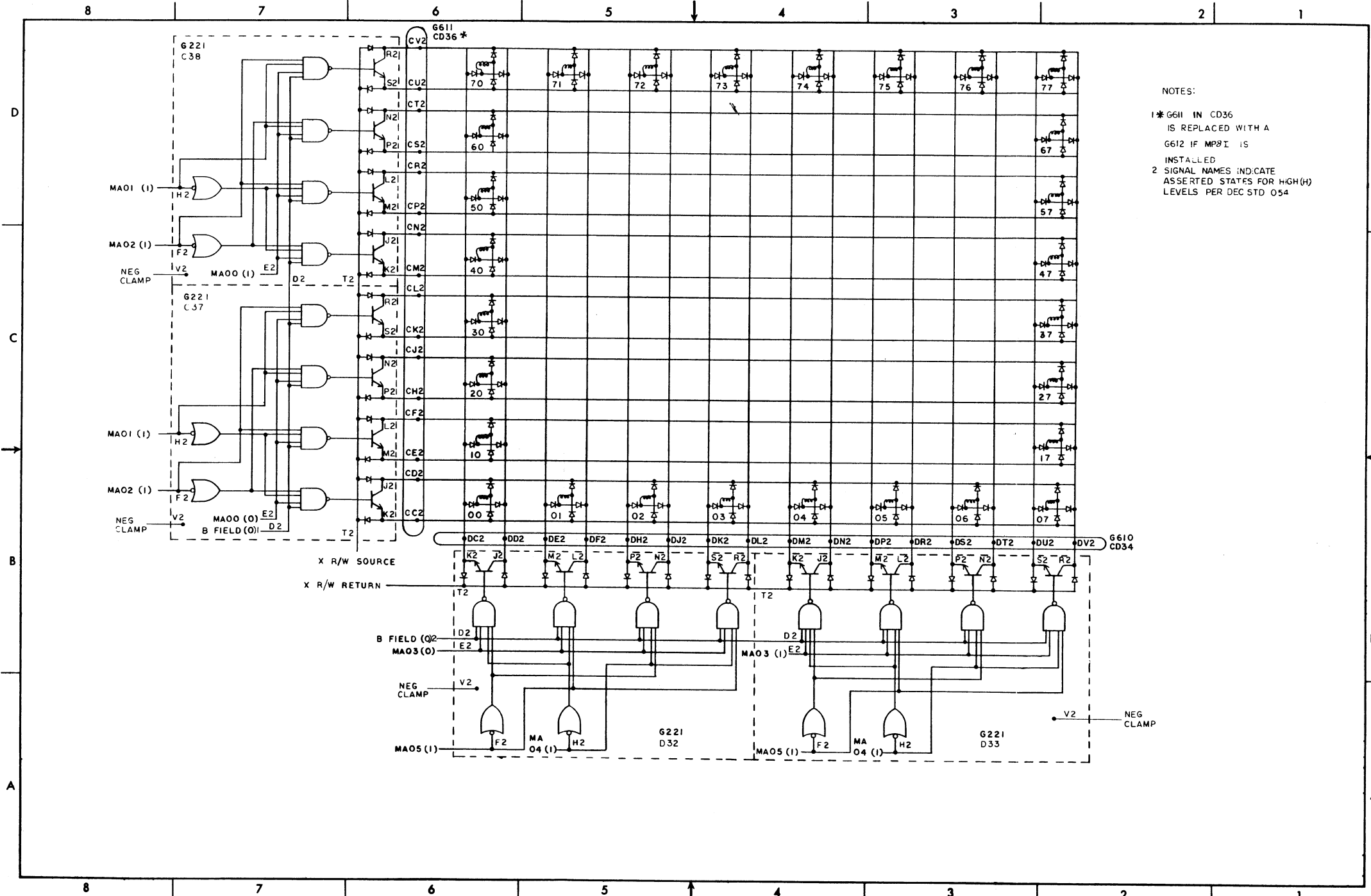




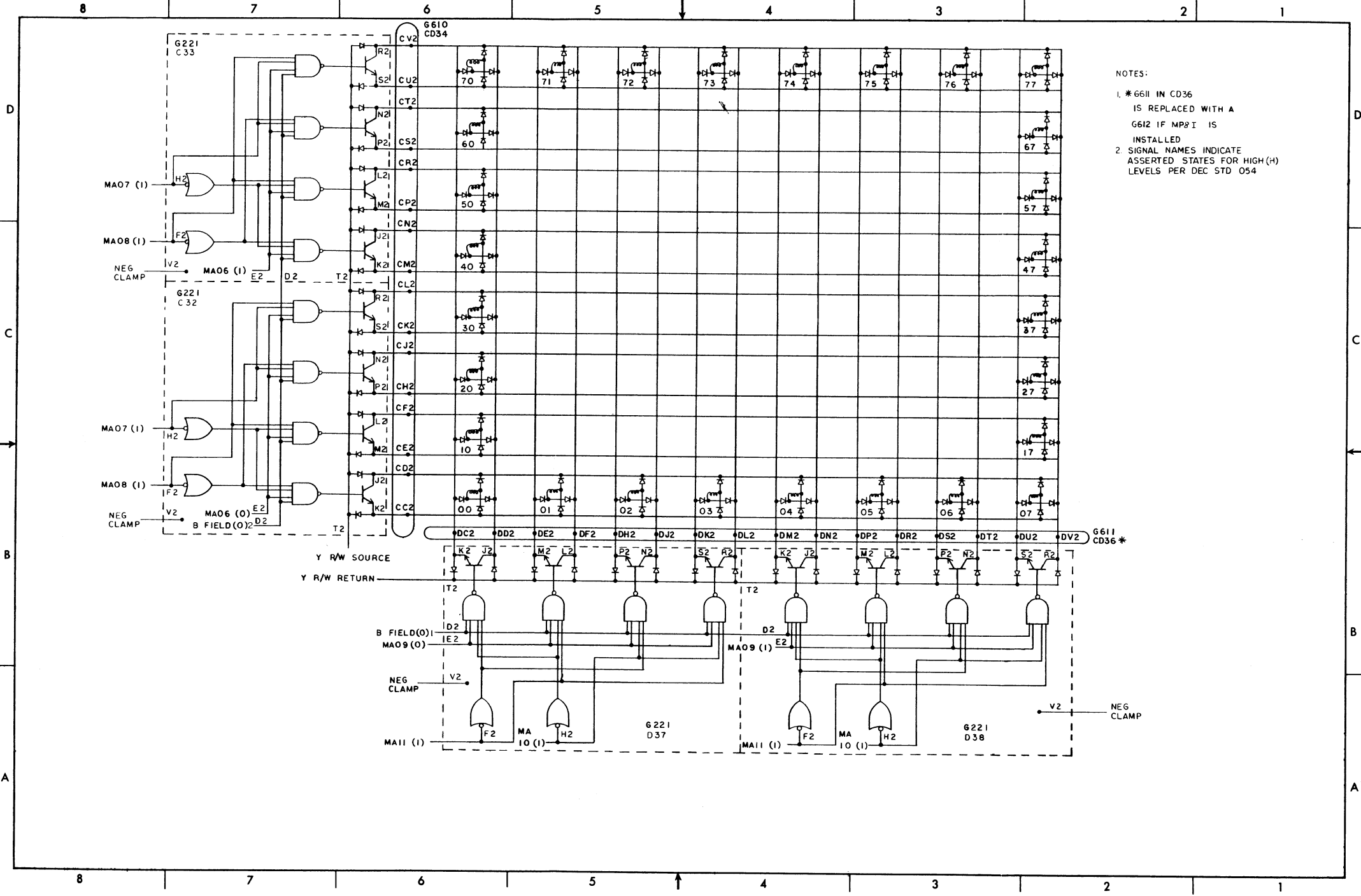
D-BS-8I-0-13 Memory Control



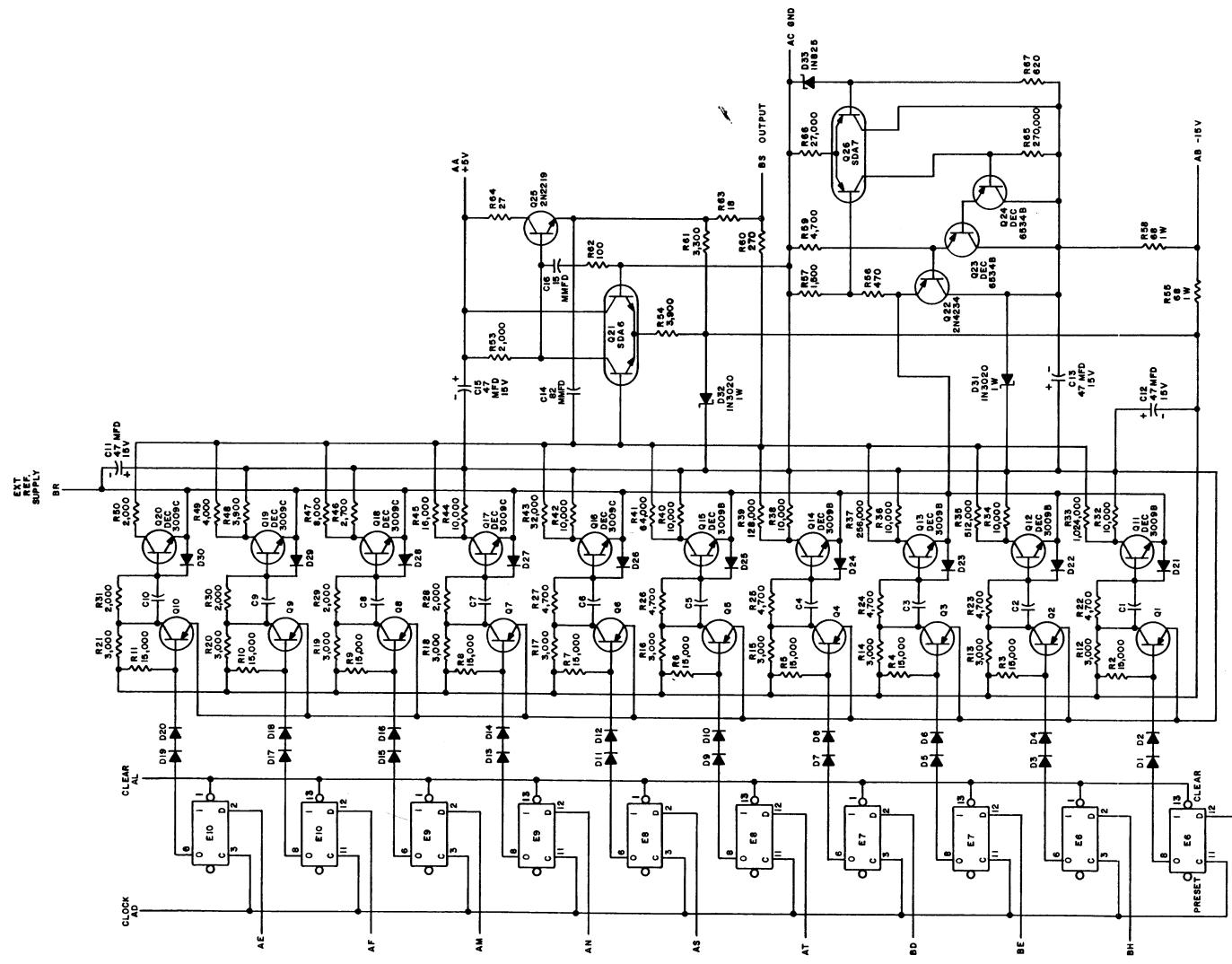
D-BS-81-0-14 Sense Amps and Inhibit Drivers



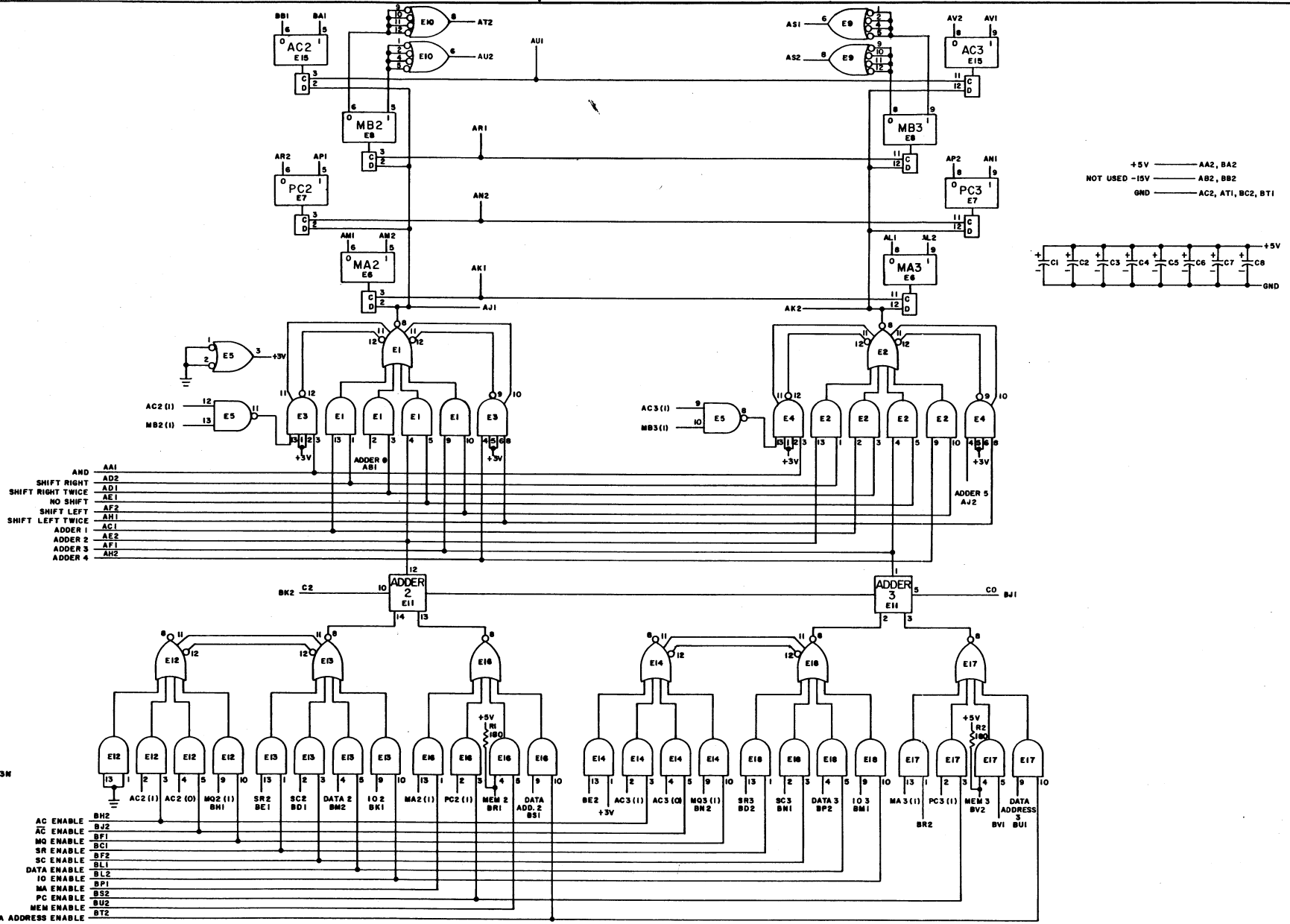
NOTES:
 1 * 6611 IN CD36 IS REPLACED WITH A 6612 IF MP81 IS INSTALLED
 2 SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH(H) LEVELS PER DEC STD 054

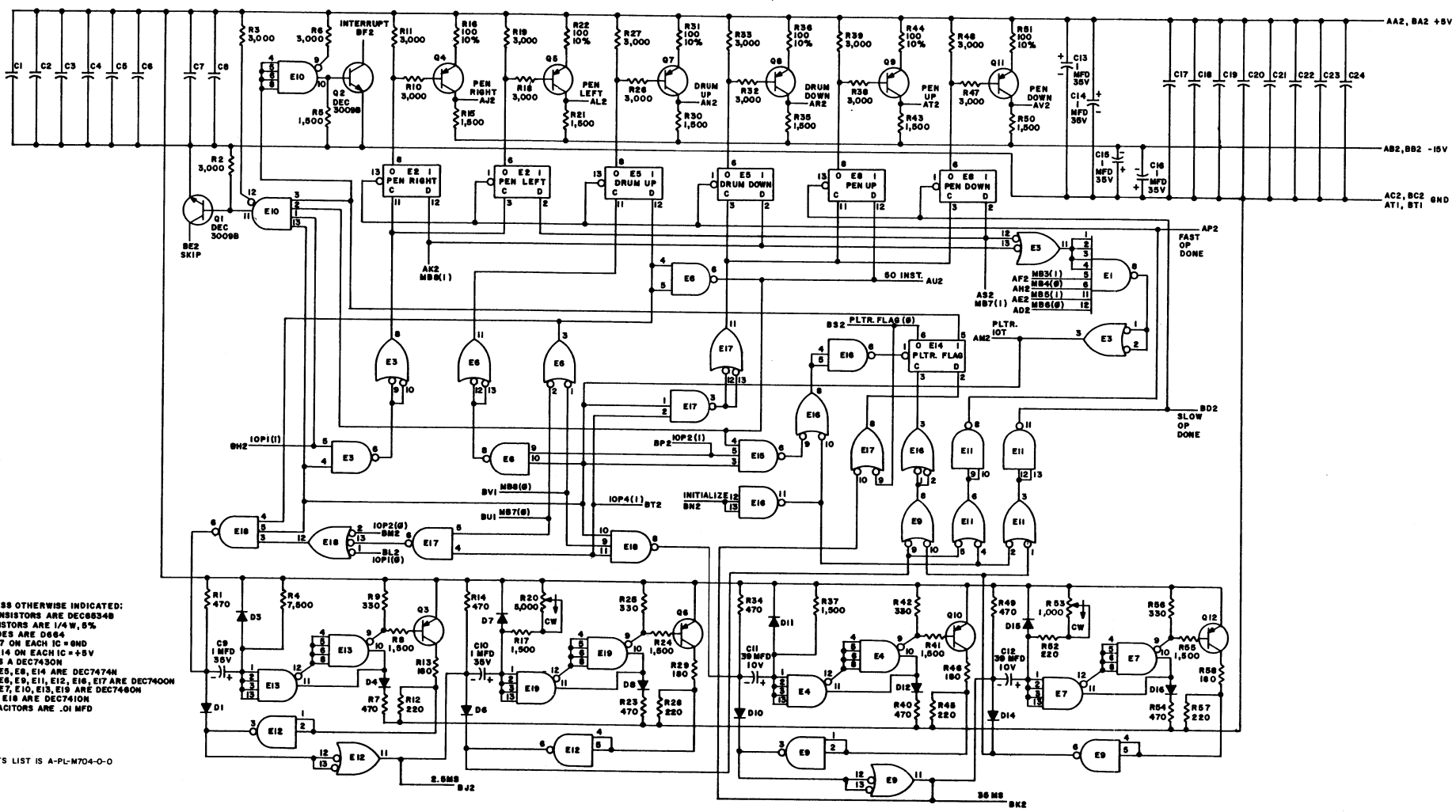


- NOTES:
- * 6611 IN CD36 IS REPLACED WITH A 6612 IF MP9 I IS INSTALLED
 - SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH (H) LEVELS PER DEC STD 054



UNLESS OTHERWISE INDICATED:
 TRANSISTORS ARE DEC2894-3B
 CAPACITORS ARE 50% PPM
 RESISTORS ARE 1/4W, 5%
 Q1'S ARE DEC174N AC GND
 PIN 14 ON EACH IC = AA +5V
 R33 IS 1/2W, 1%, 60 PPM
 R32 IS 1/2W, 1%, 25% PPM
 R37, R39, R41 & R43 ARE 1/2W, 1%, 25% PPM
 R46, R47, R49 & R50 ARE .3W, 0.1%, 5% PPM
 Q16 THRU Q20 ARE SELECTED SILVER DOT





UNLESS OTHERWISE INDICATED:
 TRANSISTORS ARE DEC683-4B
 RESISTORS ARE 1/4 W, 5%
 DIODES ARE D664
 PIN 7 ON EACH IC = GND
 PIN 14 ON EACH IC = +5V
 E1 IS A DEC7430N
 E2, E5, E8, E14 ARE DEC7474N
 E3, E9, E9, E11, E12, E18, E17 ARE DEC7400N
 E4, E7, E10, E13, E19 ARE DEC7460N
 E15, E16 ARE DEC7410N
 CAPACITORS ARE .01 MFD

PARTS LIST IS A-PL-M704-0-0