

# PDP. 9

Programmed Data Processor general purpose computer  
Parallel, Binary with 18 Bit word fixed word length  
8K - (8192) 18 Bit words 2 1/2 D type core  
Single address  
1/2 cycle time (complete memory cycle)

Standard peripherals

PTK - Paper Tape - PC02 300 lines/sec 8 level  
can read alpha or binary 1 line alph (8 Bits)  
3 lines Binary (6 Bits)

Punch PC03 - 50 lines/sec also alpha or binary

Combined PC09

TTY Keyboard INPUT 10 CAR/sec  
output 10 CAR/sec

RTC - real time clock - 60 CPS counter

PI - Program Interrupt facility can be turned on or off.  
signal central processor when peripheral is ready (flag)

DMA - Direct Memory Access

switch to central processor or DMA to other computer

DCH - Data channel - entry port for peripheral to communicate  
med. speed - not built to know where to put, or how many  
or where from (Pee Tape)

Data channel break 3 or 4 cycles

2 memory locations are reserved DCH  $\phi$  1 30 - # word cont.

2. 31 CA CURRENT ADDRESS

CA + 1

Pee Tape 200ms to get ready

3. Start word

# Registers

AC - Accumulator 18 Bit register main arithmetic register  
result end up here also contains 1 operand  
I/O register program controlled

MB - Memory Buffer - 18 stage register

MA - Memory Address location in core 13 bit register  
15 bits with additional memory

PC - program counter 13 bit keeps track of address of  
next instruction sequencing

IR - instruction register 5 bits receive 1st 5 bits of 18  
bit instruction

L. LINK 1 bit extension of AC ext. arithmetic capabilities

2 types of arithmetic Two's complement or one's complement

Link on ones is add overflow  
2's is carry stage

Bit 0 is sign bit if 0 number is +  
1 " is - in complementary forms

AR - arithmetic register 18 bit register to keep  
accumulator on key operations is address indicator

Bus transfer system

all transfers are transferred through AR to prevent runaway

Instructions

SBB Pg 7-1  
USERS MANUAL

1. Memory Ref

2. Augmented  $\begin{cases} \text{OData} \\ \text{IOT} \\ \text{EAE} \end{cases}$

200 DAC \* I ← I\* Says that the Referenced Location contains the Address for the operation specified

~~XXXXXXXXXX~~

AND → 
$$\begin{array}{r} 613562 \\ 046177 \\ \hline 661761 \end{array}$$
 octal addition over 7 add 2

204 LAC 300  
205 AND 1000

Data 001 010 011 000 001 010  
 ^ 111 111 100 000 000 000  
 -----  
 001 010 000 000 000 000

10- 123012  
1000 774000

Masking or Extracting

XOR

202 XOR 517

$$\begin{array}{r} 0101101010 \\ \oplus 0100010111 \\ \hline 0001010101 \end{array}$$

if both are same 0  
different keep a 1

SAD

Skip next step if accumulator is different from 1000

203 SAD 1000

~~204~~  
205

I32

303 I32 42 add a 1 and skip if zero  
less not affect AC or link

# ISZ loop

```

200 xvll
201 xvY
202 xXx
203 xXx
204 ISZ 100 / -10
205 JMP 200
206 HLT
    
```

10 Decimal is 12 octal 000012

-10 is written 777766

```

000 000 000 000 001 010
111 111 111 111 110 101
-----
111 111 111 111 110 110
    
```

$$X = \sqrt{A+B} + \sqrt{C+D} - \sqrt{B+D}$$

```

C(100) - A
C(101) - B
C(102) - C
C(103) - D
C(104) -  $\sqrt{A+B}$ 
C(105) -  $\sqrt{C+D}$ 
C(106)  $\sqrt{B+D}$ 
    
```

```

300 LAC 100 / GET value of A
301 ADD 101 / Sum of A+B
302   | JMS 1372 / Go Get  $\sqrt{A+B}$ 
      | GET Sq Rt.
303 DAC 104  $\sqrt{A+B}$ 
304 LAC 102 Get C
305 ADD 103 Sum of C+D
306 JMS 1372 / Go Get  $\sqrt{C+D}$ 
307 DAC 105
    
```

$\sqrt{\text{Sub Routine}}$   
1372 PC #

1422 ~~Go Back to~~  
JMP\* 1372

JMS: 1. must store in referenced location of PC  
2. Ref location + 1  $\rightarrow$  PC (address)

# CAL

302 CAL 606  
JMS 20

allows extra bits to be freed

---

# XCT

204 XCT 1000  
205 ADD 100

1000 LAC 303

---

CAL  $\begin{matrix} PC \rightarrow 20 \\ '21' \rightarrow PC \end{matrix}$

---

DAC  $AC \rightarrow Y$

---

JMS  $\begin{matrix} PC \rightarrow Y \\ 'Y'+1 \rightarrow PC \end{matrix}$

---

OZM  $\emptyset \rightarrow Y$

---

LAC  $Y \rightarrow AC$

---

XOR  $Y+A \rightarrow AC$

---

ADD  $\begin{matrix} Y+AC \rightarrow AC \\ LV \text{ of } 10 : 1 \rightarrow L \end{matrix}$

---

TAD  $\begin{matrix} Y+AC \rightarrow AC \\ CO \text{ of } \emptyset : \bar{L}-L \end{matrix}$

---

XCT - Do IAS in Y

---

ISZ  $\begin{matrix} Y+1 \rightarrow Y \\ \text{IF } Y+1 = \emptyset \text{ THEN } PC+1 \rightarrow PC \end{matrix}$

---

AND  $Y \wedge AC \rightarrow AC$

---

SAD IF  $Y \neq AC : PC+1 \rightarrow PC$

---

JMP "Y"  $\rightarrow PC$

Y = CORE MEM LOCATION

# Operate Instructions

Pg 7-8

|         |   |   |   |   |     |     |            |   |     |     |     |     |     |     |     |     |         |
|---------|---|---|---|---|-----|-----|------------|---|-----|-----|-----|-----|-----|-----|-----|-----|---------|
| 0       | 1 | 2 | 3 | 4 | 5   | 6   | 7          | 8 | 9   | 10  | 11  | 12  | 13  | 14  | 15  | 16  | 17      |
| 1       | 1 | 1 | 1 | 0 | CLA | CLK | 1 OR 2 PL  | 0 | SNL | SZA | SMA | HLT | RAR | RAL | OAS | CML | Comp    |
| OP Code |   |   |   |   |     |     | ifl        | 1 | SZL | SNA | SPA |     | RTR | RTL |     |     | 15 Comp |
| 748     |   |   |   |   |     |     | Moves 2 PL |   |     |     |     |     |     |     |     |     |         |

## Data or Accumulator Switches

AC V DATA Switches → AC (OAS)

## EVENT TIMES

1. Sensing of skip conditions take place first
2. bits 5+6
3. bits 16+17
4. " 13+14
5. " 15
6. " 12

LAW 76 + "N" 00000 - 17777  
 Load AC with "N"

## Auto Indexing

MEM Loc 10-17 when addressed indirectly contents will be incremented by 1 before it can be used

200 DZM \* 13                      want to zero 300-330  
 201 ISZ 04/777747              in 13/000277  
 202 JMP 200  
 203 HLT

# ISZ Auto Indexing

200 ISZ \* 13

13 = 000 042

42 = 000 172

43 = 777 403

encicement location + contents each 1

Fetch cycle - at beginning MB contains address of instruction

-100NS - MBO +1 PCI (Increment PC)  
-120NS - MA JAM

312NS - AC OUT AR IN

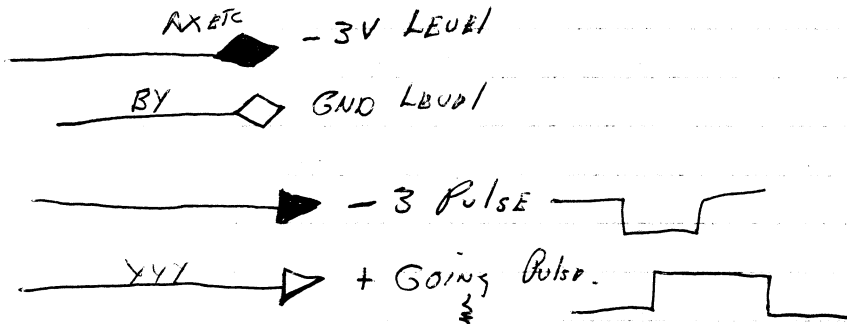
500NS - Memory sends 18 Bit word SA to B Bus to Addr.  
nothing on A to NOSH to MB also code to IR

765NS - Memory write from MB back in memory



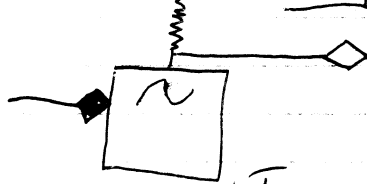


PDP 9 has -3 & 1/2 states



|               |
|---------------|
| MEMORY        |
| MC-70         |
| Control Proc. |
| KC 09-A#      |
| 1-0           |
| KD-09-A#      |

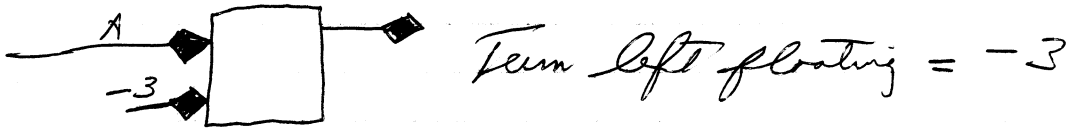
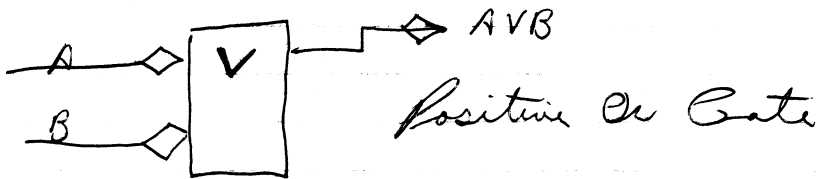
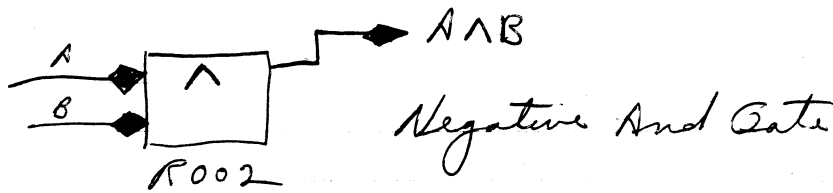
Inverter



D22 - location in Section

inputs can be levels or pulses

Diode Gate

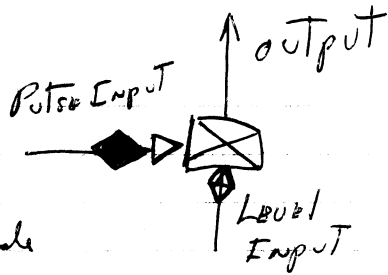


Nand Gate R111 Bin on card node terminal for expanding  
Both inputs neg to get gnd. out



Nor Either input pos get neg -3 out

OCD gate



Diode capacitor Diode

SET { Set by pulse in at -3V  
Level must be at  $\pm$  for 400 NS

FIRB - Pulse input goes + then output occurs  
enable signal can be removed and output still  
can be obtained for 200 NS

Pulse amp.  $\uparrow$  Transformer coupled

B602

Pos or Neg out Pulse Width 40NS

S602-603 - 2 inputs OCD or strait input  
100NS wide  
400NS on 602 if D+M Jumper

W612 - Transformer coupled 120NS or 320NS J&K or T&U

## Delay Networks

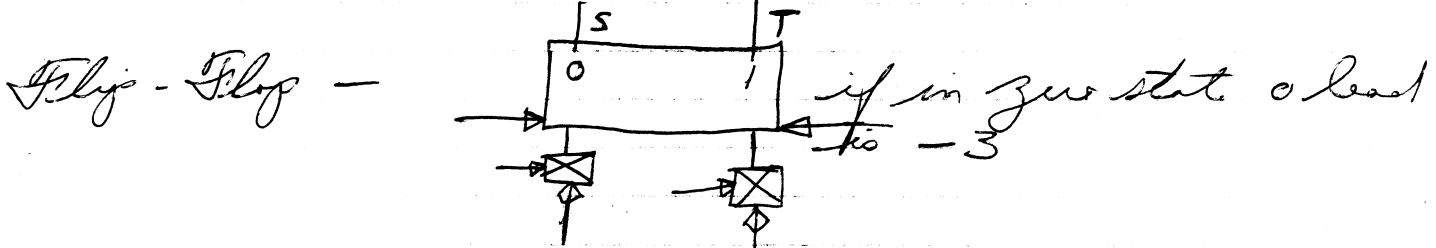
B310 Tapped Delay line inverts on output  
12.5NS Taps 15NS delay thru transistor

R302 Single shot neg. out during delay time

B301 One shot, inversion on input neg pulse  
level output + pulse output pulse occurs at  
end of delay time

B360 - adjustable delay Pos on Meg out  
variable delay 40Ns pulse

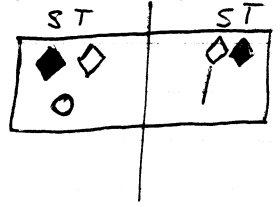
Mixer - B169 or B141 - Has 2 input and gates



Gated Clear into zero state

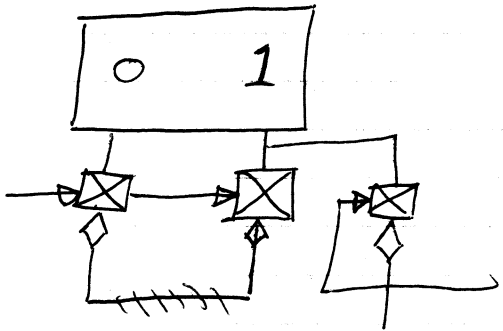
Direct set puts into 1 state  
Direct clear puts into 0 state

5202



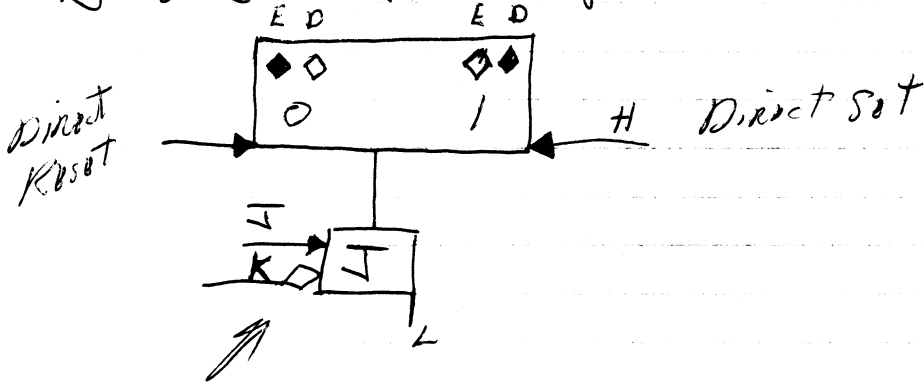
5203 - Only Has DCD gate on 1 side only

5205 Has pulse input common to both sides



B-213

Jam FFlop



Jam Network

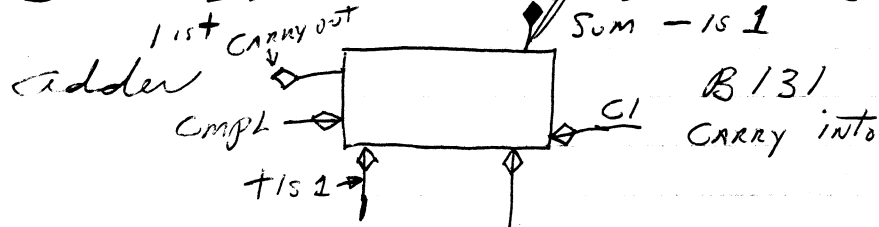
To put into 1 state Term J must be neg and if K is positive K is level input  
 0 state J is negative K negative

If put or gate on expanded level input  
 Buffered means signal has come through inverter to ease loading

PV / KE AFTER Jam PV will end up at same KB same voltage

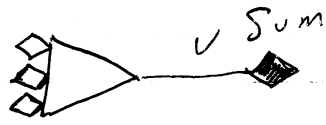
Jam network has 20NS time delay  
 if level is there when jam comes no delay

B 213 has emitter follower on outputs

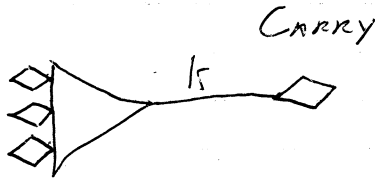


true sum output (binary 1 out) an odd # of true inputs

To get carry out 2 or more times inputs



refer to module drawing



if CMPL is present makes stage think carry is present. is only used for logical functions other than ADD

# Main Memory

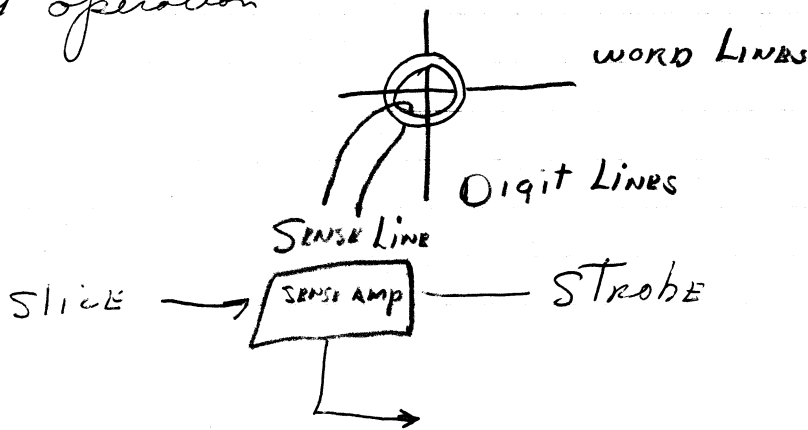
Dec Type MC 70B

2 1/2 D organization

8K (8192) 18 Bit words

complete memory cycle 1  $\mu$ s (read modify + write)

3D Read operation



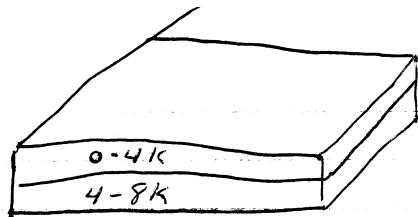
if switches, signal comes out

voltage applied to switch to zero

after reading all cores in 18 bit words are in zero state

write operation - 2D write reversed current to switch state of core if bit coming out was 1 then switch  $\Delta$  current is automatically reversed if bit is one  $\Delta$  current is generated

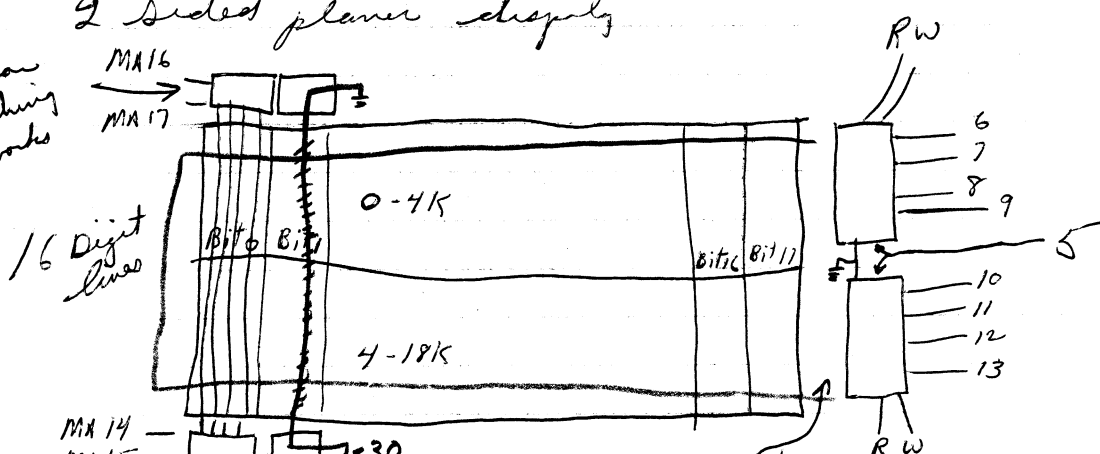
Main Memory Cycle 1  $\mu$ s for read and write back.



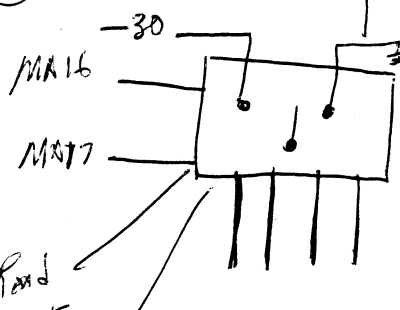
Field 0  
Field 1

2 sided planer display

Bipolar Switching Networks



MA 14  
MA 15  
MA 5 6 7 8 9 10 11 12 13 14 15 16 17  
Field Sel. WORD Selection Digit SEL  
14A 14B 15A 15B

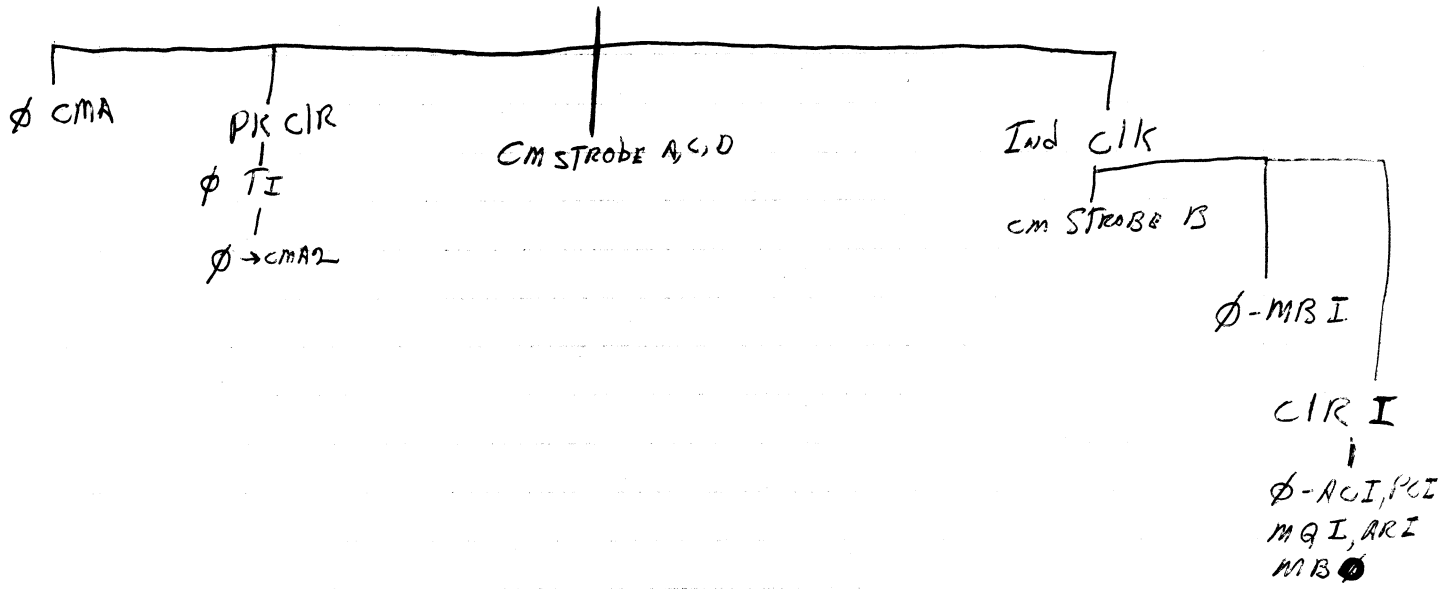


16 Lines out of each  
256 Lines

4,096 upper or 4,096 lower

18 sense amps  
MA Bit 5 field selection

POWER NOT OK OR POWER LOW  
PWR CLK Pos



Run phi



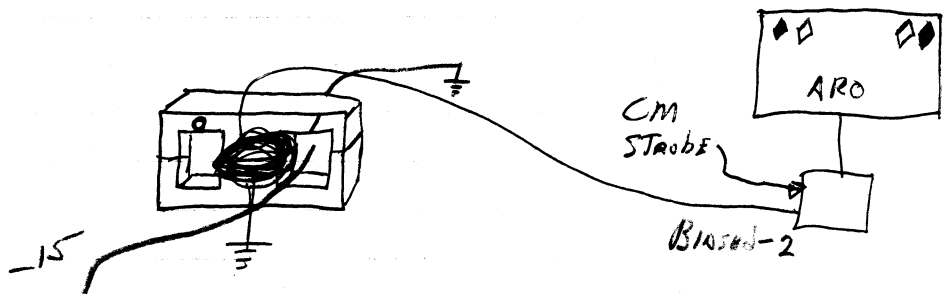


# Control Memory

sets up levels to perform operations  
read only, prewired

Addressing locations it wants does not operate  
sequentially

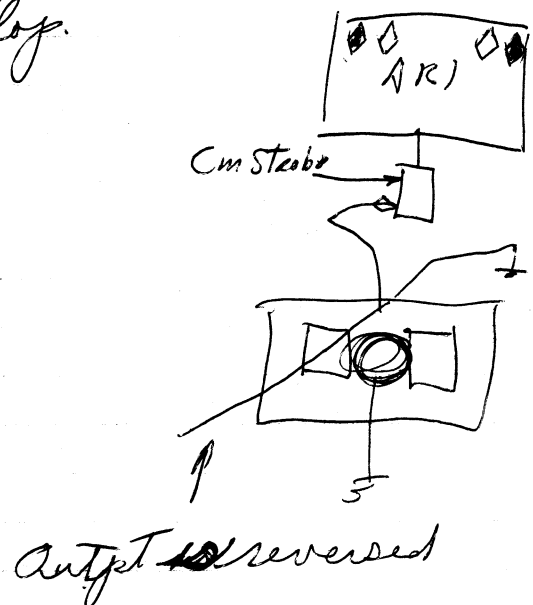
64<sub>(10)</sub> addressable locations  
each location contains 36 bit 30 Bits - Command.  
6 bits addr. bits. tell you where to go next  
contains 36 cores ...

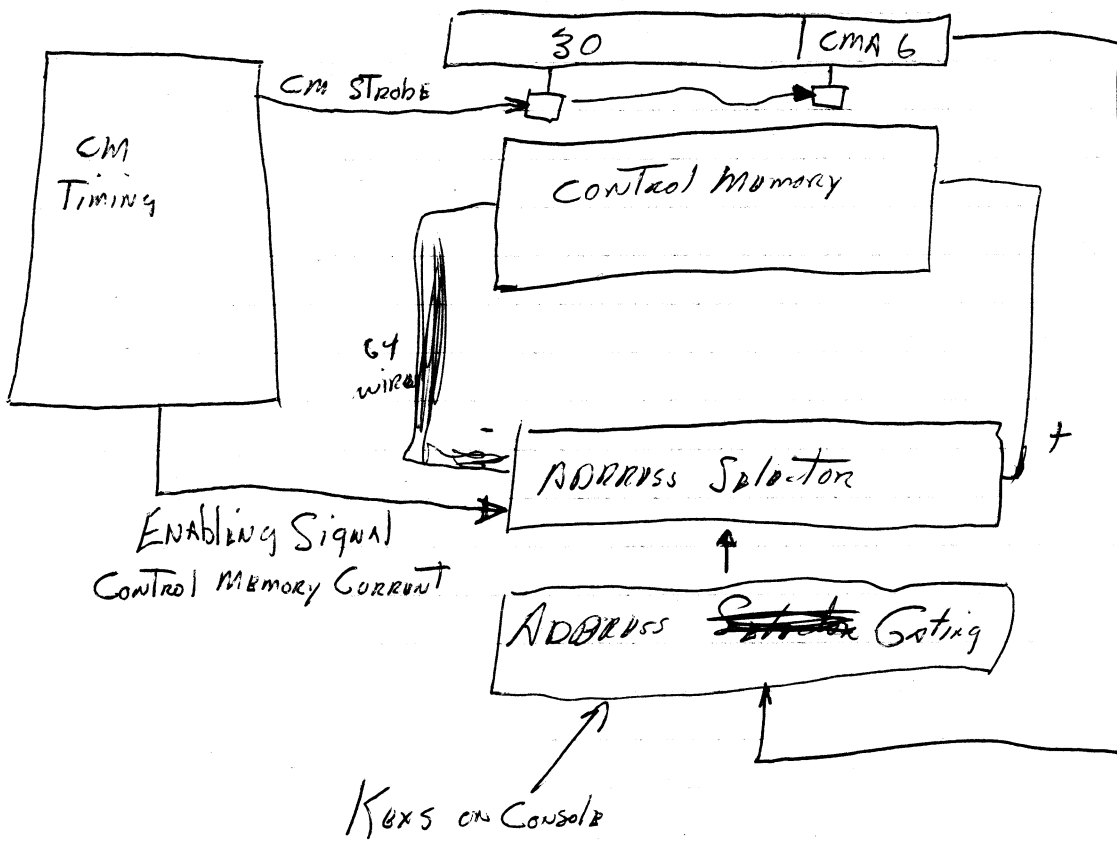


1/2 inch long 1/2 inch high

each 1 core feeds 1 flip-flop.

each core will have  
64 lines passing through  
it





CMA

|   |   |   |   |   |   |
|---|---|---|---|---|---|
| 0 | 1 | 2 | 3 | 4 | 5 |
| 0 | 1 | 0 | 0 | 0 | 1 |

G-210 modules

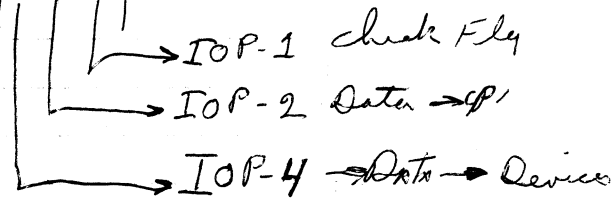
IORS read flags 700314

0 0 0 0 0 0  
Printer Scope

CAF clear all flags 703302  
does not clear any controlling FF's

|         |   |   |   |   |                 |   |   |   |   |    |            |    |    |    |    |    |    |
|---------|---|---|---|---|-----------------|---|---|---|---|----|------------|----|----|----|----|----|----|
| 0       | 1 | 2 | 3 | 4 | 5               | 6 | 7 | 8 | 9 | 10 | 11         | 12 | 13 | 14 | 15 | 16 | 17 |
| 0       | 0 | 0 | 0 | 0 | 0               | 0 | 0 | 0 | 0 | 0  | 0          | 0  | 0  | 0  | 0  | 0  | 0  |
| OP Code |   |   |   |   | Device Sel CODE |   |   |   |   |    | Sub Device |    | ↑  |    |    |    |    |

chr  
AC  
if2



ION - Enables a peripheral to signal when it desires servicing interrupt facility on 700042

IOF 700002 - resets PIE

KSF - Skip on keyboard flag 700301

KRB - 700312 read keyboard buffer to AC. 10-17

PC02 - Reader

PC03 - Paper tape punch

Each either binary or alpha - usually asked in binary 8 is always punched 7 never punched 1st 6 are bits

Reader - 300 lines/sec optical reader completely under program control both alpha or binary mode

Alpha - 1 line of 8 bits  
Binary - 3 lines of 6 bits

has 18 bit buffer in computer, must have hole -  
8 punched in order to read.  
Hardware read in format - Binary

RSB - Select reader in binary mode 700144

# Real Time Clock

Main Mem loc 7 is real time clk counter. Increment is stolen with out any program cont. when clock count goes to 0 clock flag is set for program interrupt

CION 700044

Data Channel - provides fast transfer from M. Memory and medium speed peripheral. flag on device will automatically pull program into break cycle (3 or 4). Uses word count like real-time clk.

Reserved for data channels

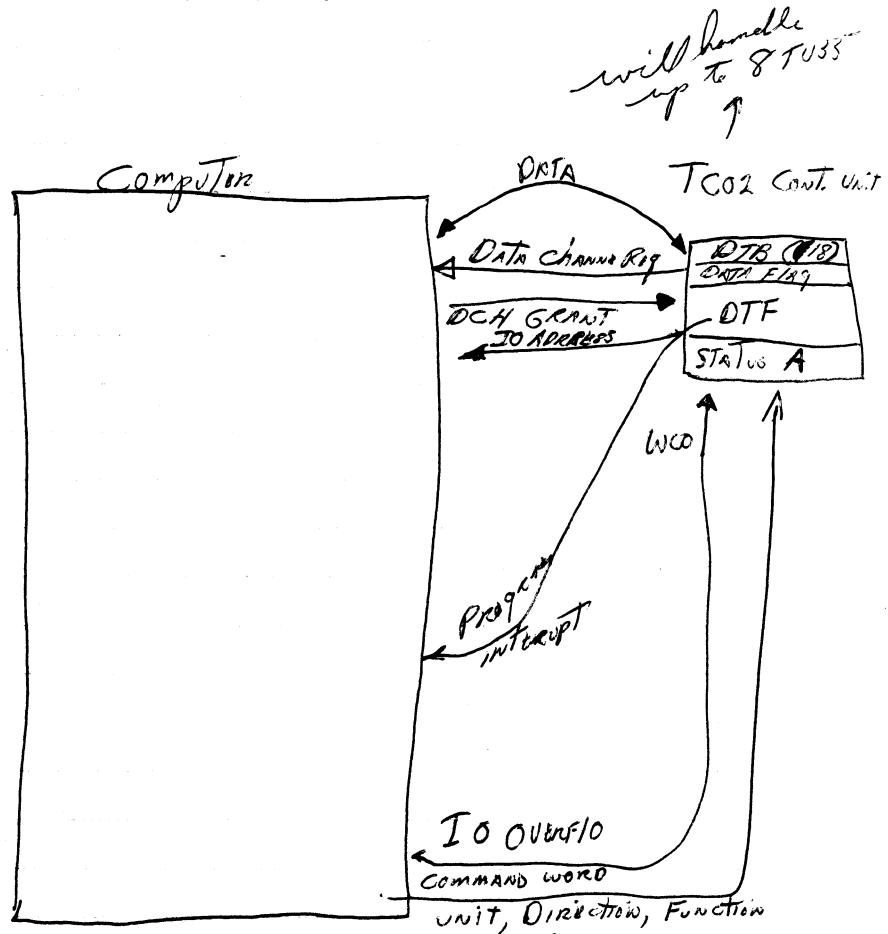
Data ch 0 → 30 - word count location for determination of how many words  
 → 31 - address of 1st word to be read in (current address)  
 See Tape are all tied to ch-0

Data ch 1 → 32  
 → 33

ch 2 → 34  
 → 35

ch 3 → 36  
 → 37

See Tape - 200ms can assemble 18 bit word full speed



$\overline{ADD}$   
 $\overline{AR}$   
 $+ \overline{MB}$   
 $\overline{AC}$

$\overline{TAD}$   
 $\overline{AR}$   
 $\overline{MB}$   
 $\overline{AC}$

carry out of address 0  
 = end around carry

carry out of  $\overline{ADD}$  1's compliment add end around carry  
 In 2's compliment add compliment line

### IOT codes

|                  |   |   |   |          |   |                    |   |   |   |    |   |    |     |    |                                  |    |    |  |
|------------------|---|---|---|----------|---|--------------------|---|---|---|----|---|----|-----|----|----------------------------------|----|----|--|
| 0                | 1 | 2 | 3 | 4        | 5 | 6                  | 7 | 8 | 9 | 10 | 11                                      | 12 | 13  | 14 | 15                               | 16 | 17 |  |
| OP CODE<br>70(8) |   |   |   | NOT USED |   | DEVICE Sel<br>CODE |   |   |   |    | Sub.<br>Device Sel<br>Mode of Operation |    | CIA |    | INPUT OUTPUTS                    |    |    |  |
|                  |   |   |   |          |   |                    |   |   |   |    |   |    |     |    | 1 → IOP(1)<br>Flag CLK           |    |    |  |
|                  |   |   |   |          |   |                    |   |   |   |    |   |    |     |    | → IOP 2<br>DATA TRANS<br>TO C.P. |    |    |  |
|                  |   |   |   |          |   |                    |   |   |   |    |   |    |     |    | → IOP-4<br>DATA<br>TO A DEVICE   |    |    |  |

1ms Pulses

