

#### IDENTIFICATION

PRODUCT CODE: MAINDEC-08-D1AC-D  
PRODUCT NAME: PDP-8 Memory Power On/Off Test  
DATE CREATED: September 16, 1968  
MAINTAINER: Diagnostic Group  
AUTHOR: M. Horovitz  
PREVIOUS CODE: MAINDEC 829



1. ABSTRACT

This program is a Memory Data Validity Test to be used after a simulated power failure.

2. REQUIREMENTS

Storage

Memory locations  $0001_8$ -- $7477_8$

Subprogram and/or Subroutines

RIM

Binary Loader

Equipment

PDP-8 Processor, keyboard reader, and Teleprinter

3. USAGE

3.1 Loading

Normal binary tape loading procedures are to be used with this program.

3.2 Start up and/or Entry

Load address 0014 and press START.

The program should then halt at  $0042_8$ .

Load address 0001 and press START.

The program should now loop.

3.3 Errors in Usage

Errors detected by the program cause the program to halt at memory address  $0055_8$ . The contents of memory addresses  $0011_8$  and  $0012_8$  indicate the addresses of the data that failed to check-sum. Memory addresses  $0007_8$  and  $0010_8$  contain the data words that failed to check-sum.

Lower Address =  $(0011_8) = 100_8 - 3677_8$

Upper Address =  $(0012_8) = 3700_8 - 7477_8$

Lower Error Word =  $(0007_8) = 2525_8$

Upper Error Word =  $(0010_8) = 5252_8$

3.4 Error Recovery

Press CONTINUE to test for other error words in memory.

Reload address  $0020_8$  to restart the entire program.

#### 4. DESCRIPTION

##### 4.1 Discussion

This program tests memory for bit drop out and pick up after a simulated power failure has occurred.

By starting the program at memory address  $0014_8$ , data words consisting of  $2525_8$  are written into memory locations  $0100_8$ -- $3677_8$ , and the data words consisting of  $5252_8$  are written into memory locations  $3700_8$ -- $7477_8$  after which the program halts at memory address  $0042_8$ . Load address  $0001$  and re-start the program; the program will 2's add the contents of memory location  $0100_8$  with  $3700_8$ . If the result equals  $7777_8$ , the program will 2's add the contents of memory locations  $0101_8$  with  $3701_8$ , etc. until the memory addresses of  $3677_8$  and  $7477_8$  are tested. The program stays in the 2's add compare loop until an error occurs. Concurrently cycle the power to the PDP-8 off and on. After the power has been reapplied to the PDP-8, load address  $0001_8$  and press START. If an error occurred during the power cycling, the program halts at location  $0056_8$ . The program may be restarted at memory address  $0001_8$  as many times as desired. Restart address to fill memory is  $0020_8$  not  $0014$ .

##### 4.2 Examples and/or Applications

A HALT occurs at memory address  $0055_8$ .

Address  $0007_8 = 2505_8$  (Data Word)

Address  $0010_8 = 5252$  (Data Word)

Address  $0011_8 = 0101$  (Address Word)

Address  $0012_8 = 3701$  (Address Word)

Bit 7 was dropped at memory address  $0101_8$ .

#### 5. EXECUTION TIME

1 msec/loop

/4 MEMORY POWER ON OFF TEST

0001  
 0001 5001  
 0002 0002  
 0003 0003

JMP 1 /START AFTER POWER UP  
 2  
 3

0014  
 0014 1072  
 0015 3000  
 0016 1073  
 0017 3001

\*0014  
 IAU PATCH  
 UCA 0  
 IAU PATCH+1  
 UCA 1

0020 4022  
 0021 5030  
 0022 0000  
 0023 1065  
 0024 3011  
 0025 1066  
 0026 3012  
 0027 5422

START, JMS SETUP /START INITIAL  
 JMP WRKUN  
 0  
 IAU K00//  
 UCA 11  
 IAU K56//  
 UCA 12  
 JMP 1 SETUP

0030 1070  
 0031 3411  
 0032 1071  
 0033 3412  
 0034 1011  
 0035 7040  
 0036 1066  
 0037 7040  
 0040 7640  
 0041 5030

WRKUN,  
 IAU JPREG  
 UCA 1 11  
 IAU LOREG  
 UCA 1 12  
 IAU 11  
 UMA  
 IAU K56//  
 UMA  
 ULA SZA  
 JMP WRKUN

0042 7402

/TURN POWER OFF AND ON

0043 4022  
 0044 7200  
 0045 1411  
 0046 3007  
 0047 1412  
 0050 3010  
 0051 1007  
 0052 1010  
 0053 7040  
 0054 7440

COMPAR, JMS SETUP  
 CLA  
 IAU 1 11  
 UCA UPPER  
 IAU 1 12  
 UCA LOWER  
 IAU UPPER  
 IAU LOWER  
 UMA  
 SZA

/11=UPPER ADDRESS 100-3/00  
 /12=LOWER ADDRESS 3/01-7/00

0055 7402  
 0056 1011  
 0057 7040  
 0060 1066  
 0061 7040  
 0062 7640  
 0063 5044  
 0064 5043

HLT, /ERROR, NO COMPARE  
 IAU 11  
 UMA  
 IAU K56//  
 UMA  
 SZA CLA  
 JMP COMPAR+1  
 JMP COMPAR

0065	0077	0077
0066	3677	3677
0067	7700	7700
0070	2525	2525
0071	5252	5252
0072	0043	CUMPAR
0073	5400	JMP I 0
0007	*000/	/ERROR WORD (2525)
0010	UPPER, 0	/ERROR WORD (5252)
	LOWER, 0	
	\$	

THERE ARE NO ERRORS

SYMBOL TABLE

CUMPAR	0043
E1	0055
K0077	0065
K3677	0066
K7700	0067
LOREG	0071
LOWER	0010
PATCH	0072
SETUP	0022
START	0020
STEND	0042
UPPER	0047
UPREG	0070
WRKON	0030

SYMBOL TABLE

UPPER	0007
LOWER	0010
START	0020
SETUP	0022
WRKON	0030
STEND	0042
COMPAR	0043
E1	0055
K0077	0065
K3677	0066
K7700	0067
UPREG	0070
LOREG	0071
PATCH	0072