DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION — DATE 22 MARCH 78

TITLE KT8A FIELD INSTALLATION AND ACCEPTANCE PROCEDURE

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	ECO CHANGE	00001	A.TSHUDY	4-78		5-3-78
B	ECO CHANGE	ML0002	P.GARDNER	12-78		19 Dec 78

ENG	APPD	SIZE	CODE	NUMBER	REV
	RB Pearson	A	SP	KT8A-3	B

EN-10764-16-N873-(382)
DRA 107A

ML SHEET 1 OF 12

ENGINEERING SPECIFICATION — Lucrum — CONTINUATION SHEET

TITLE KT8A FIELD INSTALLATION AND ACCEPTANCE PROCEDURE

I General

This document will define the hardware requirements and tests to be preformed to: #1) install, #2) configure and #3) accept a KT8-AA system or KT8-AB add-on to an existing system.

Because the KT8-A Memory Management options has several possible hardaware configurations, the Hardware Rules/Restrictions (appendix A), General Configuration Guide (appendix B) and Configuration Examples (appendix C) should be referenced before installing this option.

A. If the KT8-AA was shipped as part of a system, refer only to the Acceptance procedure.

B. If the KT8-AB is an add-on installation to upgrade an existing system, then refer to the Installation and Acceptance Procedures.

II Hardware

This section defines the required hardware to install and accept a KT8-A and also defines the three hardware designations of the KT8-A option.

A. The KT can be installed and accepted on any 8A/420 or 620 machine.

B. The KC8A Programmer's Console is not required, as the KT diagnostics have a console package.

C. Program loading media is via: Paper tape, Floppy, or RK#5.

D. The Three designations of the KT are as follows:

1. KT8A-A - the KT Memory Management option shipped as part of a system configured by a DEC Manufacturing facility.

2. KT8A-B - the required hardware to upgrade an 8A/420 or 8A/620 system. The KM8-AC (M8317YB or YC) is part of this option.

SIZE	CODE	NUMBER	REV
A	SP	KT8A-3	B

DEC FORM NO EN-01022-16-N370-(381)

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TITLE KT8A FIELD INSTALLATION AND ACCEPTANCE PROCEDURE

3. KT8-EX - this option is required any time the memories are located is two seperate boxes (BA8C's). If required as part of an add-on, both the KT8-AB and KT8-EX must be ordered as seperate line items.

III Installation

Before proceding with your installation refer to Appendix A and B to familarize yourself with the rules and configurations. Also refer to the configuration example that most represents your particular installation.

1. Install all memory in the system, refer to Congiguration guide (appendix B).

2. Install the KT8-AB in any vacant OMNIBUS slot with an "E" connector.

3. If the system is comprised of two (2) BA8C boxes and memory will be located in each box than install the M9020, terminator module, in any available "E" connector of the box not containing the KT8-A (M8416). Now connect the cable (70-11411-1J) between the two berg connectors of the M8416 and M9020.

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A	SP	KT8A-3	B

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IV Acceptance

The time to accept a KT8-A configuration depends upon the amount of memory installed.

1. Load and run the KT8-A Memory Management Diagnostic, Maindec #8-DJKTA-A, for five min. with NO errors.

2. Load and run the Extended Address Test Maindec #8-DHKMC-C, for one pass with NO errors.

3. Load and run the Extended Memory Data and Checkerboard Test, Maindec #3-DHKMA-D, for one pass with NO errors.

4. To insure system integrity, load and build a DEC/X8 program using version 2, which will exercise up to 128K of memory. It is important that the program is build using the latest DEC/X8 modules.

NOTE: Reference should be made to the latest write-up for DEC/X8 (version 2) as further parameters must be inputted to support break devices.

SIZE	CODE	NUMBER	REV
A	SP	KT8A-3	B

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APPENDIX A

HARDWARE RULES/RESTRICTIONS

1. Any OMNIBUS CPU (KK8A or KK8F) using a BA8C box (20 slot box) is acceptable.
2. The KT8-A system can only be configured using any combination of MM8AB (16K core) and MS8C (16K or 32K MOS) memories.

   NOTE: MM8AA, MR8A, MS8A, MM8E, MM8EJ and MR8F memories cannot be used to configured a KT8A system.
3. If the system is made up of MM8AB core memories (16K), then they must be modified per ECO MM8AB #7, refer to table 1 for instructions.
4. If the system is made up of MS8C type memories (16Kor 32K MOS), them refer to table 2 for switch configuration.
5. The PDP/8E chassis cannot be used as part of a KT8-A system.
6. If Power Fail/Auto Restart and/or Bootstraps are required as part of the system, then a KM8-AC (M8317YB or YC) must be used with the Memory Extension and Timeshare option disabled via the jumper configuration in table 3.

   NOTE: The M8317 and M8317YA are incompatable with the KT8A system.

TABLE 1 MM8-AB 16K CORE MEMORY CONNECTIONS

MEMORY BANK	MEMORY FIELD	CONNECTIONS WIRE	CONNECTIONS JUMPER
0	0-3 (0-16K)	AB1 to EB2	1-3, 3-4 in
	4-7 (16-32)	AB1 to EB2	2-4, 3-4 in
1	0-3 (32-48)	AB1 to ED2	1-3, 3-4 in
	4-7 (48-64)	AB1 to ED2	2-4, 3-4 in
2	0-3 (64-80)	AB1 to EL2	1-3, 3-4 in
	4-7 (80-96)	AB1 to EL2	2-4, 3-4 in
3	0-3 (96-112)	AB1 to ER2	1-3, 3-4 in
	4-7 (112-128)	AB1 to ER2	2-4, 3-4 in

TABLE 2A MS8-CA 16K MOS MEMORY SWITCH SETTINGS

MEMORY BANK	MEMORY FIELD	SWITCHES SET TO "OFF" ALL OTHERS "ON"
0	0-3 (0-16K)	S1-1
	4-7 (16-32K)	S1-2
1	0-3 (32-48K)	S1-3
	4-7 (48-64K)	S1-4
2	0-3 (64-80K)	S1-5
	4-7 (80-96K)	S1-6
3	0-3 (96-112)	S1-7
	4-7 (112-128)	S1-8

TABLE 2B MS8-CB 32K MOS MEMORY SWITCH SETTING

MEMORY BANK	MEMORY FIELD	SWITCHES SET TO "OF ' ALL OTHERS "ON"
0	0-7 (0-32K)	S1-1 and S1-2
1	0-7 (32-64K)	S1-3 and S1-4
2	0-7 (64-96K)	S1-5 and S1-6
3	0-7 (96-128)	S1-7 and S1-8

TABLE 3 JUMPER CONFIGURATION TO DISABLE MEMORY EXTENSION AND TIMESHARE

JUMPERS	
W1	CUT
W2	IN
W3	IN
W4	IN

APPENDIX B

General Configuration Rules

1. All memories must be physically located in the OMNIBUS where an "E" connector is present.
2. Remembering the above rule, place the memories as far away as posible from the CPU.
3. Direct Memory Address interfaces can only be located between the CPU and the first memory element. With one exception, in a two box system (2 BA8C's) where memory is located in both boxes a DMA interface may be located in any vacant slot of the box containing the CPU.
4. Programmed I/O interfaces may be located in any vacant slot of the system.
5. When memories are located in two BA8C chassis then the KT8-EX option must be used to extend the memory management option bank bits. The M9020 terminator card must be located in an "E" connector of the BA8C not containing the M8416. The 70-11411-1J cable is then connected between the M9020 and the M8416.

APPENDIX C

Configration Examples

Because the KT8-A is limited to use in the BA8C chassis (20 slot box) there are only four possible configurations.

1. The entire system located in one BA8C with a KK8A CPU as shown below.

SLOT	OPTION	DEFINITION
1	KK8A	CPU (M8315)
2	DKC8A	OPTION ONE (M8316), IF REQUIRED
3	KM8-AC	OPTION TWO (M8317YB or YC), IF REQUIRED
4	KT8-A	MEMORY MANAGEMENT OPTION (M8416)
5	-----	DMA DEVICES CONFIGURED FROM THIS POINT TOWARD MEMORY
6	-----	
7	-----	
8	-----	
9	-----	
10	-----	
11	MEMORY	MEMORY CONGIGURED FROM THIS POINT TOWARD THE CPU
12	-----	ONLY I/O INTERFACES
13	-----	
14	-----	
15	-----	
16	-----	
17	-----	
18	-----	
19	-----	
20	-----	ONLY I/O INTERFACES

2. The entire system located in one BA8C with a KK8F CPU as shown below.

SLOT	OPTION	DEFINITION
1	KK8F	TERMINATOR, M8320
2	DKC8A	OPTION ONE (M8316), IF REQUIRED
3	KM8-AC	OPTION TWO (M8317YB orYC), IF REQUIRED
4	KT8-A	MEMORY MANAGEMENT OPTION (M8416)
5	MEMORY	MEMORY CONFIGURED FROM THIS POINT TOWARD CPU
6	-----	
7	-----	
8	-----	
9	-----	
10	-----	
11	-----	
12	-----	
13	-----	
14	-----	
15	-----	
16	-----	
17	-----	DMA AND I/O INTERFACES CONFIGURED FROM THIS POINT TOWARD MEMORY
18	KK8F	CPU, M8310
19	KK8F	CPU, M8300
20	KK8F	CPU, M8330

3. The KT8-A system made up of two BA8C boxes with the KK8F CPU in one box and all the memory located in the other box as shown below.

(TOP BA8C)

SLOT	OPTION	DEFINITION
1	KK8F	TERMINATOR, M8320
2	-----	ANY I/O INTERFACE
3	-----	ANY I/O INTERFACE
4	KT8-A	MEMORY MANAGEMENT OPTION (M8416)
5	MEMORY	MEMORY CONFIGURED FROM THIS POINT TOWARD THE CPU
6	-----	
7	-----	
8	-----	
9	-----	
10	-----	
11	-----	LAST POSSIBLE MEMORY IN THIS CONFIGURATION
12	-----	ANY DMA OR I/O INTERFACES
13	-----	
14	-----	
15	-----	
16	-----	
17	-----	
18	-----	
19	-----	
20	BC08H-3	OMNIBUS EXPANDER CABLES

(BOTTOM BA8C)

1	BC08H-3	OMNIBUS EXPANDER CABLES
2	DKC8A	OPTION ONE (M8316), IF REQUIRED
3	KM8-AC	OPTION TWO (M8317YB or YC), IF REQUIRED
4	-----	
5	-----	
6	-----	
7	-----	
8	-----	
9	-----	
10	-----	
11	-----	
12	-----	
13	-----	
14	-----	
15	-----	
16	-----	
17	-----	DMA AND I/O INTERFACES CONFIGURED FROM THIS POINT TOWARD MEMORY
18	KK8F	CPU, M8310
19	KK8F	CPU, M8300
20	KK8F	CPU, M8330

4. The KT8-A system made up of two BA8C boxes with a KK8F in one box and memories located in both boxes as shown below:

(TOP BA8C)

SLOT	OPTION	DEFINITION
1	KK8F	TERMINATOR, M8320
2	-----	ANY I/O INTERFACE
3	-----	ANY I/O INTERFACE
4	M9820	KT8A TERMINATOR, LOCATE IN SLOT "E" OF OMNIBUS
5	MEMORY	MEMORY CONFIGURED FROM THIS POINT TOWARD CPU
6	-----	
7	-----	
8	-----	
9	-----	
10	-----	
11	MEMORY	LAST MEMORY ELEMENT IN THIS BA8C!
12	-----	ANY I/O INTERFACES
13	-----	
14	-----	
15	-----	
16	-----	
17	-----	
18	-----	
19	----	ANY I/O INTERFACES
20	BC08H-3	OMNIBUS EXPANDER CABLES

(BOTTOM BA8C)

1	BC08H-3	OMNIBUS EXPANDER CABLES
2	DKC8A	OPTION ONE (M8316), IF REQUIRED
3	KM8-AC	OPTION TWO (M8317YB or YC), IF REQUIRED
4	KT8-A	MEMORY MANAGEMENT OPTION, M8416
5	MEMORY	CONTINUE CONFIGURING MEMORY FROM THIS POINT TOWARD THE CPU
6	-----	
7	-----	
8	-----	
9	-----	
10	-----	
11	-----	LAST POSSIBLE MEMORY IN THIS CONFIGURATION!
12	-----	
13	-----	
14	-----	
15	-----	
16	-----	
17	-----	DMA AND I/O INTERFACES CONFIGURATED FROM THIS POINT TOWARD MEMORY
18	KK8F	CPU, M8310
19	KK8F	CPU, M8300
20	KK8F	CPU, M8330

COMPONENT SIDE VIEW

2-1

1-4

1-5

1-6

J1

E107 E97 E89 E80 E70 E60 E40 E33 E24 E18 E10
C29 R35 R34 R29 C23 C21 R17 R16 R13 R11 C10 C7 C4
R35 R36 C30
E122 E115 E108 E96 E88 E79 E69 E59 E49 E39 E32 E23 E17 E9
R37 R33 R32 R28 R21 C20 C13 R2 R1
E121 E114 E105 E95 E87 E78 E68 E58 E48 E31 E16 E8
C31 R27 R26 R20 C19
E120 E113 E104 E94 E86 E77 E67 E57 E47 E7
C36 R24 R25 R29 R18 C15
E119 E112 E103 E93 E85 E76 E66 E56 E46 E38 E30 E22 E15 E6
R30 R31 R12 R9 R8 C9 C2
E118 E111 E102 E92 E84 E75 E65 E55 E45 E37 E29 E14 E5
C35 C37 C18 R11 R7 R6 R3
E117 E110 E101 E91 E83 E74 E64 E54 E44 E36 E28 E4
R36 C28 C22 R15 R14 R10 C5
E109 E100 E90 E82 E73 E63 E53 E43 E35 E27 E21 E13 E3
C25 R23 R22
E99 E72 E62 E52 E42 E34 E26 E20 E12 E2
C34 C27 E81 R1 R5 C12 C6 C2
E116 E108 E98 E71 E61 E51 E41 E33 E25 E19 E11 E1
C24 C16 C14 C8 C1

F E D C B A

V U T S R P N M L K J H F E D C B A

NOTES: MODULE REWORK AT RELEASE
ETCH CUT SIDE 2 @ 1 BETWEEN
DAZ 2 FEEDTHRUS NEAR C16

CHK	CHANGE NO	REV
JA	M8146C0001	C

S. KLIEN

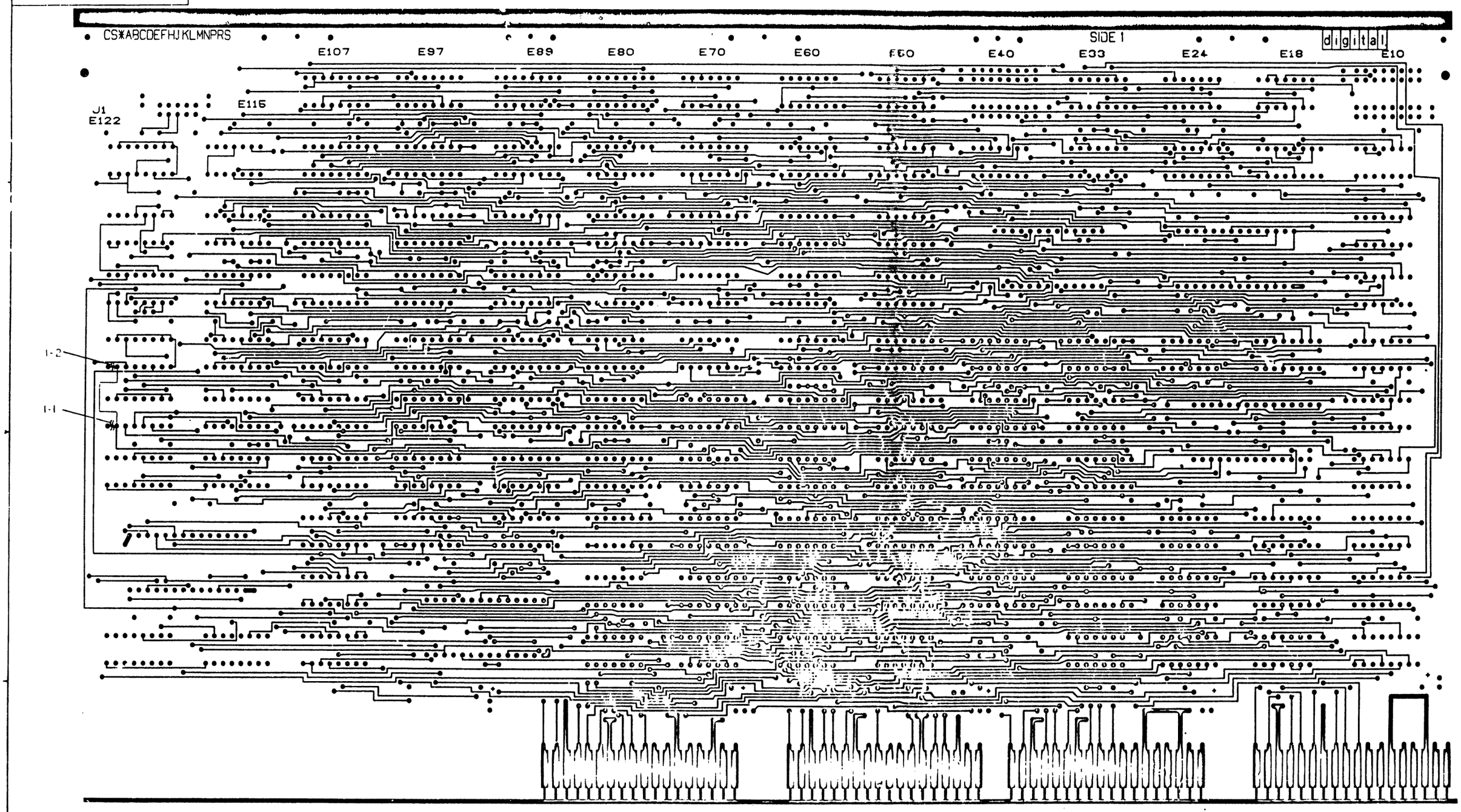
ETCH REV. C
P.C. DESIGN DATA BASE REV. C

SIGNATURES	DATE
DRN.	10/77
CHK'D.	11/77
ENG. R. Rogers	12/7/77
PROJ.ENG. R. Rogers	12/7/77
PROD.	12/7/77
SCALE 2/1	
SHT. 1 OF 6	
NEXT HIGHER ASSY. KM8B	

digital

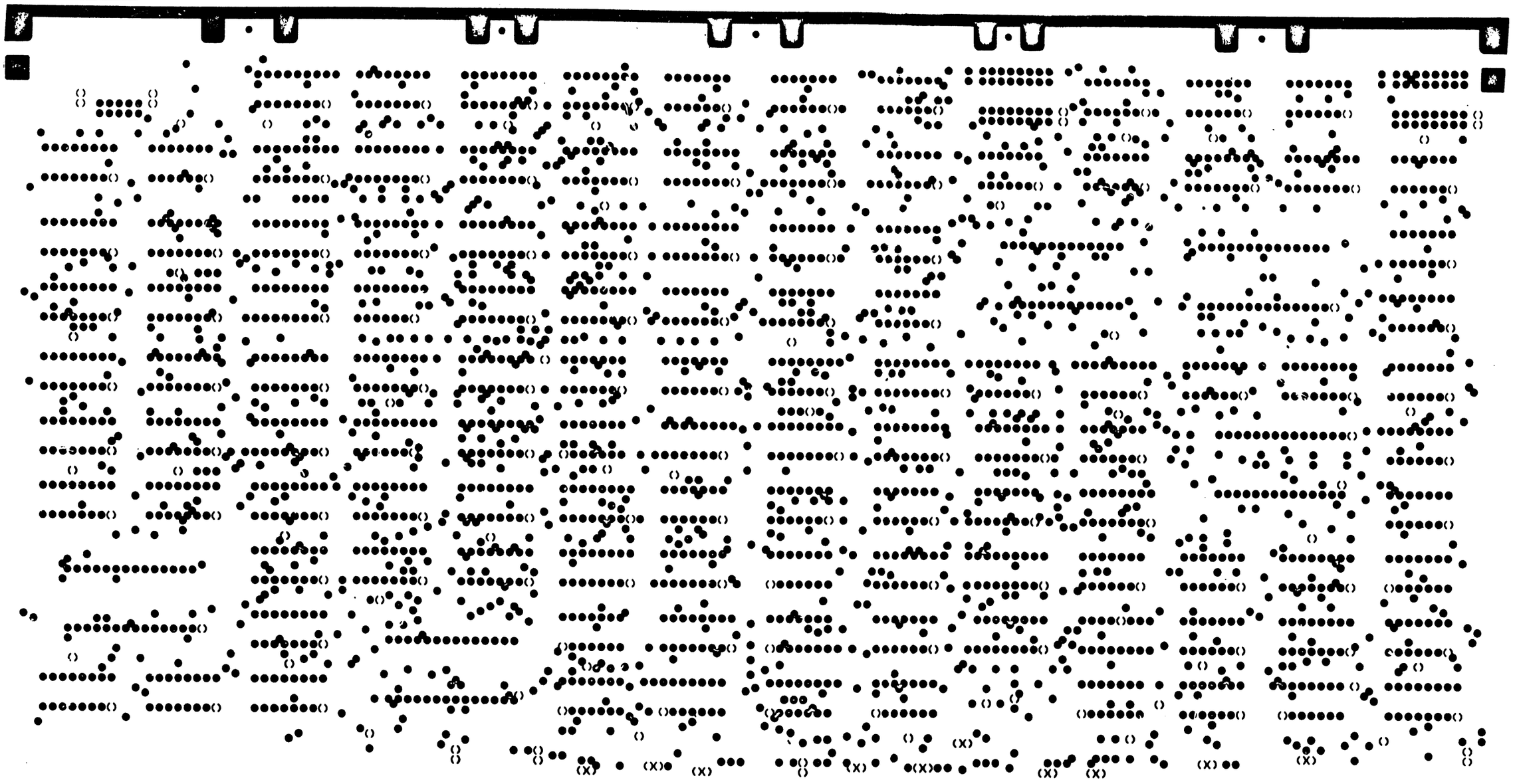
TITLE PDP8 MEMORY MANAGEMENT BOARD

SIZE	CODE	NUMBER	REV
D	UA	M8146-0-0	D



VIEWED FROM SIDE 1

TITLE	PDP8 MEMORY MANAGEMENT BOARD		SIZE	CODE	NUMBER		REV.
			D	UA	M8416 -0-0		D
SCALE	2:1	SHEET 2 OF 6	DIST				

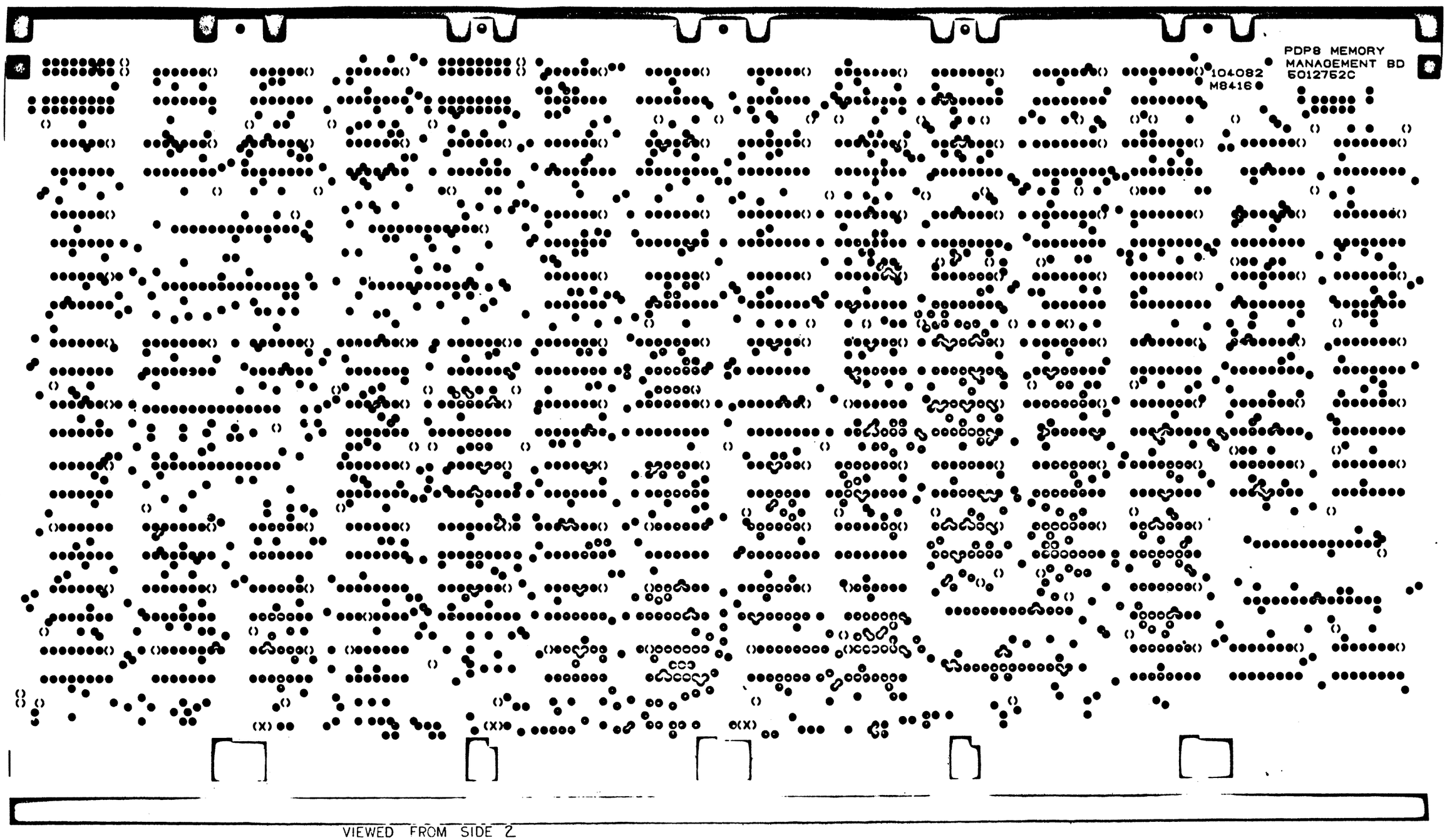


VIEWED FROM SIDE 1

REVISION		
CHK	CHANGE NO.	ECO

TITLE	PDP-8 MEMORY MANAGEMENT BOARD	SIZE	CODE	NUMBER / REV
		D	UA	M8416 -0-0 / D
SCALE	3:1	SHEET 3 OF 6	DIST	

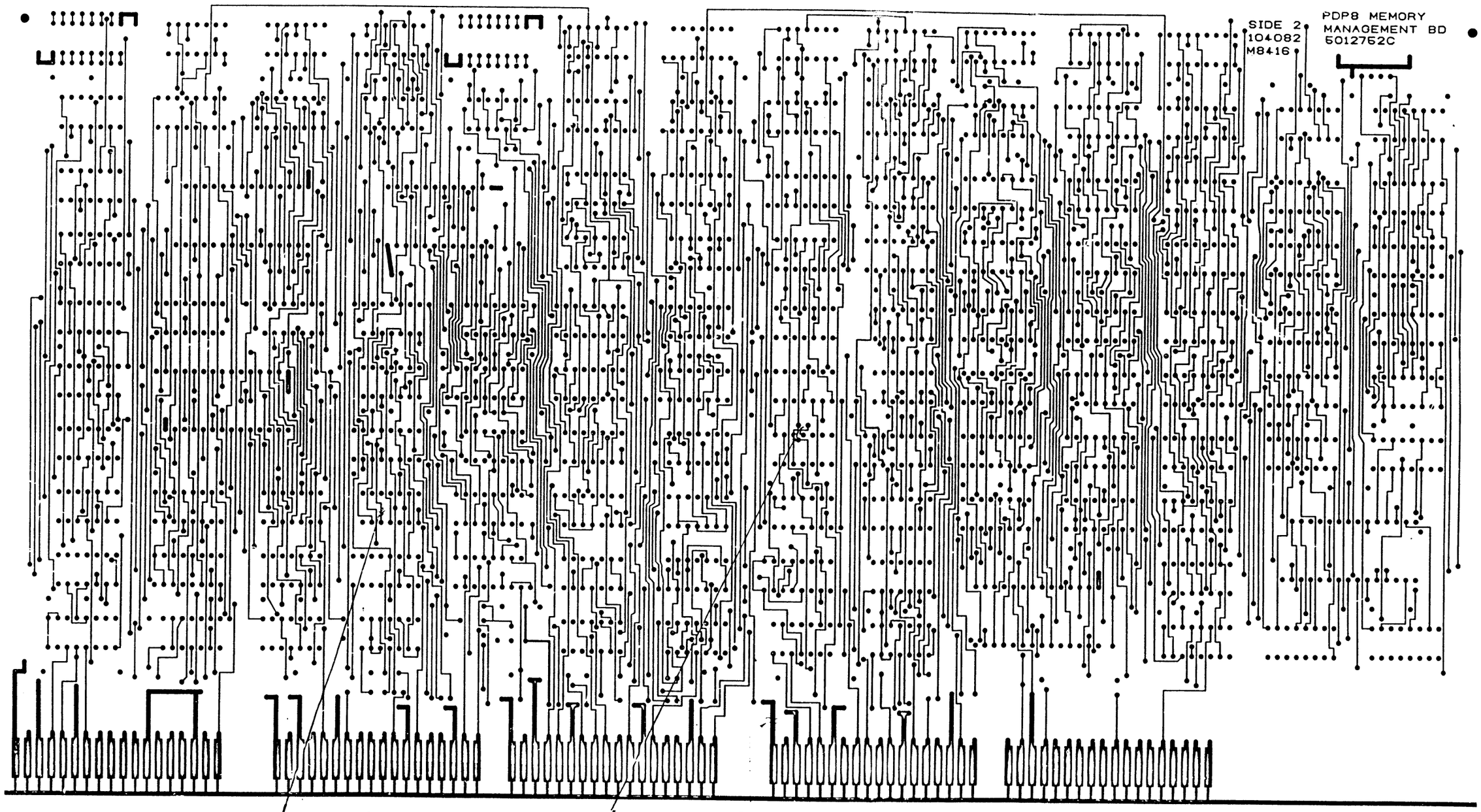
PDP8 MEMORY MANAGEMENT BD
104082
M8416
5012752C



VIEWED FROM SIDE 2

REVISIONS		
CHK	CHANGE NO	REV

TITLE PDP 8 MEMORY MANAGEMENT BOARD	SIZE D	CODE 104	NUMBER M8416 -1-D	REV D
SCALE 2:1	SHEET 4 OF 6	DIST		



TITLE PDP 8 MEMORY MANAGEMENT BOARD		SIZE D	CODE CA	NUMBER M8416 -0-0	REV. D
SCALE 2:1	SHEET 5 OF 6	DIST			

REWORK INSTRUCTIONS

E.C.O. #1

ETCH CUTS SIDE 1

1-1: BETWEEN E118 PIN1 & E118 PIN2
1-2: BETWEEN E119 PIN1 & E119 PIN2

ETCH CUTS SIDE 2

1-3: BETWEEN E64 PIN10 & FEED THRU ABOVE AND BETWEEN E64 PIN5 11,12

WIRE ADDS SIDE 1

1-4: FROM E118 PIN2 TO E119 PIN2
1-5: FROM E118 PIN1 TO E65 PIN5-7
1-6: FROM E63 PIN6 TO FEED THRU THAT WAS CUT FROM E64-10

ECO #2:

ETCH CUTS SIDE2

2-1: E27-5

WIRE ADDS SIDE1

2-2: E33-11 TO E27-5

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
PDP8 MEMORY MANAGEMENT BOARD	D	UA	M8416-0-0	D
SCALE —	SHEET 6 OF 6	DIST.		

P A R T S L I S T

LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QTY	REFERENCE DESIGNATOR
				M8416	1	
1	1	D-MD-5012752-0-0	5012752-00			
2	2		1000016-00	100.0 MMF 100V 5%200PPM DM15S	2	C12,C19
3	3		1005306-00	6.8MFD 35V 10% S.TANT	5	C1,C8,C14,C16,C24
4	4		1012784-00	.047 MFD 50V -20+80 CER	28	C2-C7,C9,C10,C11,C13,C15,C17,C18,C20-C23,
					CONT	C25-C29,C31-C36
5	5		1110603-00	1N 5711 TM=100PS PIV= 70V HM8	1	D1
6	6		1209941-05	HEADER,100 10POS RT ANGLE	1	J1
7	7		1210711-02	HANDLE,MODULE,HEX	1	
8	8		1300316-00	470 1/4W 5% CC	1	R5
9	9		1300365-00	1 K 1/4W 5% CC	25	R1,R2,R3,R6-R10,R12,R14,R16,R17,R22-R29,
					CONT	R31-R35
10	10		1300479-00	10 K 1/4W 5% CC	12	R4,R11,R13,R15,R18,R19,R21,R30,R36-R39
11	11		1302941-00	14.7 K 1/4W 1% RN55D-F 100PPM	1	R20
12	12		1501999-00	DEC3009A NPN 300MW SI 20 25 M	1	Q1
13	13		1909701-00	74154 1 OF 16,BINA	1	E31
14	14		1909705-00	DEC 8881 NAND GATE-QUAD 2IN O	4	E4,E8,E19,E42
15	15		1909934-00	8266 MUS 1 OF 2 (QUAD)	2	E69,E79
16	16		1910393-00	DEC 7384 OR GATE-QUAD 2IN,UTI	4	E52,E53,E72,E75
17	17		1910537-00	74S11 AND GATE-TRIPLE 3INP	1	E27
18	18		1910544-00	74S74 FF-D DUAL,EDGE TRIGG	3	E32,E63,E65
19	19		1911330-01	74173N FF-D QUAD,TRI-STATE	11	E1,E62,E73,E90,E97,E98,E99,E118,E119,E121,
					CONT	E122
20	20		1911469-00	DEC 8640 RECEIVER,BUS,QUAD,U	7	E3,E11,E25,E41,E51,E61,E71
21	21		1911527-00	8097 BUFFER GATE-HEX 2INP	10	E37,E55,E83,E84,E91,E100,E101,E104,E105,
					CONT	E107
22	22		1911579-00	8641 TRANSCEIVER,BUS,QUA	3	E12,E13,E45
23	23		1911676-00	74S139 DECODER-DUAL TWO-INP	1	E120
24	24		1912388-00	74S02 NOR GATE-QUAD 2IN,PO	1	E64
25	25		1912649-00	LS75 LATCH 4BIT,BISTABLE	1	E26
26	26		1912661-00	74S189 MEMORY READ/WRITE	1	E82

REVISION HISTORY			SECTION 1 OF 1	RESP.ENG.: R.REGAN	DATE: 27-OCT-77	D I G I T A L
ENG	ECO NUMBER	REV	SECTION, VARIATION INDEX	MADE BY: TED KELLEY	DATE: 29-AUG-77	TITLE PARTS LIST
J.A	00001	C	1.00	CHECKED: N. GELARDERES	DATE:	PDP8 MEMORY MANAGEMENT BOARD
A.T	M8416-ML002	D	2.	DSN.ENG.: R. REGAN	DATE: 14-NOV-77	SIZE CODE DOCUMENT NUMBER REV
			3.	PROD.: MELVIN SCHENKE	DATE: 14-NOV-77	K PL M8416-0-DBP D
			4.	ASSEMBLY NUMBER: D-UA-M8416-0-0		EDIT #
			5.			PART NUMBER: M8416 36
			6.			
			7.			
			8.			
			9.			
			10.			
			11.			
			12.			

LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION		QTY	REFERENCE DESIGNATOR
27	27		1912697-00	LS174	FF-D HEX W/CLEAR	5	E15,E17,E85,E88,E103
28	28		1912796-00	74148	FXCODER,PRIORITY,8 T	1	E89
29	29		1912799-00	LS00	NAND-GATE-QUAD 2IN,P	8	E6,E18,E50,E54,E57,E66,E70,E94
30	30		1912800-00	LS01	NAND-GATE-QUAD 2IN,P	1	E20
31	31		1912801-00	LS02	NOR-GATE-QUAD 2IN	3	E29,E47,E48
32	32		1912803-00	LS04	INVERTER GATE-HEX 1I	8	E2,E5,E7,E22,E39,E44,E58,E115
33	33		1912805-00	LS08	AND GATE-QUAD 2IN,PO	2	E33,E67
34	34		1912807-00	LS10	NAND GATE-TRIPLE 3IN	5	E21,E24,E49,E56,E92
35	35		1912810-00	LS20	NAND GATE-DUAL 4IN	3	E9,E36,E43
36	36		1912815-00	LS30	NAND GATE-SINGLE 8IN	1	E30
37	37		1912817-00	LS37	NAND GATE-QUAD 2IN,P	1	E38
38	38		1912819-00	LS42	DECODER,BCD-DECIMAL	1	E34
39	39		1912824-00	LS74	FF-D DUAL,EDGE TRIGG	3	E59,E60,E76
40	40		1912828-00	LS85	COMPARATOR,4BIT MAGN	2	E68,E78
41	41		1912853-00	LS175	FF-D QUAD	8	E35,E46,E93,E102,E108,E110,E116,E117
42	42		1912858-00	LS221	ONE SHOT-DUAL,SCHMIT	1	E77
43	43		1912859-00	LS256	MUX 1 OF 2 (DUAL),	1	E23
44	44		1914087-00	8098	BUFFER GATE-HEX 2IN,	4	E86,E95,E96,E106
45	45		23211A1-00	A1-07		1	E80
46	46		23440A2-00	A2-05		1	E28
47	47		23441A2-00	A2-05		1	E74
48	48		23442A2-00	A2-05		2	E87,E113
49	49		23621A9-00	A9-01		3	E111,E112,E114
50	50		23007C6-00	C6-01		1	E14
51	51		23008C6-00	C6-01		1	E16
52	52		23009C6-00	C6-01		1	E81
53	53		23010C6-00	C6-01		1	E109
54	54		9000024-01	EYELET, ROLLED FLANGE, .121 OD X		12	
55	55		9105740-55	WIRE(WRAP)30AWG	UL1423	A/R	

56 NOTE: LINE 18: PARTS SUBSTITUTION LIST
57 NOTE: ITEM #18 1910544-01 74S74 FF-D DUAL (60 VERSION) QTY 3
58 NOTE: ITEM #18 1910950-00 74S74 FF-D DUAL (45 VERSION) QTY 3

D	I	G	I	T	A	L	TITLE	SECTION	SIZE	CODE	DOCUMENT NUMBER	REV
							PDP8 MEMORY MANAGEMENT BOARD	1 OF 1	K	PL	M8416-0-DBP	D

USER SIZE REG
74LS174 E88
P3 BD6 H
P3 BD7 H
P3 BD8 H
P3 BD9 H
P3 BDIØ H
P3 BD11 H
D5 D0 D1 D4 D2 D3 CLR CLK
R5(I) RØ(I) R1(I) R4(I) R2(I) R3(I)
P2 RST L
P3 BTP3 L
P4 LUSR L
74LSØ2 E29

P4 RUSR L
8Ø98 E1Ø6 (I) (15)
RD6 L
RD7 L
RD8 L
RD9 L
RDIØ L
RD11 L

RELOCATION REG
74LS174 E85
P3 BD7 H
P3 BD8 H
P3 BD9 H
P3 BDIØ H
P3 BD11 H
D5 D0 D1 D4 D2 D3 CLR CLK
R5(I) RØ(I) R1(I) R4(I) R2(I) R3(I)
P2 RST L
P3 BTP3 L
P4 LRR L
74LSØ2 E47

P4 RRR L
P1 RRØ H
P1 RR1 H
8Ø98 E86 (I)
RD7 L
RD8 L
RD9 L
RDIØ L
RD11 L

74LS85 E68
P3 BM5 H
B3 A3 B2 A2 B1 A1 BØ AØ
A>B A=B A<B
IN< IN= IN>
74LSØ2 E48
74LSØ4 E39
P1 OVER H

74LS85 E78
P3 BM9 H
P3 BM6 H
P3 BM7 H
P3 BM8 H
A<B A=B A>B
+5V
R21 1ØK

RELOCATION ROM
23442A2 E87
P6 USM H
AØ A1 A2 A3 A4 A5 A6 A7 ME1 ME2 D4 D3 D2 D1
P1 BFLØ H
P1 BFL1 H
P1 BFL2 H

RELOCATION ROM
23442A2 E113
P1 BBØ H
P1 BB1 H

READ VIRTUAL FIELD ROM
23621A9 E114
P6 USM H
P4 RDF L
P2 IFC H
P2 DFC H
A8 A7 A6 A5 A4 A3 A2 A1 AØ CE D3 D2 D1 DØ
P1 CRF H
RD6 L

READ VIRTUAL FIELD ROM
23621A9 E112
P2 DFA H
P2 IFA H
P2 DFB H
P2 IFB H
RD7 L
RD8 L

P4 RIF L
P4 RDF L
74LSØ8 E33
P1 ENRF L
E27 PIN 5

REVISIONS			
CHK	CHANGE NO.	REV.	
JA	M9416-0000	C	
	M8416-ML002	D	

DRN. TESLA 11-4-77
CHK 12/1/77
ENG 12-7-77
PROJ. ENG 12-7-77
PROD. 12-7-77
NEXT HIGHER ASSY. D-UA-M8416-0-0
SCALE
SHEET 1 OF 7

FIRST USED ON KT8-A

TITLE PDP8 MEMORY MANAGEMENT BOARD (PI)

SIZE D | CODE CS | NUMBER M8416-Ø-1 | REV. D

DIST.

P4 INT H — 74LSØ4 E115 — P4 DFEN (Ø) H, P3 BTS4 H — 74LSIØ E92 — P2 INT L

P4 NEW FLD H — 74LSØ4 E115

INSTRUCTION FIELD BUFFER — 74173 E97

P4 LET IO L

P1 BFLØ H — 8Ø98 E95

P1 BFL1 H — 8Ø98 E95

P1 BFL2 H — 8Ø98 E95

P4 RTF L, P4 RTS L — 74LS37 E38

P4 LXA H — 74LSØ2 E48

P3 BD6 H — 8Ø98 E96

P3 BD7 H — 8Ø98 E96

P3 BD8 H — 8Ø98 E96

P4 RMF L — 8Ø97 E1Ø7

P4 INT H, P4 CKIFB H, DATA ENA, OUT CONT, CLK, CLR

INSTRUCTION FIELD REG — 74LS175 E93

+5V — R35 1K, R34 1K, R29 1K

P2 IFA H, P2 IFB H, P2 IFC H

P4 CKIF H

+5V — R3Ø 1ØK

P1 BFLØ H — 8Ø98 E95

P1 BFL1 H — 8Ø98 E95

P1 BFL2 H — 8Ø98 E95

P3 BD9 H — 8Ø98 E96

P3 BDIØ H — 8Ø98 E96

P3 BDI1 H — 8Ø98 E96

P4 DFEN (I) H, P4 INIT EN (I) H — 74LSØØ E94

DATA FIELD REG — 74LS175 E1Ø2

P2 DFC H, P2 DFB H, P2 DFA H

P4 CKDF H

8Ø97 E1Ø4 — R33 1K, R32 1K, R28 1K

RD6 L, RD7 L, RDIØ L, RDI1 L

P6 DISF L

CPMA DISABLE L CUI

8Ø97 E1Ø1 — RD9 L, RDIØ L, RDI1 L

74LSI74 E1Ø3 — SAVE FIELD REG

P4 CKSV H

+5V

MAINT REG — 74173 E62 — DATA ENA, D3 D2 DI DØ, R3(I) R2(I) R1(I) R0(I) — RD9 L, RDIØ L, RDI1 L

P4 RMR L, P6 CKMR L, P3 BINIT H

EMA BUFF B — 74173 E73 — DATA ENA, D3 D2 DI DØ, R3(I) R2(I) R1(I) R0(I)

P2 EMAEN L, P3 BTP4 H

P3 BD6 H — 74LSØ4 E2

P3 BD7 H — 74LSØ4 E2

P3 BD8 H — 74LSØ4 E2

EMA BUFF B — 74173 E1 — DATA ENA, D3 D2 DI DØ, R3 (I) R2 (I) R1 (I) R0 (I) — AD2 EMAØ L, AE2 EMA1 L, AH2 EMA2 L

OUT CONT, CLK, CLR

P4 PLXA H, P4 PCLR H

P4 PLXA L — P2 ELAR L

74LS74 E63 — P2 ENBSL

P4 PCLR L — 74LSØ8 E67

R15 1ØK +5V

7384 E52 — P2 BCPMAD L

74LS74 E63 — P2 EMAEN H, P2 EMAEN L

P3 BTP4 H — P2 RST L

8Ø97 E1Ø5 — RD6 L, RD7 L, RD8 L, RD9 L, RDIØ L, RDI1 L

P4 GTS L, P4 RIB L, P4 GTF L — 74LSIØ E56 — 74LSØ4 E115 — P2 SUF OUT H — 74LS37 E38 — P2 RSB L

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
PDP8 MEMORY MANAGEMENT BOARD (P2)	D	CS	M8416-Ø-1	D
SCALE —	SHEET 2 OF 7	DIST.		

MD00 L AK1 8640 E11 → 74LS04 E5 → P3 BM0 H / P3 BM0 L
MD01 L AL1 8640 E11 → P3 BM1 H
MD02 L AM1 8640 E11 → 74LS04 E5 → P3 BM2 H / P3 BM2 L
MD03 L AP1 8640 E11 → 74LS04 E7 → P3 BM3 H / P3 BM3 L
MD04 L BK1 8640 E25 → 74LS04 E7 → P3 BM4 H / P3 BM4 L
MD05 L BL1 8640 E25 → P3 BM5 H
MD06 L BM1 8640 E25 → P3 BM6 H
MD07 L BP1 8640 E25 → P3 BM7 H
MD08 L DK1 8640 E71 → P3 BM8 H
MD09 L DL1 8640 E71 → 74LS04 E44 → P3 BM9 H / P3 BM9 L
MD010 L DM1 8640 E71 → P3 BM10 H / P3 BM11 H
MD011 L DP1 8640 E71 → 74LS04 E44 → P3 BM11 L

+5V

RD0 L R12 1K → 74LS04 E5 → P3 BD0 H
RD1 L R9 1K → 74LS04 E5 → P3 BD1 H
RD2 L R8 1K → 74LS04 E5 → P3 BD2 H
RD3 L R2 1K → 74LS04 E5 → P3 BD3 H

8641 E13 (DATA BUS XCEIVER)
AR1 DATA 00 L
AS1 DATA 01 L
AU1 DATA 02 L
AV1 DATA 03 L

RD4 L R1 1K → 74LS04 E7 → P3 BD4 H
RD5 L R6 1K → 74LS04 E7 → P3 BD5 H
RD6 L R7 1K → 74LS04 E7 → P3 BD6 H
RD7 L R31 1K → 74LS04 E7 → P3 BD7 H

8641 E12 (DATA BUS XCEIVER)
BR1 DATA 04 L
BS1 DATA 05 L
BU1 DATA 06 L
BV1 DATA 07 L

RD8 L R25 1K → 74LS04 E44 → P3 BD8 H
RD9 L R24 1K → 74LS04 E44 → P3 BD9 H
RDA L R26 1K → 74LS04 E44 → P3 BDA H
RDB L R27 1K → 74LS04 E44 → P3 BDB H

8641 E45 (DATA BUS XCEIVER)
DR1 DATA 08 L
DS1 DATA 09 L
DU1 DATA 10 L
DV1 DATA 11 L
INITIALIZE H CR1

AC BUFFER 74LS174 E17
P3 BD0 H → D0 R0 (1) → 2
P3 BD1 H → D1 R1 (1) → 5
P3 BD2 H → D2 R2 (1) → 7
P3 BD3 H → D3 R3 (1) → 10
P3 BD4 H → D4 R4 (1) → 12
P3 BD5 H → D5 R5 (1) → 15
CLR CLK

AC BUFFER 74LS174 E15
P3 BD6 H → D0 R0 (1) → 2
P3 BD7 H → D1 R1 (1) → 5
P3 BD8 H → D2 R2 (1) → 7
P3 BD9 H → D3 R3 (1) → 10
P3 BD10 H → D4 R4 (1) → 12
P3 BD11 H → D5 R5 (1) → 15
CLR CLK

74LS258 E23
A1 B1 A2 B2 A3 B3 A4 B4 SEL O/C
Y1 → RD3 L
Y2 → RD4 L
Y3 → RDA L
Y4 → RDB L

REARRANGE PLA 82S100 E16
D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 FE EN
R7 → RD0 L
R6 → RD1 L
R5 → RD2 L
R4 → RD5 L
R3 → RD6 L
R2 → RD7 L
R1 → RD8 L
R0 → RD9 L

P4 RACA L
P4 RACC L
P4 RACB L
P3 BINIT L
74LS20 E9 → 74LS04 E22
MBCT4 L → 74LS08 E33

TP2 H CE2 7384 E53 → 74LS04 E22 → P3 BTP2 L
P3 BINIT H
CR1 7384 E53 → 74LS04 E22 → 74LS10 E21

P3 BTP3 H → 74LS00 E6 → 74LS00 E6 → 74LS00 E6
P4 MBC L → 74LS04 E22
TS4 L CP2 8640 E51 → P3 BTS4 H

P3 MBK H
8881 E19 CV1 → MSIRDIS L
8881 E19 CU1 → CPMADIS L
8881 E4 BE2 → BREAK IN PROG L

INSTRUCTION DECODE PLA 82S100 E14
P3 BM0 H / P3 BM1 H → 74LS10 E21
F L DJ2 → 8640 E61 → P3 BF H
P4 LXA H / D L DK2 → 8640 E61 → P3 BD H
P3 BM2 H P3 BM3 H P3 BM4 H P3 BM5 H P3 BM6 H P3 BM7 H P3 BM8 H P3 BM9 H P3 BM10 H P3 BM11 H P3 BPAUSE H P6 RVFEN H P6 EEM H P6 USM H P6 DIOI H
D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 FE EN
R7 → P3 INIOEN H
R6 → P3 DECEN L
R5 → P3 CFROM L
R4 → P3 CITCEN L
R3 → P3 HOS L
R2 → 8881 E19 → CE1 C0 L
R1 → 8881 E19 → CH1 C1 L
R0 → 74LS01 E20 → P3 BTS3 H

RI0 1K → +5V
P3 BTS4 H / P3 MBK H → 74LS01 E20
P4 BTS1 H / P6 BIND2 H → 74LS01 E20

TP4 H CJ2 → 74S11 E27 → P3 BTP4 H
TP3 H CH2 → 8640 E51 → 74LS37 E38 → P3 BTP3 H / P3 BTP3 L
TS3 L CM2 → 8640 E51 → P3 BTS3 H
PULSELA H DR2 → 7384 E53 → P3 BPLA H
TP1 H CD2 → 7384 E53 → P3 BTP1 H

PAUSE L CD1 → 8640 E41 → 74LS75 E26
P4 BTS4 H → D1
D0 → R0 (1) → P3 BPAUSE H
R0 (0)
D1 → R1 (1) → P3 E2CFROM L
R1 (0)
ENB1 ← P3 BTP3 L

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
PDP8 MEMORY MANAGEMENT BOARD (P3)	D	CS	M8416-0-1	D
SCALE — SHEET 3 OF 7	DIST.			

P3 BM4 H
P3 BM9 L
74LS20 E43
P4 LXM L
P3 BM11 L
74LS20 E36
P4 GTF L
P3 BM4 L
P3 BM9 H
P3 BM11 H
P3 INIOEN H
74LS20 E36
P4 RTF L

74LS10 E24
8881 E42
10 CLI
INTERNAL IO

P4 INT IN H
P4 USINT H
74LS37 E38
P4 FATAL L
74S74 E32
P4 FATAL (0) H

P4 GTF L
74LS00 E18
8881 E8
RD3 L

8266 E79
A3 B3 A2 B2 A1 B1 A0 B0
F3 F2 F1 F0 S1 S0
P4 CKIFB H
P4 CKIBB H
P4 CKIF H
P4 CKDF H

(DEV CODE 17)
74LS42 E34
P3 CI7EN L
P3 BM9 H
P3 BMI0 H
P3 BM11 H
D3 D2 D1 D0
F9 F8 F7 F6 F5 F4 F3 F2 F1 F0
P4 RACC L
P4 RACB L
P4 RACA L
P4 MBC L
P4 RMR L
P4 RLB L
P4 RBM L
P4 LBM L

8266 E69
A3 B3 A2 B2 A1 B1 A0 B0
F3 F2 F1 F0 S1 S0
P4 CKDB H
P4 CKUFB H
P4 CKUF H

P3 BTP3 H
74LS02 E29
D 74LS75 E26 C 0
P3 BTS3 H
P4 BLBM L

(DEV CODE 20-30)
74154 E31
F0 F1 F2 F3 F4 F5 F6 F7 F8 F9 F10 F11 F12 F13 F14 F15
P4 GTS L
P4 RTS L
P4 RXM L
P4 LRR L
P4 RRR L
P4 LUSR L
P4 RUSR L
P4 CINT L
P4 RDF L
P4 RIF L
P4 RIB L
P4 SINT L
P4 CUF L
P4 SUF L
STB1 STB0
P3 BM8 H
P3 BM7 H
P3 BM6 H
P3 BM9 H
D0 D1 D2 D3
74LS00 E70
R4 RMF L

REGISTER CLOCK CONTROL ROM
23211A1 E80
A4 A3 A2 A1 A0 CE
D8 D7 D6 D5 D4 D3 D2 D1
P4 NEW FLD H

P3 BM3 L
P3 BF H
P3 BM1 H
P3 BM0 L
74LS10 E49
74LS02 E29
74LS00 E70
P4 SUF L
74LS08 E67

IR1 L
DE2
IRQ L
DD2
8640 E61
P3 BD H
P4 JMP+JMS H

P6 USM H
P1 OVER H
P3 BTP3 H
74LS00 E70
74LS10 E49
74LS08 E67

LA ENABLE L
KEY CONTROL L
BM2
DU2
8640 E51
P4 LXA H
P3 PLA H
74LS00 E57
74LS04 E58
P4 PLXA H

INT IN PROG L
BP2
8640 E3
P4 INT IN PROG L
74LS02 E29
P4 INT H
P3 BTP4 H
74LS00 E57
74LS10 E49
P4 PLXA L
74LS04 E58
P4 CKSV H

MAMS LOAD CONTROL H
BH2
8640 E3
F SET H
DP2
7384 E75

P4 PCLR L
P3 MOS L
74LS10 E24
P3 BF H
P6 USM H
P3 BM0 H
P3 BM1 H
P3 BI 2 L
P6 DIOT L
P4 LET IO L
74LS30 E30

P4 FATAL L
8881 E4
P4 INT IN PROG L
P4 INT IN H
74LS00 E57
74LS00 E57
74LS00 E57

P4 NEW FLD H
P3 BTP3 H
74LS00 E18
74LS00 E18
74LS20 E9
P4 INT INH L
74LS08 E33
P4 CUMB L

P4 CUF L
74LS04 E22

P4 JMP+JMS H
P3 BD H
74LS04 E58
74LS00 E66
74LS08 E67
74LS00 E66
R19 10K
+5V
74LS74 E76
DATA FIELD EN
P4 DFEN (1) H
P3 BTP3 H
P4 DFEN (0) H

P3 BM6 H
P3 BM7 H
P3 BM8 H
74LS10 E21
CHANGE FIELD DECODE
23440A2 E28
A7 A6 A5 A4 A3 A2 A1 A0
D4 D3 D2 D1
ME1 ME2
R14 1K
R3 1K
R16 1K
R17 1K
+5V
P4 CDF L
P4 CIF L
P6 EN5 H
P6 EN9 H
P3 BM4 H
P3 BM5 H
P3 BM9 H
P3 BM10 H
P3 BM11 H
P3 E2CFROM L
P3 CFROM L

P3 BM9 H
P6 EEM L
74LS02 E47
74LS02 E47
P3 DECEN L
74LS02 E47
74LS04 E39

C12 100PF
D1 IN5711
CDI
PAUSE L
R5 470
Q1 3009A
74S02 E64
P3 BTS3 H
74S02 E64

RUN L
BU2
8640 E41
P4 LET IO L
POWER OK L
BV2
8640 E41
74LS00 E66

C19 100PF
R20 14.7K
5%
74LS221 E77
P4 PCLR H

R18 10K
+5V
P6 MAINT H
P4 NEW FLD H
74LS00 E18
D 74LS74 E76 C 0
P4 INIT EN (1) H
P4 INIT EN (0) H

LAEN L
BM2
8640 E41
TSI L
CK2
8640 E41
P4 BTSI H

74LS04 E39
74LS10 E24
P4 CINT L
74LS08 E33
74LS04 E2
P3 BTP3 H
USER INT FF
R4 10K
+5V
D 74S74 E32 C 0
P3 BINIT L
P4 SINT L
74LS04 E22

8881 E42
CPI
INT RQST
P4 USINT H
8881 E42
CSI
SKIP L

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	PDP8 MEMORY MANAGEMENT BOARD (P4)	SIZE	CODE	NUMBER
		D	CS	M8416-0-1
SCALE	SHEET 4 OF 7	DIST.		REV. D

BANK SELECT ROM
2364|A2
E74
P4 INT IN PROG L
P4 DFEN (I) H
P4 INIT EN (Ø) H
P2 BCPMAD L
P3 BTS4 H
P3 BPAUSE H
P6 EBM H
LBM + RBMN
IBS L
P5 DBS L
P5 BMEN L
FORCE Ø L

74148
E89
P4 NEW FLD H
P4 LXA H
74LS04
E115
E39
P4 CIF L
P4 CDF L
P4 RTS L
P4 RMF L

BANK SELECT MUX PLA
82S1Ø0
E109
MUX CØ H
MUX C1 H
MUX C2 H
SBØ L
SB1 L
SB2 L
SB3 L
IBB Ø H
IBB 1 H
P1 BBØ H
P1 BB1 H
P3 BD1 H
P3 BD2 H
P3 BD3 H
P3 BD4 H
P3 BD5 H
FE EN

INSTRUCTION BANK REG
74LS175
E11Ø
P4 CKIF H
CLR CLK

DATA BANK REG
74LS175
E1Ø8
P4 CKDB H

INSTRUCTION BANK BUFF
74LS175
E116
P4 CKIBB H
R36
1ØK
+5V

8Ø97
E1Ø1
E91
P6 DISPB L
RD1 L
RD2 L
RD4 L
RD5 L

74S139
E12Ø
P5 IBSØ L
P5 IBS1 L
P5 IBS2 L
P5 IBS3 L

SAVE BANK REG
74LS175
E117
P4 CKSV H

READ VIRTUAL FIELD ROM
2362|A9
E111
P1 RR1 H
P1 RRØ H
P1 CRF H
P4 RDF L
P6 USM H
P1 ENRF L
RD9 L
RD5 L

P2 RSB L
8Ø97
E1ØØ
RD4 L
RD3 L
RD2 L
RD1 L
P4 RBM L
RDIØ L
RD11 L

BREAK MAP ADDRESS PLA
82S1Ø0
E81
P3 BTS4 H
P4 RBM L
P4 LBM L
P3 BDØ H
P3 BD1 H
P3 BD2 H
P3 BD3 H
P3 BD4 H
P3 BD5 H
P3 BD6 H
P3 BD7 H
P3 BD8 H
P3 BD9 H
P3 BDIØ H
P3 BD11 H

BREAK MAP
74S189
E82
P4 BLBM L
R22
1K
R23
1K
+5V

LAST BREAK REG
74173
E9Ø
DATA ENA
P4 RLB L
P3 BTP4 H
P3 BINIT H
RD6 L
RD7 L
RD8 L
RD9 L

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
PDP8 MEMORY MANAGEMENT BOARD (P5)	D	CS	M8416-Ø-1	D
SCALE — SHEET 5 OF 7	DIST.			

74173 E119 — REMOTE BANK SELECT REG B
P5 IBSØ L, P5 IBS1 L, P5 IBS2 L, P5 IBS3 L
P6 EMAEN H — 74S02 E64
P3 BTP4 H
74173 E118 — LOCAL BANK SELECT REG B
P6 PRUPL, P2ENBSL
EB2 P6 BSØ L, ED2 P6 BS1 L, EL2 P6 BS2 L, ER2 P6 BS3 L
J1 — RBSØ L, RBS1 L, RBS2 L, RBS3 L
R37 R38 R39 R11 10K, +5V
AA2, BA2, CA2 — +5V
C1, C8, C14, C16, C24, 6.8UF, 35V
C2 THRU C7, C9, C10, C11, C13, C15, C17, C18, C20 THRU C23, C25 THRU C29, C31 THRU C36 .047UF, 50V
AC1, AT1, AF1, AN1, AC2, AT2, AF2, AN2, BC1, BT1, BF1, BN1, BC2, BT2, BF2, BN2, CC1, CT1, CF1, CN1, CC2, CT2, CF2, CN2, DC1, DT1, DF1, DN1, DC2, DT2, DF2, DN2, EC2, FC2, ET1, FT1,
MAINT REG 74173 E99 — P4 RMR L — RD1 L, RD2 L, RD3 L, RD4 L
MAINT REG 74173 E98 — P6 CKMR L, P3 BINIT H — RD5 L, RD6 L, RD7 L, RD8 L
REMOTE BANK SELECT REG A
P2 ELAR L
74173 E122
74173 E121
74S139 E120 — P3 BD1 H, P3 BD2 H, ENB2
LOCAL BANK SELECT REG A
P4 PLXA H, P4 PCLR H
8097 E55, 8097 E56
P4 PCLR L — 74S74 E65 — P3 BTP4 H — P6PRUPL
P4 PLXA L

EXTENDED MODE REG 74LS175 E35
P3 BDØ H, P3 BD1 H, P3 BD2 H, P3 BD3 H
P6 EEM H, P6 EEM L, P6 EN5 H, P6 EN5 L, P6 EN9 H, P6 EN9 L, P6 RVFEN H, P6 RVFEN L
P4 LXM L, P3 BTP3 L — 74LSØ2 E48 — P2 RST L
EXTENDED MODE REG 74LS175 E46
P3 BD4 H, P3 BD5 H, P3 BD6 H
P6 DIOI H, P6 DIOI L, P6 EBM H, P6 EBM L
P6 MAINT L — 74LSØ2 E48 — P4 INT INH L — P6 MAINT H
LINK L, AV2 — 8640 E3 — 8881 E4 — RDØ L
P4 GTF L, P4 GTS L — 74LSØØ E6

INDI L, CU2 — 7384 E72 — 74S04 E113 — 74LS10 E92 — P6 DISPB L
74LSØØ E94 — P6 DISF L
IND2 L, CV2 — 7384 E72 — P6 IND2 H
P4 BTSI H — 74LS10 E92
P4 FATAL (Ø) H — 8097 E83 — RD3 L
P6 USM L — 8097 E83 — RD5 L

P4 RXM L
P6 EEM L — 8097 E55 — RDØ L
P6 EN5 L — 8097 E37 — RD1 L
P6 EN9 L — 8097 E37 — RD2 L
P6 RVFEN L — 8097 E37 — RD3 L
P6 DIOI L — 8097 E37 — RD4 L
P6 EBM L — 8097 E37 — RD5 L
P6 MAINT L — 8097 E37 — RD6 L

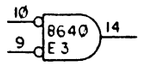
P3 BTP2 L — 74LSØØ E54
P5 DBS L, P5 BMEN L — 74LSØØ E54 — P3 BTP4 H — 74LS10 E56
P3 BTP3 H, P6 MAINT H, P4 NEW FLD H — 74LS10 E56
P3 BTP1 H — 74LSØØ E54 — P6 CKMR L

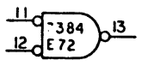
P3 BD5 H — 74LSØØ E50
P4 RMF L — 74LS04 E39 — 74LSØØ E50
P4 SUF L — 74LS04 E39
P3 BTP3 H — 74LSØØ E50
P4 CKUFB H — 74LS74 E60 UMB
P4 CKUF H, P4 CUMB L — 74LS74 E59 UMFF
+5V — R13 10K
P6 USM H
P6 DIOI L, PI ENRTL — 74S11 E27 — 8881 E8
P3 BM2 H — 8881 E8 — DM2 — USER MODE L
SVUF
P4 CKSV H — 74LS74 E59
P6 USM L
P2 SUF OUT H — 8881 E8 — RD5 L

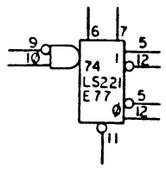
REVISIONS		
CHK	CHANGE NO.	REV.

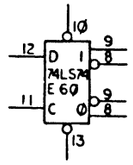
TITLE	SIZE	CODE	NUMBER	REV.
PDP8 MEMORY MANAGEMENT BOARD (P6)	D	CS	M8416-0-1	D
SCALE —	SHEET 6 OF 7	DIST.		

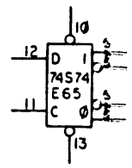
SPARES

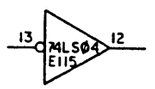


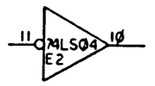


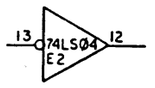


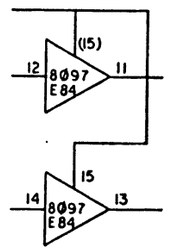






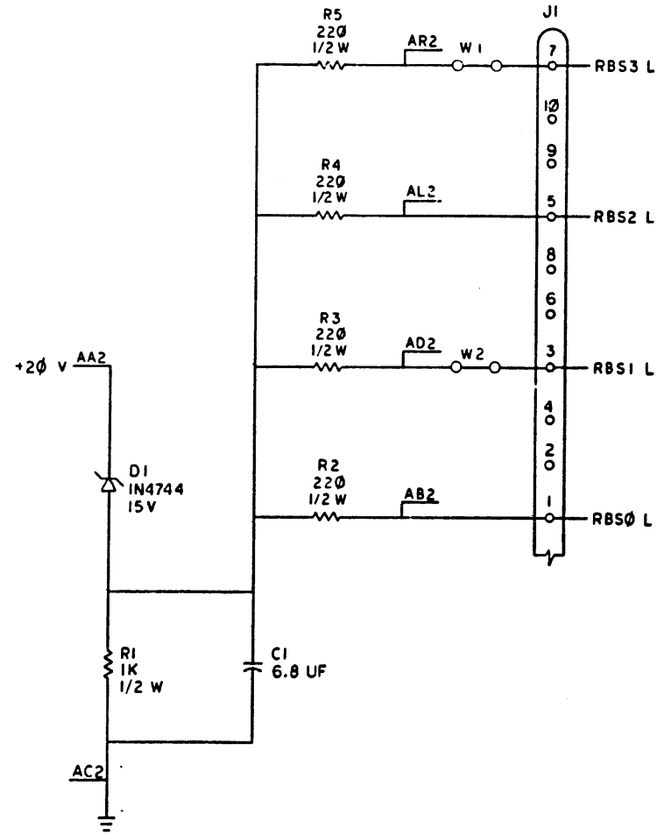






REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
PDP8 MEMORY MANAGEMENT BOARD	D	CS	M8416-0-1	D
SCALE — SHEET 7 OF 7	DIST.			



REVISIONS	CHK	CHANGE NO.	REV.

DRN.	11-9-77	FIRST USED ON KT8-A
CHK.	12/7/77	
ENG.	12-7-77	TITLE
PROJ. ENG.	12-7-77	KT8-A TERMINATOR
PROD.	12-7-77	
NEXT HIGHER ASSY.	D-UA-M9020-Ø-Ø	SIZE D · CODE CS · NUMBER M9020-Ø-1 · REV. *
SCALE		
SHEET 1 OF 1		DIST.