## IDENTIFICATION

| | |
|---|---|
| Product Code: | Maindec 802 |
| Product Name: | Memory Checkerboard Test |
| Date Created: | September 1, 1965 |
| Maintainer: | Diagnostic Group |

## 1. ABSTRACT

Maindec 802 tests memory for core failure on half-selected lines under the worst possible conditions for reading and writing. It is used primarily for testing the operation of memory at marginal voltages.

## 2. REQUIREMENTS

### 2.1 Storage

There are two versions of Maindec 802. The Low End program occupies registers 0003-0111 octal and tests memory from 0112-~~7777~~ 7700 octal.

The High End program occupies registers 7450-7555 octal and tests memory from 0000-7447 octal.

Both programs require the RIM Loader to be in registers 7756-7776 octal.

### 2.2 Equipment

Standard PDP-8

## 3. USAGE

### 3.1 Loading

Turn off the Teletype reader.

Set the SWITCH REGISTER to 7756.

Press LOAD ADDRESS; then START.

Place the desired RIM program tape in the reader and turn on the reader.

When the program has been loaded, stop the computer, turn off the reader, and remove the tape.

### 3.2 Switch Settings

Starting Addresses

0001 Low End Checkerboard
7450 High End Checkerboard

### 3.3 Program Control Settings

One of the four possible patterns that can be written in memory is obtainable by each of the following SR settings:

| | |
|---|---|
| 0100 | (This setting is used for the standard PDP-8 core unit.) |
| 0000 | (These are for special core |
| 0001 | units from other suppliers. |
| 0021 | See paragraph 5.2.) |
| 0101 | (This setting is used for Type 185, 186 and MM08 Memories.) |

For most PDP-8's, the setting of 0100 should be used.

## 3.4 Start-up and/or Entry

With the program in memory, set the SWITCH REGISTER to the starting address, 0001 for Low End or 7450 for High End.

Press LOAD ADDRESS.

Set the SWITCH REGISTER to one of the four settings given in paragraph 3.3 to obtain the correct pattern. For most PDP-8's, this will be 0100.

Press START.

## 3.5 Errors in Usage

The contents of a given memory cell should be either 7777 or 0000. An error occurs if a 1 becomes a 0, or vice versa. The following pair of stops occur for each error. Two addresses are given for each stop; the first is for the Low End Test, the second for the High End Test.

| C(MA) | Error | Cause for Error |
|---|---|---|
| 0071<br>7536 | E1 | Memory cell does not contain 7777 or 0000.<br>AC displays contents of cell in error. |
| 0074<br>7541 | E1A | AC contains address of cell causing previous error stop. |

## 3.6 Recovery from Such Errors

| Error | Recovery Procedure |
|---|---|
| E1 | Record the C(AC). Press CONTINUE to reach the next halt. |
| E1A | Record the C(AC). Press CONTINUE to resume testing. |

The errors detected by the Checkerboard Test are not usually traceable to modules which the operator can easily replace. The test is of primary value to the field service engineer in checking out the performance of the memory and its associated circuits under marginal voltage conditions. Nonetheless, the checkerboards are useful for cursory checks during normal maintenance testing.

## 4. RESTRICTIONS

4.1 The Low End Test requires the presence of the RIM Loader in upper memory, but destroys the Loader during the course of the test. The operator must remember to restore the RIM Loader after the Low End Test has been run.

There are no restrictions on the use of the High End Test.

## 5. DESCRIPTION

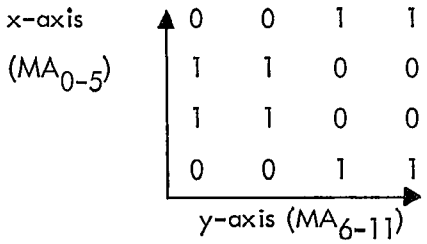
### 5.1 Discussion

In a standard core plane, a given core is selected when the combined currents of the x- and y-selection lines produce a magneto motive force which exceeds the threshold for reversing the flux direction of the core. This occurs at the intersection of the activated selection lines. However, all other cores which are threaded onto the activated lines will be slightly disturbed. Under marginal voltage conditions, such half-selected cores might also reverse polarity if their states are properly established by the pattern which the Checkerboard Test writes into memory.

When a selected core is in the 1 state, the read current will cause it to reverse polarity and become 0. When the core is in the 0 state, the write current will cause it to become 1. Thus, the possibility of a reading error is greatest when all the half-selected cores are in the 1 state; a writing error is most probable when all the half-selected cores are in the 0 state.

If a half-selected core changes polarity, the error will be detected when the memory register containing that core is tested by the program. For a reading error, the contents of that core will appear as a 0 in a field of 1's, and vice versa for a writing error.

Every Checkerboard Test pattern consists of alternating pairs of memory cells, one pair containing 7777's the other containing 0000's. Since memory manufacturers wire their core stacks in different ways, the same pattern of alternations cannot be used for every type of core, and still allow a "worst case" condition, that is, one in which all half-selected cards undergo the greatest possible disturbance which can occur when testing memory. The following pattern is used for the Ferroxcube memories with which most PDP-8's are provided.



Since the Y-axis selection lines are conditioned by the low-order six bits of the memory address register ($MA_{6-11}$), and the X-axis lines by the high-order bits ($MA_{0-5}$), the above array is interpreted as follows: (X- and Y-axis should be interpreted as shown above).

Positions on the X-axis represent consecutive locations in memory from 00-77.

Positions on the Y-axis represent consecutive $100_8$'s. Thus, the lower left corner represents location 0000. This position contains a 0, which means that the contents of the entire memory cell at address 0000 are 0. Likewise, the contents of memory cell 0201 are 1's or 7777; this is determined by reading the third row up on the X-axis, and across one position on the Y-axis.

The pattern in memory appears as follows:

| Address | Contents |
|---|---|
| 0000 | 0000 |
| 0001 | 0000 |
| 0002 | 7777 |
| 0003 | 7777 |
| 0004 | 0000 |
| 0005 | 0000 |
| 0006 | 7777 |
| 0007 | 7777 |
| .... | .... |

From the pattern matrix, we see that after $77_8$ registers the pattern will reverse itself, thus:

| Address | Contents |
|---|---|
| 0076 | 7777 |
| 0077 | 7777 |
| 0100 | 7777 |
| 0101 | 7777 |
| 0102 | 0000 |
| 0103 | 0000 |
| 0104 | 7777 |
| 0105 | 7777 |
| 0106 | 0000 |
| 0107 | 0000 |
| .... | .... |

And so on through memory. The pattern reverses every $100_8$ registers.

## 5.2 Pattern Generator

The patterns generated by the other three switch register settings are defined by the following pattern matrices.

| SR Setting | | Pattern Matrix |
|---|---|---|
| 0000 | X-axis | 1 1 0 0<br>1 1 0 0<br>0 0 1 1<br>0 0 1 1<br>Y-axis |
| 0001 | X-axis | 1 0 0 1<br>1 0 0 1<br>0 1 1 0<br>0 1 1 0<br>Y-axis |
| 0021 | X-axis | 0 1 1 0<br>1 0 0 1<br>1 0 0 1<br>0 1 1 0<br>Y-axis |
| 0101 | X-axis | 1 0 0 1<br>0 1 1 0<br>0 1 1 0<br>1 0 0 1<br>Y-axis |

## 6. METHODS

### 6.1 Discussion

The program writes the pattern into the area of memory to be tested. It then tests each word as follows:

The contents of the word are checked for incorrect bits.

The contents are complemented, deposited in the same register, and retested for incorrect bits.

The original contents are returned to the register, and the next one is checked.

After all of memory is tested, the program then writes the complement of the pattern and proceeds to check as before. In this way, every core is tested for errors that might occur when it is read and when information is written into it.

# 7. PROGRAM

## 7.1 Program Listing

### 7.1.1 Low End

```
                /MAINDEC 802:    PDP-8 CHECKERBOARD

                *1                      /LOW END TEST
0001  7121              CLL CML IAC
0002  3107              DCA COM

0003  7604  STX,        LAS
0004  1111              TAD MUD
0005  3105              DCA PAT
0006  1111              TAD MUD
0007  3106              DCA SA

0010  2107  STB,        ISZ COM
0011  1107              TAD COM
0012  0103              AND DOT             /2
0013  7640              SZA CLA
0014  1102              TAD NOT             /10
0015  1077              TAD HOT
0016  3025              DCA Y               /COMPLEMENT THE PATTERN

0017  1101  STC,        TAD POT             /100
0020  1106              TAD SA              /TEST FOR FINAL ADDRESS
0021  7650              SNA CLA
0022  5003              JMP STX
0023  1105              TAD PAT
0024  0100              AND ROT             /200

0025  0000  Y,          0
0026  1102              TAD NOT             /Y LINE PRESETS X LINE
0027  1077              TAD HOT             /TO SNA OR SZA
0030  3033              DCA X
0031  1105              TAD PAT
0032  0103              AND DOT             /2

0033  0000  X,          0
0034  7040              CMA
0035  7420              SNL
0036  5047              JMP CCK
0037  3506              DCA I SA            /STORE PATTERN AND RECOMPLEMENT

0040  2106  STD,        ISZ SA              /WORD WHEN CHECKING
0041  2105              ISZ PAT
0042  1106              TAD SA
```

```
0043  0104          AND BOT          /77
0044  7650          SNA CLA
0045  5017          JMP STC
0046  5031          JMP X-2

0047  3110  CCK,    DCA WRD          /CHECK PATTERN
0050  1506          TAD I SA
0051  7041          CMA IAC
0052  1110          TAD WRD
0053  7640          SZA CLA
0054  5070          JMP CC3          /ERROR IN CORE
0055  1110          TAD WRD
0056  7040          CMA
0057  3506          DCA I SA         /COMPLEMENT THE WORD
0060  1506          TAD I SA         /IN CORE
0061  7001          IAC
0062  1110          TAD WRD
0063  7640          SZA CLA          /TEST COMPLEMENT WORD
0064  5070          JMP CC3          /ERROR

0065  1110  CC2,    TAD WRD
0066  7100          CLL
0067  5037          JMP STD-1

0070  1506  CC3,    TAD I SA         /ERROR: AC CONTAINS INCORRECT WORD
0071  7402  E1,     HLT
0072  7200          CLA
0073  1106          TAD SA           /AC CONTAINS ADDRESS OF
0074  7402  E1A,    HLT              /REGISTER IN ERROR
0075  7300          CLA CLL

0076  5065  CC4,    JMP CC2

0077  7640  HOT,    7640             /CONSTANTS
0100  0200  ROT,    200
0101  0100  POT,    100
0102  0010  NOT,    10
0103  0002  DOT,    2
0104  0077  BOT,    77

0105  0000  PAT,    0                /VARIABLES
0106  0000  SA,     0
0107  0000  COM,    0
0110  0000  WRD,    0
0111  0112  MUD,    .+1
```

```
BOT     0134
CCK     0047
CC2     0065
CC3     0070
CC4     0076
COM     0107
DOT     0103
EI      0071
EIA     0074
HOT     0077
MUD     0111
NOT     0102
PAT     0105
POT     0101
ROT     0100
SA      0106
STB     0010
STC     0017
STD     0040
STX     0003
WRD     0110
X       0033
Y       0025
```

7.1.2 High End

```
                /MAINDEC 802:     PDP-8 CHECKERBOARD
                *7450

7450  7121              CLL CML IAC          /HIGH END TEST
7451  3353              DCA COM

7452  7604  STX,        LAS
7453  3354              DCA PAT
7454  3355              DCA SA

7455  2353  STB,        ISZ COM
7456  1353              TAD COM
7457  0352              AND DOT              /2
7460  7640              SZA CLA
7461  1351              TAD NOT              /10
7462  1350              TAD HOT
7463  3272              DCA Y                /COMPLEMENT THE PATTERN

7464  1347  STC,        TAD SOT              /400
7465  1355              TAD SA               /TEST FOR FINAL ADDRESS
7466  7650              SNA CLA
7467  5252              JMP STX
7470  1354              TAD PAT
7471  0346              AND ROT              /200
```

```
7472  0000  Y,     0
7473  1351         TAD NOT          /10-Y LINE PRESETS
7474  1350         TAD HOT          /X LINE TO SNA OR SZA
7475  3300         DCA X
7476  1354         TAD PAT
7477  0352         AND DOT          /2

7500  0000  X,     0
7501  7040         CMA
7502  7420         SNL
7503  5314         JMP CCK
7504  3755         DCA I SA         /STORE PATTERN AND THE COMPLEMENT

7505  2355  STD,   ISZ SA           /WORD WHEN CHECKING
7506  2354         ISZ PAT
7507  1355         TAD SA
7510  0345         AND BOT          /77
7511  7650         SNA CLA
7512  5264         JMP STC
7513  5276         JMP X-2
7514  3356  CCK,   DCA WRD          /CHECK PATTERN
7515  1755         TAD I SA
7516  7041         CMA IAC
7517  1356         TAD WRD
7520  7640         SZA CLA
7521  5335         JMP CC3          /ERROR IN CORE
7522  1356         TAD WRD
7523  7040         CMA
7524  3755         DCA I SA         /COMPLEMENT THE WORD
7525  1755         TAD I SA         /IN CORE
7526  7001         IAC
7527  1356         TAD WRD
7530  7640         SZA CLA          /TEST COMPLEMENT WORD
7531  5335         JMP CC3          /ERROR

7532  1356  CC2,   TAD WRD
7533  7100         CLL
7534  5304         JMP STD-1
7535  1755  CC3,   TAD I SA
7536  7402  E1,    HLT              /ERROR:AC CONTAINS
7537  7200         CLA              /INFORMATION IN ERROR
7540  1355         TAD SA
7541  7402  E1A,   HLT              /AC CONTAINS ADDRESS OF
7542  7300         CLA CLL          /REGISTER IN ERROR
7543  7300         CLA CLL
7544  5332  CC4,   JMP CC2
```

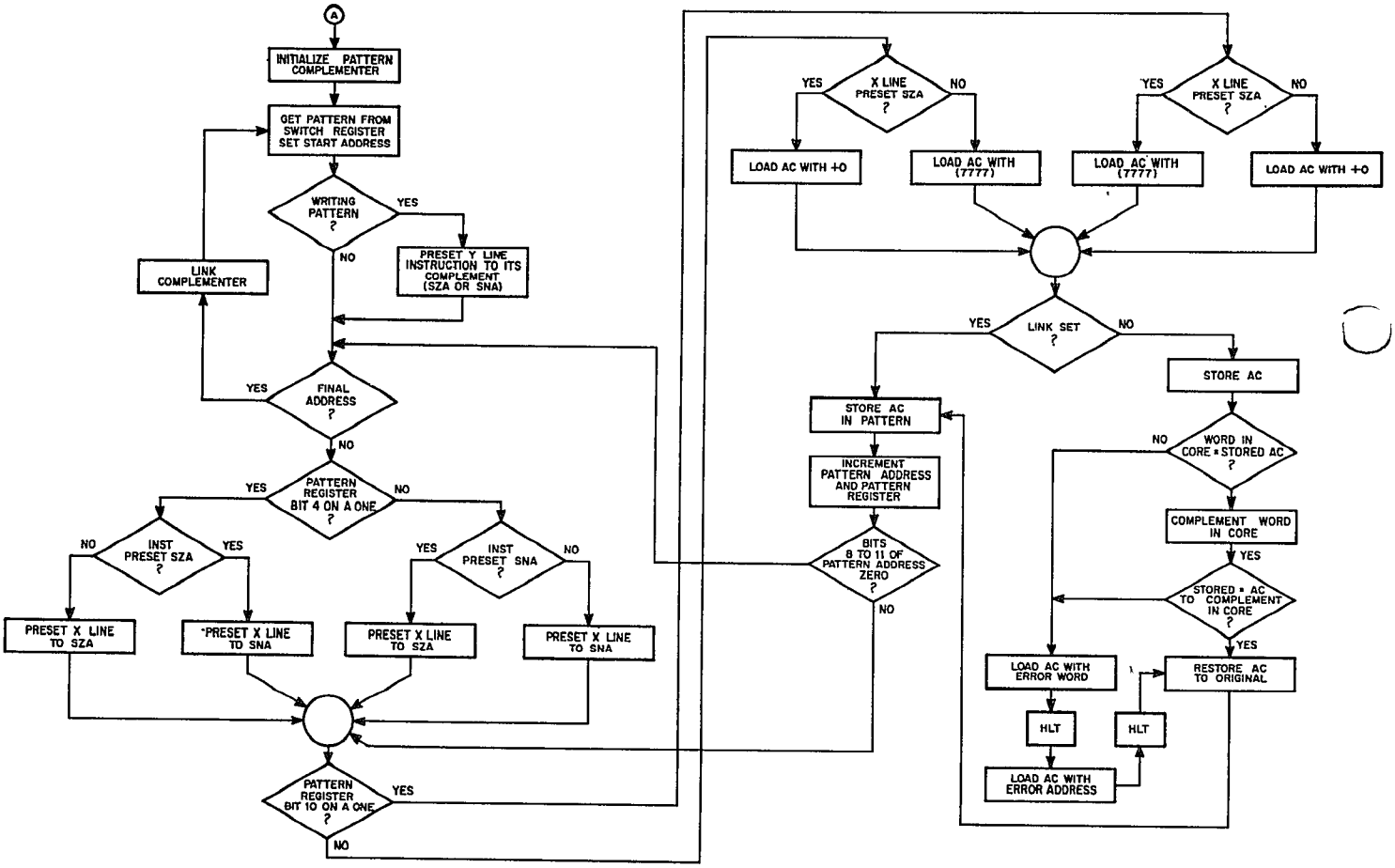
```
7545  0077  BOT,    77
7546  0200  ROT,    200
7547  0400  SOT,    400
7550  7640  HOT,    7640
7551  0010  NOT,    10
7552  0002  DOT,    2

7553  0000  COM,    0                    /VARIABLES
7554  0000  PAT,    0
7555  0000  SA,     0
7556  0000  WRD,    0
```

```
BOT     7545
CCK     7514
CC2     7532
CC3     7535
CC4     7544
COM     7553
DOT     7552
E1      7536
E1A     7541
HOT     7550
NOT     7551
PAT     7554
ROT     7546
SA      7555
SOT     7547
ST5     7455
STC     7464
STD     7505
STX     7452
WRD     7556
X       7500
Y       7472
```

8. DIAGRAM

8.1 Flow Chart




9. REFERENCES (Not Applicable)