IDENTIFICATION

Product Code: MAINDEC 08-D1DA-D

Product Name: Extended Memory Checkerboard - Part 2

Date Created: September 8, 1965

Maintainer: Diagnostic Group

Previous Code: MAINDEC 820-2

1. ABSTRACT

MAINDEC 08-D1DA-D is a preliminary test for core memory failures on half-selected lines under worst-case conditions of reading and writing. It is used to test memory module X while running the program in memory module Y. This is applicable for test of Type 184 Memory Modules and MM08 Memory Modules.

MAINDEC 08-D1CA-D will also test the control portion of the Extended Memory Type 138 or Extended Memory Type 185.

2. REQUIREMENTS

Storage

The program occupies registers 0000_8 - 0111_8 and tests memory from 0000_8 - 7776_8.

The RIM Loader must be in registers 7756_8 - 7776_8.

Subprograms and/or Subroutines

High RIM Loader, Binary Loader Digital-8-2-U-RIM

Equipment

Standard PDP-8 and Extended Memory Module Type 183.

3. USAGE

3.1 Loading

If the Binary Loader is in memory, go to the Extended Memory Checkerboard Test. Otherwise, the RIM Loader and/or the Binary Loader must be loaded into memory.

The Extended Memory Checkerboard Test may now be loaded as follows:

Set 7777_8 in the SWITCH REGISTER
Press LOAD ADDRESS key
Place object tape in the ASR 33
Press START key on the operator console
Engage reader

3.2 Switch Settings

Starting address: 0000_8 DF(X), IF(X).

Program Control Settings - One of four possible patterns that can be written is obtainable by each of the following SR settings.

0100_8	This setting is used for the standard PDP-8 unit.
0000^8	These are used for special core units from other supplies.
0001	(Reference section 5.2.)
0101	This setting is used for Type 185, 186 or MM08 Memories of the PDP-8.

3.3 Start up and/or Entry

With the program in the desired memory field set the following:

a. Load address 0000_8. Load the data field and instruction field of the memory containing the object program.

b. Set the instruction CDF (62N1) to the field to be tested in the SWITCH REGISTER.

c. Press DEPOSIT.

d. Repeat step a.

e. Reference Program Control Settings (section 3.2).

f. Press START.

3.4 Errors in Usage

The contents of a given memory cell should be either 7777 or 0000. An error occurs if a 1 becomes a 0, or vice versa. The following pair of stops occurs for each error:

C(MA)	Error	Cause of Error
0071	E1	Memory cell does not contain 7777 or 0000. AC displays contents of cell in error.
0074	E1A	AC contains address of cell causing previous error stop.

3.5 Recovery from Such Errors

Error	Recovery Procedure
E1	Record the C(AC). Press CONTINUE to reach the next halt.
E1A	Record the C(AC). Press CONTINUE to resume testing.

4. RESTRICTIONS

This program is only a preliminary test and should only be used to simplify memory adjustments and maintenance procedures.

Maindec 802* should be loaded into the memory module under test for a final test. (Reference Maindec 802* for usage)

5. DESCRIPTION

5.1 Discussion

* See Appendix

In a standard core plane, a given core is selected when the combined voltages of the x- and y- selection lines exceed the threshold voltage for reversing the polarity of the core. This occurs at the intersection of the activated selection lines. However, all other cores which are threaded onto the activated lines will be slightly disturbed. Under marginal voltage conditions, such half-selected cores may also reverse polarity if their states are properly established by the pattern which the Checkerboard Test writes into memory.

When a selected core is in the 1 state, the read current causes it to reverse polarity and become 0. When the core is in the 0 state, the write current causes it to become 1. Thus, the possibility of a reading error is greatest when all the half-selected cores are in the 1 state; a writing error is most probable when all the half-selected cores are in 0 state.

If a half-selected core changes polarity, the error is detected when the memory register containing that core is tested by the program. For a reading error, the contents of that core will appear as a 0 in a field of 1's, and vice versa for a writing error.

Every Checkerboard Test pattern consists of alternating pairs of memory cells, one pair containing 7777's, the other containing 0000's. Since many manufacturers wire their core stacks in different ways, the same pattern of alternations cannot be used for every type of core and still allow a worst-case condition; that is, one in which all half-selected cores undergo the greatest possible disturbance which can occur when testing memory. The following pattern is used for the Ferroxcube memories with which most PDP-8's are provided.

x-axis (MA_{0-5})				
▲	0	0	1	1
	1	1	0	0
	1	1	0	0
	0	0	1	1
	y-axis (MA_{6-11}) ▶			

Since the y-axis selection lines are conditioned by the low-order six bits of the memory address register (MA_{6-11}), and the x-axis lines by the high-order bits (MA_{0-5}), the above array is interpreted as follows: (x- and y-axes should be interpreted as shown above).

Positions on the x-axis represent consecutive locations in memory from 00-77.

Positions on the y-axis represent consecutive 100_8's. Thus, the lower left corner represents location 0000. This position contains a 0, which means that the contents of the entire memory cell at address 0000 are 0's. Likewise, the contents of memory cell 0201 are 1's or 7777; this is determined by reading the third row up on the x-axis, and across one position on the y-axis.

The pattern in memory appears as follows:

Address	Contents
0000	0000
0001	0000
0002	7777
0003	7777
0004	0000
0005	0000
0006	7777
0007	0000
....	....

It can be seen from the pattern matrix, that after 77_8 registers, the pattern reverses itself, thus:

Address	Contents
0076	7777
0077	7777
0100	7777
0101	7777
0102	0000
0103	0000
0104	7777
0105	7777
0106	0000
0107	0000
....	....

And so on through memory. The pattern reverses every 100_8 registers.

5.2 Pattern Generation

The patterns generated by the other three switch register settings are defined by the following pattern matrices.

SR Setting		Pattern Matrix
0000	x-axis	1 1 0 0 1 1 0 0 0 0 1 1 0 0 1 1 y-axis
0001	x-axis	1 0 0 1 1 0 0 1 0 1 1 0 0 1 1 0 y-axis
0021	x-axis	0 1 1 0 1 0 0 1 1 0 0 1 0 1 1 0 y-axis

SR Setting		Pattern Matrix			
	x-axis	1	0	0	1
0101		0	1	1	0
		0	1	1	0
		1	0	0	1

6. METHODS

6.1 Discussion

The program writes the pattern into the area of memory to be tested. It then tests each word as follows:

The contents of the word are checked for incorrect bits.

The contents are complemented, deposited in the same register, and retested for incorrect bits.

The original contents are returned to the register, and the next one is checked.

After all memory is tested, the program writes the complement of the pattern and proceeds to check as before. In this way, every core is tested for errors that might occur when it is read and when information is written into it.

7. EXECUTION TIME

2 seconds

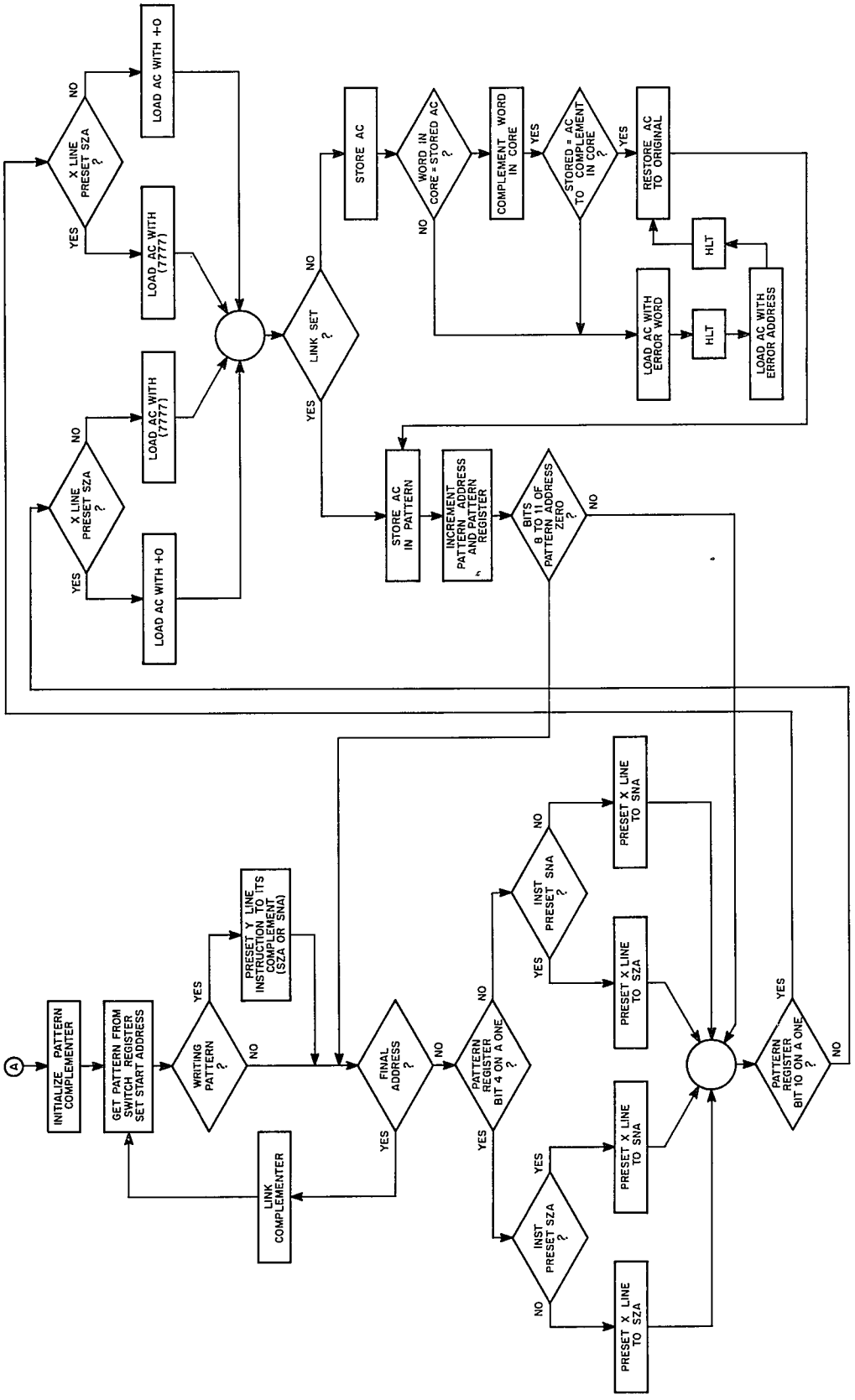
8. PROGRAM LISTING

```
                /MAINDEC 08-D1DA-D
                /EXTENDED MEMORY CHECKERBOARD-PART 2

                *Ø
0000  0000            Ø
0001  7121            CLL CML IAC
0002  3107            DCA COM

0003  7604  STX,      LAS
0004  1111            TAD MUD
0005  3105            DCA PAT
0006  1111            TAD MUD
0007  3106            DCA SA

0010  2107  STB,      ISZ COM
0011  1107            TAD COM
0012  0103            AND DOT             /2
0013  7640            SZA CLA
0014  1102            TAD NOT             /10
0015  1077            TAD HOT
0016  3025            DCA Y               /COMPLEMENT THE PATTERN
```

```
0017  1101  STC,   TAD POT          /100
0020  1106         TAD SA           /TEST FOR FINAL ADDRESS
0021  7650         SNA CLA
0022  5003         JMP STX
0023  1105         TAD PAT
0024  0100         AND ROT          /200

0025  0000  Y,     0
0026  1102         TAD NOT          /Y LINE PRESETS X LINE
0027  1077         TAD HOT          /TO SNA OR SZA
0030  3033         DCA X
0031  1105         TAD PAT
0032  0103         AND DOT          /2

0033  0000  X,     0
0034  7040         CMA
0035  7420         SNL
0036  5047         JMP CCK
0037  3506         DCA I SA         /STORE PATTERN AND RECOMPLEMENT

0040  2106  STD,    ISZ SA           /WORD WHEN CHECKING
0041  2105         ISZ PAT
0042  1106         TAD SA
0043  0104         AND BOT          /77
0044  7650         SNA CLA
0045  5017         JMP STC
0046  5031         JMP X-2

0047  3177  CCK,    DCA WRD          /CHECK PATTERN
0050  1506         TAD I SA
0051  7041         CMA IAC
0052  1177         TAD WRD
0053  7640         SZA CLA
0054  5070         JMP CC3          /ERROR IN CORE
0055  1177         TAD WRD
0056  7040         CMA
0057  3506         DCA I SA         /COMPLEMENT THE WORD
0060  1506         TAD I SA         /IN CORE
0061  7001         IAC
0062  1177         TAD WRD
0063  7640         SZA CLA          /TEST COMPLEMENT WORD
0064  5070         JMP CC3          /ERROR

0065  1177  CC2,    TAD WRD
0066  7100         CLL
0067  5037         JMP STD-1

0070  1506  CC3,    TAD I SA         /ERROR: AC CONTAINS INCORRECT WORD
0071  7402  E1,     HLT
0072  7200         CLA
0073  1106         TAD SA           /AC CONTAINS ADDRESS OF
0074  7402  E1A,    HLT              /REGISTER IN ERROR
0075  7300         CLA CLL

0076  5065  CC4,    JMP CC2
```

```
0077  7640  HOT,   7640          /CONSTANTS
0100  0200  ROT,   200
0101  0001  POT,   0001
0102  0010  NOT,   10
0103  0002  DOT,   2
0104  0000  BOT,   0000

0105  0000  PAT,   0             /VARIABLES
0106  0000  SA,    0
0107  0000  COM,   0
0110  0000  RD,    0
0111  0000  MUD,   0000
```

```
BOT     0104
CCK     0047
CC2     0065
CC3     0070
CC4     0076
COM     0107
DOT     0103
EI      0071
EIA     0074
HOT     0077
MUD     0111
NOT     0102
PAT     0105
POT     0101
RD      0110
ROT     0100
SA      0106
STB     0010
STC     0017
STD     0040
STX     0003
WRD     0177
X       0033
Y       0025
```


A
INITIALIZE PATTERN COMPLEMENTER
GET PATTERN FROM SWITCH REGISTER SET START ADDRESS
WRITING PATTERN ?
YES
NO
PRESET Y LINE INSTRUCTION TO ITS COMPLEMENT (SZA OR SNA)
FINAL ADDRESS ?
YES
NO
LINK COMPLEMENTER
PATTERN REGISTER BIT 4 ON A ONE ?
NO
YES
INST PRESET SNA ?
YES
NO
PRESET X LINE TO SZA
PRESET X LINE TO SNA
INST PRESET SZA ?
YES
NO
PRESET X LINE TO SNA
PRESET X LINE TO SZA
PATTERN REGISTER BIT 10 ON A ONE ?
YES
NO
STORE AC IN PATTERN
INCREMENT PATTERN ADDRESS AND PATTERN REGISTER
BITS 8 TO 11 OF PATTERN ADDRESS ZERO ?
NO
YES
X LINE PRESET SZA ?
NO
YES
LOAD AC WITH +0
LOAD AC WITH (7777)
X LINE PRESET SZA ?
NO
YES
LOAD AC WITH +0
LOAD AC WITH (7777)
LINK SET ?
NO
YES
STORE AC
WORD IN CORE = STORED AC ?
NO
YES
COMPLEMENT WORD IN CORE
STORED = AC COMPLEMENT IN CORE ?
YES
RESTORE AC TO ORIGINAL
LOAD AC WITH ERROR WORD
HLT
HLT
LOAD AC WITH ERROR ADDRESS

APPENDIX

MAINDEC 802 - Memory Checkerboard Test