

IDENTIFICATION

PRODUCT CODE: MAINDEC-8E-DIAB-D
PRODUCT NAME: MM8E 4K MEMORY CHECKERBOARD
DATE CREATED: JUNE 7, 1971
MAINTAINER: DIAGNOSTIC GROUP
AUTHOR: VERNON FREY

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1. ABSTRACT

This program is designed to detect core failures on half-selected lines under worst case noise conditions. Its use is intended for the PDP-8E with a basic 4K memory system.

2. REQUIREMENTS

Equipment

A PDP-8E computer with 4K of memory.

Storage

Initially the program is in core locations 2000-777 and in core locations 7000-7577.

3. LOADING PROCEDURE

Load the program with the binary loader (BIN).

4. OPERATING PROCEDURE

There are two entries to the program. These entries allow the user to start by testing upper core (1000-7777), or start by testing lower core (0000-6777). To start the program:

A. Load Address with desired entry address.

LOAD ADDRESS	0200
--------------	------

 Test upper core (1000-7777).

LOAD ADDRESS	7000
--------------	------

 Test lower core (0000-6777)

B. Set switch register to desired operation according to the following table.

SWITCH	0 (down)	1 (up)
SR00	Continue testing	Halt after test
SR07	Relocate program	Inhibit relocation

C. Press key start.

NOTE 1: RIM and BIN are saved during this test and will not be lost if the program is halted using SR00.

NOTE 2: This program will alternate testing upper and lower core unless SR07 is set. During program relocation a comparison check is made to insure no program loss.

5. ERRORS

The contents of a given memory test location should always be 0000 or 7777, therefore anything other than 0000 or 7777 will result in a test error halt. A relocation error halt will occur if the relocation comparison check fails.

Test Error Halts

A test error halt is indicated by halt address 07XX or 75XX.

If the link is set, the error occurred on complemented data.

1st halt - The AC displays the contents of the location in error.

Record the C(AC) and press key continue.

2nd halt - The AC displays the address of the location in error.

Record the C(AC) and press key continue to resume testing with the next sequential memory address.

Relocation Error Halts

A relocation error halt is indicated by halt address 03XX or 71XX.

1st halt - The AC displays the contents of the location transferring from. Record the C(AC) and press key continue.

2nd halt - The AC displays the address of the location transferring from. Record the C(AC) and press key continue.

3rd halt - The AC displays the contents of the location transferring to. Record the C(AC) and press key continue.

4th halt - The AC displays the address of the location transferring to. Record the C(AC) and C(MA). Manually correct bad core location if possible. Load Address = C(MA) and press key continue to continue relocation.

6. RESTRICTIONS

Starting Restrictions

The program may be restarted at 0200 if the program is in lower core, or at 7000 if the program is in upper core. It can easily be determined where the program is by manually looking at a few core locations.

Operating Restrictions

None

7. EXECUTION TIME

The time to write and test the worst case pattern and its complement in upper and lower core is approximately 1 second.

During program execution a 5 will be typed on the TTY every 5 minutes of program run time. This allows the operator to determine approximate run time before a failure occurred.

8. SCOPE LOOPS

Two special scope loops have been provided in this program.

Before entering a scope loop run the checkerboard program with the halt switch up. This will write worst case pattern thru core.

Scope Loop 1

This scope loop reads the address in the switches 6 times before complementing.

- A. LOAD ADDRESS 0536 if program is in lower core
7336 if program is in upper core.
- B. Set switches = address to be looped on.
- C. Press key start.

Scope Loop 2

This scope loop executed a simple read, complement, write.

- A. LOAD ADDRESS 0561 if program is in lower core
7361 if program is in upper core.
- B. Set switches = address to be looped on.
- C. Press key start.

NOTE: The address being looped on can be changed simply by changing the switch settings. The previous address will be left with its original content.

9. PROGRAM DESCRIPTION

General

A given core is selected when the combined currents of the X- and Y- selection lines produce a magneto motive force which exceeds the threshold for reversing the flux direction of the core. This occurs at the intersection of the activated selection lines. All other cores which are threaded onto the activated lines will be slightly disturbed. Under marginal current conditions, such half-selected cores might also reverse polarity when their states are properly established by the pattern which the Checkerboard Test writes into memory.

When a selected core is in the 1 state, the read current will cause it to reverse polarity and become \emptyset . When the core is in the \emptyset state, the write current will cause it to become 1. Thus, the possibility of a reading error is greatest when all half-selected cores are in the 1 state; a writing error is most probable when all the half-selected cores are in the \emptyset state.

If a half-selected core changes polarity, the error will be detected when the memory location containing that core is tested by the program. For a reading error, the contents of that core will appear as a \emptyset in a field of 1's, and vice versa for a writing error.

The Checkerboard Test pattern consists of alternating 4 memory cells containing $\emptyset\emptyset\emptyset\emptyset$ and 4 memory cells containing 7777. This pattern is reversed every 4 $\emptyset\emptyset$ octal locations. (This test pattern is generated according to the stringing of the stack and the wiring of the memory system. It is the same pattern for all 8E stacks).

Program Relocation

Program relocation is governed by the status of switch register bit 7. With this switch down (0 position) program relocation occurs each time the test pattern and it's complement have been completely tested. During the relocation a comparison check is made to insure no program loss.

Test Procedure

The worst case pattern is written, then each location is treated as follows:

- a. Read, Complement, Write the location.
- B. Read and test the location.
- C. Read, Complement, Write the location.
- D. Read and test the location.
- E. Go on to next location repeating A-D.

After the pattern is completely tested, the complement pattern is written and tested.

For further understanding of how the test is performed, refer to the listing.

/CHECKERBOARD 'WORST CASE NOISE' FO. MM8-E 4K MEMORY (VER)
/COPYRIGHT 1971, DIGITAL EQUIPMENT CORPORATION, MAYNARD, MASS.
/PROGRAMMER, VERNON FREY

/SW0=1 HALT PROGRAM SAVING BIN
/SW7=1 INHIBIT PROGRAM RELOCATION

/PROGRAM STARTING ADDRESS
/0200 TEST UPPER CORE
/7000 TEST LOWER CORE

```

0000
0000
0001
0002
0003
0200
0200
0201
0202
0203
0204
0205
0206
0207
0210
0211
0212
0213
0200
K7600,
LCNT1,
LCNT2,
LCNT3,
LINAD1,
LSW0,
LSW7,
K0200,
K7000,
K7200,
NOP
TAD
DCA
JMS
JMP
4000
0020
0200,
7000,
7200,

```

0
1
2
3

/*3
0200
LSAVBN
LGOP2
LPASS
/WILL = JMP LGOP2 FOR RESTART
/CLA USED AS CONSTANT 7600
/WILL = TRANSFER TO CONTROL COUNTER
/WILL = TRANSFER TO CONTROL
/WILL = TRANSFER FROM CONTROL
/WILL = INDIRECT ADDRESS
/THIS INST MUST BE IN LOC 206
/SR BIT 0
/SR BIT 7

/CHECK HALT PROGRAM SWITCH

```

7604
0215
0216
0217
0220
0221
0222
7604
0207
7650
5223
4232
4272
7402
LAS
AND
SNA CLA
JMP
JMS
JMS
HLT
LSR00,
AND
SNA CLA
JMP
JMS
JMS
HLT
LSR07,
AND
SZA CLA
JMP

```

LSW0
LSR07
LHILO
LRESBN
/HALT SW IS OFF
/PROG IN LO - RESTORE BIN
/PROC IN HI

/CHECK INHIBIT RELOCATION SWITCH

```

7604
0224
0225
0226
7604
5364
LAS
AND
SZA CLA
JMP

```

LSW7
SZA CLA
JMP
/INHIBIT RELOCATION

0227	0232	JMS	LHILO	
0230	1232	JMP	LRELOU	/PROG IN LO - MOVE UP
0231	5240	JMP	LRELO	/PROG IN HI - MOVE DOWN

/CHECK FOR PROGRAM IN UPPER OR LOWER MEMORY

0232	0000	LHILO, 0		
0233	1232	TAD	.-1	/0XXX OR 7XXX
0234	7004	RAL		
0235	7630	SEL CLA		/SKIP IF PROG IN LO
0236	2232	ISZ	LHILO	/PROG IN HI
0237	5632	JMP I	LHILO	

/RELOCATE PROGRAM TO UPPER MEMORY

0240	4272	JMS	LRESBN	/RESTORE BIN INTO PAGE 31
0241	1213	TAD	K7200	/-600
0242	3202	DCA	LCNT1	/CONTROLS 600 TRANSFERS
0243	1211	TAD	K0200	
0244	3204	DCA	LCNT3	/PAGE 1 CA
0245	1212	TAD	K7000	
0246	3203	DCA	LCNT2	/PAGE 28 CA
0247	4302	JMS	LRELO	/RELOCATE PROGRAM
0250	5612	JMP I	K7000	/JMP TO PROG IN UPPER MEM

/RELOCATE PROGRAM TO LOWER MEMORY

0251	4262	JMS	LSAVBN	/SAVE BIN INTO PAGE 0
0252	1213	TAD	K7200	/-600
0253	3202	DCA	LCNT1	/CONTROLS 600 TRANSFERS
0254	1211	TAD	K0200	
0255	3203	DCA	LCNT2	/PAGE 1 CA
0256	1212	TAD	K7000	
0257	3204	DCA	LCNT3	/PAGE 28 CA
0260	4302	JMS	LRELO	/RELOCATE PROGRAM
0261	5611	JMP I	K0200	/JMP TO PROG IN LOWER MEM

/SAVE BIN AND RIM INTO PAGE 0

0262	0000	LSAVBN, 0		
0263	1201	TAD	K7600	/-200
0264	3202	DCA	LCNT1	/CONTROLS 200 TRANSFERS
0265	3203	DCA	LCNT2	/PAGE 0 CA
0266	1201	TAD	K7600	
0267	3204	DCA	LCNT3	/PAGE 31 CA
0270	4302	JMS	LRELO	/RELOCATE BIN INTO PAGE 0
0271	5662	JMP I	LSAVBN	

/RESTORE BIN AND RIM INTO PAGE 31

```

0272 0000 LRESBN, 0
0273 1201 TAD K7600
0274 3202 DCA LCNT1
0275 3204 DCA LCNT3
0276 1201 TAD K7600
0277 3203 DCA LCNT2
0300 4302 JMS LRELO
0301 5672 JMP I LRESBN

```

```

/-200
/CONTROLS 200 TRANSFERS
/PAGE 0 CA
/PAGE 31 CA
/RELOCATE BIN INTO PAGE 31

```

```

/RELOCATE SUBROUTINE
/
LRELO, 0
0302 0000
0303 1604 TAD I LCNT3
0304 3603 DCA I LCNT2
0305 1604 TAD I LCNT3
0306 7041 CIA
0307 1603 TAD I LCNT2
0310 7640 SZA CLA
0311 4320 JMS LXFERF
0312 2204 ISZ LCNT3
0313 2203 ISZ LCNT2
0314 7000 NOP
0315 2202 ISZ LCNT1
0316 5303 JMP LRELO+1
0317 5702 JMP I LRELO

```

```

/TRANSFER FROM
/TRANSFER TO
/CHECK TRANSFER

/TRANSFER FAILED
/INCREMENT FROM ADDRESS
/INCREMENT TO ADDRESS

/INCREMENT TRANSFER CONTROL
/TRANSFER COMPLETE

```

```

/RELOCATION FAILURE HALT ROUTINE
/
LXFERF, 0
0320 0000
0321 1604 TAD I LCNT3
0322 7402 HLT
0323 7200 CLA
0324 1204 TAD LCNT3
0325 7402 HLT
0326 7200 CLA
0327 1603 TAD I LCNT2
0330 7402 HLT
0331 7200 CLA
0332 1203 TAD LCNT2
0333 7402 HLT
0334 7300 CLA CLL
0335 5720 JMP I LXFERF

```

```

/1ST HALT - FROM DATA
/2ND HALT - FROM ADDRESS
/3RD HALT - TO DATA
/4TH HALT - TO ADDRESS

```

```

/TYPEOUT A '5' EVERY 5 MINUTES OF RUN TIME
/
LPASS, ISZ LCNT
0336 2357 JMP LSR00
0337 5214 TAD LM750
0340 1360 DCA LCNT
0341 3357 DCA K215
0342 1361 TAD LTRANS
0343 4351 JMS /CR

```

```

/NOT 5 MINUTES YET
/RESTORE COUNTER
/CR

```

0344	1362	TAD	K212		
0345	4351	JMS	LTRANS	/LF	
0346	1363	TAD	K265		
0347	4351	JMS	LTRANS	/5	
0350	5214	JMP	LSR00		
0351	0000	LTRANS, 0		/TRANSMIT CODE	
0352	6046				
0353	6041				
0354	5353	JMP	.-1	/WAIT FOR FLAG	
0355	7300	CLA CLL			
0356	5751	JMP I	LTRANS		
0357	6400	LCNT, -1400		/COUNT 5 MINUTES	
0360	6400	LM750, -1400			
0361	0215	K215, 215		/CR	
0362	0212	K212, 212		/LF	
0363	0265	K265, 265		/5	
/GO TO PAGE 2 OR PAGE 29					
/					
0364	4365	LGOP2, JMS	.-1		
0365	0000			/0XXX OR 7XXX	
0366	7300				
0367	1365	CLA CLL			
0370	1211	TAD	.-2		
0371	0201	TAD	K0200		
0372	3205	AND	K7600		
0373	5605	DCA	LINAD1		
		JMP I	LINAD1	/0400 OR 7200	
0400	0400	LWR		/WRITE PATTERN	
0401	5216	JMP		/WRITE COMPLEMENT	
0402	5225	JMP			
0403	7774	-4			
0404	7740	-40			
0405	0523	KLENDM,		/LO END MEM ROUTINE	
0406	7330	KLAAA, HAAA		/HI END MEM ROUTINE	
0407	0000	LEND1, 0		/END MEM ROUTINE	
0408	0000	LMADD, 0		/START WRITE ADDRESS	
0409	0000	LCNT4, 0		/WRITE 2 PAGES	
0410	0000	LCNT5, 0		/WRITE 4 ADDRESSES	
0411	0000	KK0200, 0200			
0412	0200	K1000, 1000			
0413	1000	KK7600, 7600			
0414	7600	LINAD2, 0		/INDIRECT ADDRESSING	
0415	0000				
/WRITE PATTERN INTO MEMORY					
/					
0416	4235	LWR,			
0417	4253	JMS	LWCON	/CORRECT WRITE CONSTANTS	
0420	1253	JMS	LWRMEM	/WRITE PATTERN	
0421	1212	TAD	LWRMEM	/0XXX OR 7XXX	
0422	0214	TAD	KK0200		
		AND	KK7600		

```

0423 3215 DCA LINAD2
0424 5615 JMP I LINAD2 /0600 OR 7400

/WRITE COMPLEMENT PATTERN INTO MEMORY
LWRC, JMS LWCON /CORRECT WRITE CONSTANTS
JMS LWRMC /WRITE COMPLEMENT PATTERN
TAD LWRMEM /0XXX OR 7XXX
AND KK0200
AND KK7600
IAC
DCA LINAD2 /0601 OR 7401
JMP I LINAD2

```

```

/UPDATE WRITE CONSTANTS
LWCON, 0
TAD -1 /0XXX OR 7XXX
RAL
SZL CLA
JMP LWCON1 /PROG IN UPPER MEM
TAD K1000 /PROG IN LOWER MEM
DCA LMADD /START WRITE ADDRESS
TAD KLENDM
DCA LEND1 /END MEM ROUTINE
JMP I LWCON

LWCON1, TAD KLAAR /END MEM ROUTINE
DCA LEND1 /START WRITE ADDRESS
DCA LMADD
JMP I LWCON

```

```

/WRITE PATTERN OR WRITE PATTERN COMPLEMENT
LWRMEM, 0 LW1010 /WRITE PATTERN
LWRMC, 0
TAD -1 /STORE RETURN ADDRESS
DCA LWRMEM /WRITE COMPLEMENT
JMP LW0101

LW1010, TAD LM40 /-40
DCA LCNT4 /WRITE 2 PAGES
JMS LWONE /WRITE 4 WORDS OF ONES
JMS LWZERO /WRITE 4 WORDS OF ZEROS
ISE LCNT4
JMP LW1010+2
JMS I LEND1 /END OF MEMORY?
TAD LM40 /-40
DCA LCNT4 /WRITE 2 PAGES
JMS LWZERO /WRITE 4 WORDS OF ZEROS
JMS LWONE

```

```

0453 0000
0454 5261
0455 0000
0456 1255
0457 3253
0460 5270

0461 1203
0462 3210
0463 4311
0464 4300
0465 2210
0466 5263
0467 4606
0470 1203
0471 3210
0472 4300
0473 4311

```

0474 2210 ISZ LCNT4
 0475 5272 JMP LW0101+2
 0476 4606 JMS I LEND1
 0477 5261 JMP LW1010
 /END OF MEMORY?

LWZERO, 0
 0500 0000 LM4 /-4
 0501 1202 TAD /WRITE 4 ZEROS
 0502 3211 DCA LCNT5
 0503 3607 DCA I LMADD
 0504 2207 ISZ LMADD /INCREMENT MEMORY ADDRESS
 0505 7000 NOP
 0506 2211 ISZ LCNT5
 0507 5303 JMP LWZERO+3
 0510 5700 JMP I LWZERO

LWONE, 0
 0511 0000 LM4 /-4
 0512 1202 TAD /WRITE 4 ONES
 0513 3211 DCA LCNT5
 0514 7240 STA
 0515 3607 DCA I LMADD
 0516 2207 ISZ LMADD /INCREMENT MEMORY ADDRESS
 0517 7000 NOP
 0520 2211 ISZ LCNT5
 0521 5314 JMP LWONE+3
 0522 5711 JMP I LWONE

/CHECK FOR END OF MEMORY

LENDM, 0
 0523 0000 TAD LMADD
 0524 1207 SZA CLA
 0525 7640 JMP I LENDM
 0526 5723 JMP I LWRMEM
 0527 5653
 0530 0000 LAAA, 0
 0531 1207 TAD LMADD
 0532 1213 TAD K1000
 0533 7640 SZA CLA
 0534 5730 JMP I LAAA
 0535 5653 JMP I LWRMEM

/TWO SPECIAL SCOPE LOOPS

LSCOPI, LAS /TEST ADDRESS
 0536 7604 DCA LSWADD
 0537 3372 TAD I LSWADD
 0540 1772 AND I LSWADD
 0541 0772 AND I LSWADD
 0542 0772 AND I LSWADD
 0543 0772 AND I LSWADD
 0544 0772 AND I LSWADD
 0545 0772 AND I LSWADD
 0546 7040 CMA
 0547 3772 DCA I LSWADD
 0550 1772 TAD I LSWADD

0551 0772 AND I LSWADD
 0552 0772 AND I LSWADD
 0553 0772 AND I LSWADD
 0554 0772 AND I LSWADD
 0555 0772 AND I LSWADD
 0556 7040 CMA
 0557 3772 DCA I LSWADD
 0560 5336 JMP LSCOP1

LSCOP2, LAS /TEST ADDRESS
 DCA LSWADD
 TAD I LSWADD
 CMA LSWADD
 DCA I LSWADD
 TAD I LSWADD
 CMA LSWADD
 DCA I LSWADD
 JMP LSCOP2

/READ AND TEST PATTERN
 /READ AND TEST COMPLEMENT

0572 0000 LSWADD, 0
 0600 #600 JMP LTST
 0601 9224 JMP LTSTC
 0602 7774 -4
 0603 7700 LM04, -100
 0604 0763 KLENDT, LENDT
 0605 7570 KLBBB, HBBB
 0606 0000 LEND2, 0
 0607 0000 LTSTAD, 0
 0610 0000 LCNT6, 0
 0611 0000 LCNT7, 0
 0612 1000 KK1000, 1000
 0613 7600 KC7600, 7600

/LO END TEST ROUTINE
 /HI END TEST ROUTINE
 /END TEST ROUTINE
 /START TEST ADDRESS
 /TEST 2 PAGES
 /TEST 4 ADDRESSES

/READ AND TEST PATTERN CONTROL

0614 4234 JMS LRCON
 0615 4252 JMS LRMEM
 0616 1252 TAD LRMEM
 0617 1213 TAD KC7600
 0620 0213 AND KC7600
 0621 7001 IAC
 0622 3207 DCA LTSTAD
 0623 5607 JMP I LTSTAD

/CORRECT READ CONSTANTS
 /READ AND TEST PATTERN
 /0XXX OR 7XXX
 /-200

/READ AND TEST COMPLEMENT PATTERN CONTROL

0624 4234 JMS LRCON
 0625 4254 JMS LRMEMC
 0626 1254 TAD LRMEMC
 0627 7006 7006
 0630 7630 SEL CLA

/CORRECT READ CONSTANTS
 /READ AND TEST COMPLEMENT PATTERN
 /0XXX OR 7XXX
 /RTL - AND ADDRESS OF TAG HPASS

0631 5627 JMP I .-2 /PROG IN UPPER MEM
 0632 5633 JMP I .+1 /PROG IN LOWER MEM
 0633 0206 /ADDRESS OF TAG LPASS

/UPDATE READ CONSTANTS

LRCON, 0 /XXXX OR 7XXX
 TAD .-1
 RAL
 SZL CLA
 JMP LRCON1 /PROG IN UPPER MEM
 TAD KK1000 /PROG IN LOWER MEM
 DCA LTSTAD /START TEST ADDRESS
 TAD KLENDT
 DCA LEND2 /END MEM ROUTINE
 JMP I LRCON
 LRCON1, TAD KLBBB /END MEM ROUTINE
 DCA LEND2 /START TEST ADDRESS
 DCA LTSTAD
 JMP I LRCON

/READ AND TEST PATTERN OR PATTERN COMPLEMENT

LRMEM, 0 /READ AND TEST PATTERN
 LRMEMC, 0 /STORE RETURN ADDRESS
 TAD .-1 /READ AND TEST COMPLEMENT
 DCA LRMEM
 JMP LR0101
 LR1010, TAD LM100 /-100
 DCA LCNT6 /READ AND TEST 2 PAGES
 TAD LMB4 /-4
 DCA LCNT7 /READ AND TEST 4 ADDRESSES
 TAD I LTSTAD
 CMA STL
 DCA I LTSTAD
 TAD I LTSTAD
 SEA CLA
 JMS LHALTC /TEST ONE COMPLEMENTED
 TAD I LTSTAD /THIS LOC FAILED READ AND TEST
 CMA
 DCA I LTSTAD
 TAD I LTSTAD
 IAC CLL
 SEA CLA
 JMS LHALT /TEST ONE
 ISZ LTSTAD /THIS LOC FAILED READ AND TEST
 NOP
 ISZ LCNT7
 JMP LONE+2
 ISZ LCNT6

```

0706 5313 JMP LZERO
0707 4606 JMS I LEND2
0710 5260 JMP LR1010

LR0101, TAD LM100 /-100
DCA LCNT6 /READ AND TEST 2 PAGES
LZERO, TAD LM04 /-4
DCA LCNT7 /READ AND TEST 4 ADDRESSES
LZER01, TAD I LTSTAD
CMA DCA I LTSTAD
DCA I LTSTAD
TAD I LTSTAD
IAC STL
SZA CLA
JMS LHALTC
TAD I LTSTAD
CMA CLL
DCA I LTSTAD
TAD I LTSTAD
SZA CLA
JMS LHALT
ISE LTSTAD
NOP
ISE LCNT7
JMP LZERO+2
ISE LCNT6
JMS LONE
JMS I LEND2
JMP LR0101

```

```

/TEST ZERO COMPLEMENTED
/THIS LOC FAILED READ AND TEST

/TEST ZERO
/THIS LOC FAILED READ AND TEST

/END OF MEMORY?
/NO

/ERROR HALT ROUTINE FOR DATA FAILURE
LHALT, 0 TAD I LTSTAD
HLT HLT /1ST HALT = BAD DATA
CLA CLA
TAD TAD /2ND HALT = BAD LOCATION
HLT HLT
CLA CLA
JMP I LHALT

```

```

/ERROR HALT ROUTINE FOR COMPLEMENT DATA FAILURE
LHALTC, 0 TAD I LTSTAD
CMA CMA
HLT HLT /1ST HALT = BAD DATA
CLA CLA
TAD TAD /2ND HALT = BAD LOCATION
HLT HLT
CLA CLL
JMP I LHALTC

```

```

/END OF MEMORY ROUTINE
/LENDT, 0 TAD LTSTAD
SZA CLA
JMP I LENDT
JMP I LRMEM
LBBB, 0
TAD LTSTAD
TAD KK1000
SZA CLA
JMP I LBBB
JMP I LRMEM

```

/MORE MEMORY TO TEST
/END OF TEST

/MORE MEMORY TO TEST
/END OF TEST

```

*7000
NOP
7000, 7600
7001, 7600
7002, 1205
7003, 3200
7004, 7000
7005, 5364
7006, 5336
7007, 4000
7010, 0020
7011, 0200
7012, 7000
7013, 7200

```

/WILL = JMP HGOP2 FOR RESTART
/CLA USED AS CONSTANT 7600
/WILL = TRANSFER CONTROL COUNTER
/WILL = TRANSFER TO CONTROL
/WILL = TRANSFER FROM CONTROL
/WILL = INDIRECT ADDRESS
/THIS INST MUST BE IN LOC 7006
/SR BIT 0
/SR BIT 7

```

/CHK HALT PROGRAM SWITCH
/HSR00, LAS
AND HSW0
SNA CLA
JMP HSR07
JMS HHILO
JMS HRESBN
HLT

```

/HALT SW IS OFF
/PROG IN LO - RESTORE BIN
/PROG IN HI

```

/CHK INHIBIT RELOCATION SWITCH
/HSR07, LAS
AND HSW7
SZA CLA
JMP HGOP2
JMS HHILO
JMS HRELOU
JMP HRELOD

```

/INHIBIT RELOCATION
/PROG IN LO - MOVE UP
/PROG IN HI - MOVE DOWN

```

/CHK FOR PROGRAM IN UPPER OR LOWER MEMORY
/HHILO, 0 TAD

```

/0XXX OR 7XXX

```

7034 7004 RAL
7035 7630 SEL CLA
7036 2232 ISZ
7037 5632 JMP I HHILO

/RELOCATE PROGRAM TO UPPER MEMORY
HRELOU, JMS HRESBN /RESTORE BIN INTO PAGE 31
TAD C7200 /-600
DCA HCNT1 /CONTROLS 600 TRANSFERS
TAD C0200 /PAGE 1 CA
DCA HCNT3 /PAGE 28 CA
TAD C7000 /RELOCATE PROGRAM
DCA HCNT2 /JMP TO PROG IN UPPER MEM
JMS HRELO
JMP I C7000
    
```

```

/RELOCATE PROGRAM TO LOWER MEMORY
HRELOD, JMS HSAVBN /SAVE BIN INTO PAGE 0
TAD C7200 /-600
DCA HCNT1 /CONTROLS 600 TRANSFERS
TAD C0200 /PAGE 1 CA
DCA HCNT2 /PAGE 28 CA
TAD C7000 /RELOCATE PROGRAM
DCA HCNT3 /JMP TO PROG IN LOWER MEM
JMS HRELO
JMP I C0200
    
```

```

/SAVE BIN AND RIM INTO PAGE 0
HSAVBN, 0 TAD C7600 /-200
DCA HCNT1 /CONTROLS 200 TRANSFERS
DCA HCNT2 /PAGE 0 CA
TAD C7600 /PAGE 31 CA
DCA HCNT3 /RELOCATE BIN INTO PAGE 0
JMS HRELO
JMP I HSAVBN
    
```

```

/RESTORE BIN AND RIM INTO PAGE 31
HRESBN, 0 TAD C7600 /-200
DCA HCNT1 /CONTROLS 200 TRANSFERS
DCA HCNT3 /PAGE 0 CA
TAD C7600 /PAGE 31 CA
DCA HCNT2 /RELOCATE BIN INTO PAGE 31
JMS HRELO
JMP I HRESBN
    
```

```

/RELOCATE SUBROUTINE
HRELO, 0
TAD I HCNT3 /TRANSFER FROM
DCA I HCNT2 /TRANSFER TO
TAD I HCNT3 /CHECK TRANSFER
CIA
TAD I HCNT2
SZA CLA
JMS HXFERF
ISE HCNT3 /TRANSFER FAILED
ISE HCNT2 /INCREMENT FROM ADDRESS
NOP /INCREMENT TO ADDRESS
ISE HCNT1 /INCREMENT TRANSFER CONTROL
JMP HRELO+1
JMP I HRELO /TRANSFER COMPLETE

```

```

/RELOCATION FAILURE HALT ROUTINE
HXFERF, 0
TAD I HCNT3 /1ST HALT - FROM DATA
CLA HLT
TAD HLT /2ND HALT - FROM ADDRESS
CLA HLT
TAD I HCNT2 /3RD HALT - TO DATA
HLT
TAD HLT /4TH HALT - TO ADDRESS
CLA CLL
JMP I HXFERF

```

```

/TYPEOUT A 'S' EVERY 5 MINUTES OF RUN TIME
HPASS, 0
ISE HCNT
JMP HSR00 /NOT 5 MINUTES YET
TAD HM750
DCA HCNT /RESTORE COUNTER
TAD C215 /CR
JMS HTRANS
TAD C212 /LF
JMS HTRANS
TAD C265 /5
JMS HTRANS
JMP HSR00
HTRANS, 0
TL5 /TRANSMIT CODE

```

7102 0000
7103 1604
7104 3603
7105 1604
7106 7041
7107 1603
7110 7640
7111 4320
7112 2204
7113 2203
7114 7000
7115 2202
7116 5303
7117 5702

7120 0000
7121 1604
7122 7402
7123 7200
7124 1204
7125 7402
7126 7200
7127 1603
7130 7402
7131 7200
7132 1203
7133 7402
7134 7300
7135 5720

7136 2357
7137 5214
7140 1360
7141 3357
7142 1361
7143 4351
7144 1362
7145 4351
7146 1363
7147 4351
7150 5214
7151 0000
7152 6046

7153	6041	TSF	
7154	5353	JMP	.-1
7155	7300	CLA CLL	
7156	5751	JMP I	HTRANS
7157	6400	HCNT,	-1400
7160	6400	HM750,	-1400
7161	0215	C215,	215
7162	0212	C212,	212
7163	0265	C265,	265

/GO TO PAGE 2 OR PAGE 29			
7164	4365	JMS	.+1
7165	0000	0	
7166	7300	CLA CLL	
7167	1365	TAD	.-2
7170	1211	TAD	C0200
7171	0201	AND	C7600
7172	3205	DCA	HINAD1
7173	9605	JMP I	HINAD1

7200	7200	JMP	HWR
7201	9216	JMP	HWR
7202	7774	-4	
7203	7740	-40	
7204	0523	CHENDM,	LENDM
7205	7330	CHAAA,	HAAA
7206	0000	WEND1,	0
7207	0000	HMADD,	0
7210	0000	HCNT4,	0
7211	0000	HCNT5,	0
7212	0200	CC0200,	0200
7213	1000	C1000,	1000
7214	7600	CC7600,	7600
7215	0000	HINAD2,	0

/WRITE PATTERN INTO MEMORY			
7216	4235	JMS	HWCON
7217	4253	JMS	HWRMEM
7220	1253	TAD	HWRMEM
7221	1212	TAD	CC0200
7222	0214	AND	CC7600
7223	9215	DCA	HINAD2
7224	9615	JMP I	HINAD2

/WRITE COMPLEMENT PATTERN INTO MEMORY			
7225	4235	JMS	HWCON
7226	4255	JMS	HWRMC

/WAIT FOR FLAG
/COUNT 5 MINUTES
/CR
/LF
/5

/0XXX OR 7XXX
/0400 OR 7200

/WRITE PATTERN
/WRITE COMPLEMENT
/LO END MEM ROUTINE
/HI END MEM ROUTINE
/END MEM ROUTINE
/START WRITE ADDRESS
/WRITE 2 PAGES
/WRITE 4 ADDRESSES

/INDIRECT ADDRESSING

/CORRECT WRITE CONSTANTS
/WRITE PATTERN
/0XXX OR 7XXX

/0600 OR 7400

/CORRECT WRITE CONSTANTS
/WRITE COMPLEMENT PATTERN

7227 1253 HWRMEM
 7230 1212 TAD CC0200 /0XXX OR 7XXX
 7231 0214 AND CC7600
 7232 7001 IAC
 7233 3215 DCA HINAD2
 7234 5615 JMP I HINAD2 /0601 OR 7401

/UPDATE WRITE CONSTANTS

7235 0000 HWCON, 0
 7236 1235 TAD , -1 /0XXX OR 7XXX
 7237 7004 RAL
 7240 7630 SZL CLA
 7241 9247 JMP HWCON1 /PROG IN UPPER MEM
 7242 1213 TAD C1000 /PROG IN LOWER MEM
 7243 3207 DCA HMADD /START WRITE ADDRESS
 7244 1204 TAD CHENDM
 7245 3206 DCA HEND1 /END MEM ROUTINE
 7246 5635 JMP I HWCON
 HWCON1, TAD CHAAA
 DCA HEND1 /END MEM ROUTINE
 DCA HMADD /START WRITE ADDRESS
 JMP I HWCON

/WRITE PATTERN OR WRITE PATTERN COMPLEMENT

7253 0000 HWRMEM, 0 HW1010 /WRITE PATTERN
 7254 5261 JMP HW1010
 7255 0000 HWRMC, 0
 7256 1255 TAD , -1 /STORE RETURN ADDRESS
 7257 3253 DCA HWRMEM /WRITE COMPLEMENT
 7260 9270 JMP HW0101
 HW1010, TAD HM40 /-40
 DCA HCNT4 /WRITE 2 PAGES
 JMS HWONE /WRITE 4 WORDS OF ONES
 JMS HWZERO /WRITE 4 WORDS OF ZEROS
 ISE HCNT4
 JMP HW1010+2
 JMS I HEND1 /END OF MEMORY?
 TAD HM40 /-40
 DCA HCNT4 /WRITE 2 PAGES
 JMS HWZERO /WRITE 4 WORDS OF ZEROS
 JMS HWONE /WRITE 4 WORDS OF ONES
 ISE HCNT4
 JMP HW0101+2
 JMS I HEND1 /END OF MEMORY?
 JMP HW1010
 HWZERO, 0 HM4 /-4
 TAD HCNT5 /WRITE 4 ZEROS
 DCA

7303	3607	DCA I	HMADD	/INCREMENT MEMORY ADDRESS
7304	2207	ISZ	HMADD	
7305	7000	NOP		
7306	2411	ISZ	HCNT5	
7307	5303	JMP	HWZERO+3	
7310	5700	JMP I	HWZERO	
7311	0000	HWONE,		
7312	1202	TAD	HM4	/-4
7313	3211	DCA	HCNT5	/WRITE 4 ONES
7314	7240	STA		
7315	3607	DCA I	HMADD	/INCREMENT MEMORY ADDRESS
7316	2207	ISZ	HMADD	
7317	7000	NOP		
7320	2411	ISZ	HCNT5	
7321	5314	JMP	HWONE+3	
7322	5711	JMP I	HWONE	

7323	0000	/CHECK FOR END OF MEMORY		
7324	1207	HENDM,		
7325	7640	TAD	HMADD	
7326	0723	SEA CLA		
7327	5653	JMP I	HENDM	
7330	0000	JMP I	HWRMEM	
7331	1207	HAAA,		
7332	1213	TAD	HMADD	
7333	7640	TAD	C1000	
7334	5730	SEA CLA		
7335	5653	JMP I	HAAA	
		JMP I	HWRMEM	

7336	7604	/TWO SPECIAL SCOPE LOOPS		
7337	9372	HSCOP1,		/TEST ADDRESS
7340	1772	DCA	HSWADD	
7341	0772	TAD I	HSWADD	
7342	0772	AND I	HSWADD	
7343	0772	AND I	HSWADD	
7344	0772	AND I	HSWADD	
7345	0772	AND I	HSWADD	
7346	7040	CMA		
7347	9772	DCA I	HSWADD	
7350	1772	TAD I	HSWADD	
7351	0772	AND I	HSWADD	
7352	0772	AND I	HSWADD	
7353	0772	AND I	HSWADD	
7354	0772	AND I	HSWADD	
7355	0772	AND I	HSWADD	
7356	7040	CMA		
7357	9772	DCA I	HSWADD	

```

7360 5336 JMP HSCOP1
7361 7604 HSCOP2, LAS
7362 3372 DCA HSWADD
7363 1772 TAD I HSWADD
7364 7040 CMA
7365 3772 DCA I HSWADD
7366 1772 TAD I HSWADD
7367 7040 CMA
7370 3772 DCA I HSWADD
7371 9361 JMP HSCOP2
7372 0000 HSWADD, 0

7400 JMP HTST
7401 5214 JMP HTSTC
7402 7774 -4
7403 7700 -100
7404 0763 CHENDT, LENDT
7405 7570 CHBBB, HBBB
7406 0000 HEND2, 0
7407 0000 HTSTAD, 0
7410 0000 MCNT6, 0
7411 0000 MCNT7, 0
7412 1000 CC1000, 1000
7413 7600 CK7600, 7600
    
```

```

/READ AND TEST PATTERN
/READ AND TEST COMPLEMENT

/LO END TEST ROUTINE
/HI END TEST ROUTINE
/END TEST ROUTINE
/START TEST ADDRESS
/TEST 2 PAGES
/TEST 4 ADDRESSES

/READ AND TEST PATTERN CONTROL
/READ AND TEST PATTERN
/0XXX OR 7XXX
/-200

/0401 OR 7201
    
```

```

7414 4234 HRCN
7415 4252 HRMEM
7416 1252 HRMEM
7417 1213 CK7600
7420 0213 AND CK7600
7421 7001 IAC
7422 3207 DCA
7423 9607 JMP I

/READ AND TEST COMPLEMENT PATTERN CONTROL
/READ AND TEST COMPLEMENT PATTERN
/0XXX OR 7XXX
/RTL - AND ADDRESS OF TAG HPASS

/UPDATE READ CONSTANTS
    
```

```

7424 4234 HRCN
7425 4254 HRMEHC
7426 1254 HRMEHC
7427 7006 TAD 7006
7430 7630 SEL CLA
7431 9627 JMP I .-2
7432 9653 JMP I .+1
7433 0206 0206
    
```

```

7434 0000 HRCON, 0
7435 1234 TAD
7436 7004 RAL
7437 7630 SZL CLA
7440 5246 JMP
7441 1212 TAD
7442 3207 DCA
7443 1204 TAD
7444 3206 DCA
7445 5634 JMP I

7446 1205 HRCON1, TAD
7447 3206 DCA
7450 3207 DCA
7451 5634 JMP I

7452 0000 HRMEM, 0
7453 5200 HR1010
7454 0000 HRMEMC, 0
7455 1254 TAD
7456 3252 DCA
7457 5311 JMP

7460 1205 HR1010, TAD
7461 3210 DCA
7462 1202 TAD
7463 3211 DCA
7464 1607 TAD I
7465 7160 CHA STL
7466 3607 DCA I
7467 1607 TAD I
7470 7640 SZL CLA
7471 4352 JMS I
7472 1607 TAD I
7473 7040 CHA I
7474 3607 DCA I
7475 1607 TAD I
7476 7101 IAC CLL
7477 7640 SZL CLA
7500 4342 JMS
7501 2207 ISE
7502 7000 NOP
7503 2211 ISE
7504 5264 JMP
7505 2210 ISE
7506 5313 JMP
7507 4606 JMS I
7510 5260 JMP

7511 1203 HR0101, TAD
7512 3210 DCA
7513 1202 HZERO, TAD

/READ AND TEST PATTERN OR PATTERN COMPLEMENT
/HRMEM, 0 HR1010 /READ AND TEST PATTERN
/HRMEMC, 0 HR1010 /READ AND TEST PATTERN
/HRMEM HRMEM /STORE RETURN ADDRESS
/HR0101 HR0101 /READ AND TEST COMPLEMENT
/HR1010, TAD /-100
/DCI MCNT6 /READ AND TEST 2 PAGES
/HONE, TAD /-4
/HONE1, TAD I MCNT7 /READ AND TEST 4 ADDRESSES
/CHASTL CHA STL
/DCI I HTSTAD
/TAD I HTSTAD
/SZL CLA
/JMS I MHALTC /TEST ONE COMPLEMENTED
/TAD I HTSTAD /THIS LOC FAILED READ AND TEST
/DCI I HTSTAD
/TAD I HTSTAD
/IAC CLL /TEST ONE
/SZL CLA /THIS LOCATION FAILED READ AND TEST
/JMS
/ISE
/NOP
/ISE
/JMP
/ISE
/JMP
/JMS I
/JMP
/END OF MEMORY?
/NO

/HR0101, TAD /-100
/DCI MCNT6 /READ AND TEST 2 PAGES
/HZERO, TAD /-4

```

```

7514 3211 DCA HCNT7
7515 1607 HZERR01, TAD I HTSTAD
7516 7040 CMA
7517 3607 DCA I HTSTAD
7520 1607 TAD I HTSTAD
7521 7121 IAC STL
7522 7640 SZA CLA
7523 4352 JMS HHALTC
7524 1607 TAD I HTSTAD
7525 7140 CMA CLL
7526 3607 DCA I HTSTAD
7527 1607 TAD I HTSTAD
7530 7640 SZA CLA
7531 4342 JMS HHALT
7532 2207 ISE HTSTAD
7533 7000 NOP
7534 2211 ISE
7535 5315 JMP HZERO+2
7536 2210 ISE HCNT6
7537 5262 JMP HONE
7540 4606 JMS I HEND2
7541 5311 JMP HR0101

```

```

/READ AND TEST 4 ADDRESSES
/TEST ZERO COMPLEMENTED
/THIS LOC FAILED READ AND TEST
/TEST ZERO
/THIS LOC FAILED READ AND TEST

```

```

7542 0000 HHALT, 0
7543 1607 TAD I HTSTAD
7544 7402 HLT
7545 7200 CLA
7546 1207 TAD HTSTAD
7547 7402 HLT
7550 7200 CLA
7551 5742 JMP I HHALT

```

```

/ERROR HALT ROUTINE FOR DATA FAILURE
/1ST HALT = BAD DATA
/2ND HALT = BAD LOCATION

```

```

7552 0000 HHALTC, 0
7553 1607 TAD I HTSTAD
7554 7040 CMA
7555 7402 HLT
7556 7200 CLA
7557 1207 TAD HTSTAD
7560 7402 HLT
7561 7300 CLA CLL
7562 5752 JMP I HHALTC

```

```

/ERROR HALT ROUTINE FOR COMPLEMENT DATA FAILURE
/1ST HALT = BAD DATA
/2ND HALT = BAD LOCATION

```

```

7563 0000 HENDT, 0
7564 1207 TAD HTSTAD
7565 7640 SZA CLA
7566 5763 JMP I HENDT

```

```

/END OF MEMORY ROUTINE
/MORE MEMORY TO TEST

```

7567	5652	JMP I	HRMEM	/END OF TEST
7570	0000	0		
7571	1207	TAD	HTSTAD	
7572	1212	TAD	CC1000	
7573	7640	SZA	CLA	
7574	5770	JMP I	HBBB	/MORE MEMORY TO TEST
7575	5652	JMP I	HRMEM	/END OF TEST

\$

0000	11110000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
0100	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
0200	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
0300	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11110000
0400	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
0500	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11100000
0600	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
0700	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111100

1000
1100
1200
1300
1400
1500
1600
1700
2000
2100
2200
2300
2400
2500
2600
2700
3000
3100
3200
3300
3400
3500
3600
3700

C0200	7011	HRESBN	7072	LCNT6	0610
C1000	7213	HRMEM	7452	LCNT7	0611
C212	7162	HRMEMC	7454	LEND1	0406
C215	7161	HSABVN	7062	LEND2	0606
C265	7163	HSCOP1	7336	LENDM	0523
C7000	7012	HSCOP2	7361	LENDT	0763
C7200	7013	HSR00	7014	LGOP2	0364
C7600	7001	HSR07	7023	LHALT	0742
CC0200	7212	HSW0	7007	LHALTC	0752
CC1000	7412	HSW7	7010	LHILO	0232
CC7600	7214	HSWADD	7372	LINAD1	0205
CHAAA	7205	HTRANS	7151	LINAD2	0415
CH888	7405	HTST	7414	LM04	0602
CHENDM	7204	HTSTAD	7407	LM100	0603
CHENDT	7404	HTSTC	7424	LM4	0402
CK7600	7413	HW0101	7270	LM40	0403
HAAA	7330	HW1010	7261	LM750	0360
H888	7570	HWCON	7235	LMADD	0407
HCNT	7157	HWCON1	7247	LONE	0662
HCNT1	7002	HWONE	7311	LONE1	0664
HCNT2	7003	HWR	7216	LPASS	0336
HCNT3	7004	HWRMC	7225	LR0101	0711
HCNT4	7210	HWRMC	7255	LR1010	0660
HCNT5	7211	HWRMEM	7253	LRCON	0634
HCNT6	7410	HWZERO	7300	LRCON1	0646
HCNT7	7411	HXFERF	7120	LRELO	0302
HEND1	7206	HZERO	7513	LRELOD	0251
HEND2	7406	HZERO1	7515	LRELOU	0240
HENDM	7323	K0200	0211	LRESBN	0272
HENDY	7563	K1000	0413	LRMEM	0652
HGOP2	7164	K212	0362	LRMEMC	0654
HHALT	7342	K215	0361	LSAVBN	0262
HHALTC	7552	K265	0363	LSCOP1	0536
HHILO	7032	K7000	0212	LSCOP2	0561
HINAD1	7005	K7200	0213	LSR00	0214
HINAD2	7215	K7600	0201	LSR07	0223
HM04	7402	KC7600	0613	LSW0	0207
HM100	7403	KK0200	0412	LSW7	0210
HM4	7202	KK1000	0612	LSWADD	0572
HM40	7203	KK7600	0414	LTRANS	0351
HM750	7160	KLAAA	0405	LTST	0614
HMA00	7207	KLBBB	0605	LTSTAD	0607
HONE	7462	KLENDM	0404	LTSTC	0624
HONE1	7464	KLENDT	0604	LW0101	0470
HPASS	7136	LAAA	0530	LW1010	0461
HR0101	7511	LB88	0770	LWCON	0435
HR1010	7460	LCNT	0357	LWCON1	0447
HRCON	7434	LCNT1	0202	LWONE	0511
HRCON1	7446	LCNT2	0203	LWR	0416
HRELO	7102	LCNT3	0204	LWRC	0425
HRELO0	7051	LCNT4	0410	LWRMC	0455
HRELOU	7040	LCNT5	0411	LWRMEM	0453

ERRORS DETECTED: 0
LINKS GENERATED: 0
RUN-TIME: 9 SECONDS
3K CORE USED

