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PDP11/20
RS64 disk file
maintenance manual

DEC-00-HRS64-E-D

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## CHAPTER 1

## GENERAL INFORMATION

## . 1 INTRODUCTION

This manual contains instructions for interfacing, installing, operating, and maintaining the RS64 Disk File manufactured by Digital Equipment Corporation (DEC), Maynard, Massachusetts. The instructions are intended for maintenance personnel with a basic understanding of disk files but who may not necessarily be familiar with the RS64 Disk File.

The instructions are arranged in six primary divisions: General Description, Installation and Operation, Theory of Operation, Interfacing, Maintenance, and Drawings. Two appendices are also provided; (a) track writer format and relationships, and (b) the power supply.

In addition to this manual, the following documents contain information relevant to the RS64 Disk File
a. DEC Logic Handbook, 1970, C105
b. Special Maintenance Procedures for Disks, DEC-SP-DISK-DA

### 1.2 PURPOSE AND APPLICATION INFORMATION

The RS64 Disk File, Figure 1-1, is a fast, random-access file that provides up to $1,280,000$ bits of storage. With the disk select logic provided in each disk file, up to four RS64 Disk Files can be operated from one controller, hus providing a storage capability of up to $5,120,000$ bits.
The RS64 is designed for standard 19 -in. rack mounting. It is furnished with disk assembly and modularized read/write electronics contained in a slide-mounted chassis that requires $10-1 / 2 \mathrm{in}$. of front panel height. The power supply is mounted on the rear of the cabinet, separate from the drive chassis. Two basic models are available; the RS64A operates with 115 V , 47 to 63 Hz primary power and the RS64B operates with 230 V , 47 to 63 Hz primary power.

The disk assembly contains a 10 -in. nickel-cobalt plated disk that is driven by an induction motor at approximately $1400(50 \mathrm{~Hz})$ or $1800(60 \mathrm{~Hz}) \mathrm{rpm}$. Data is recorded on a single disk surface using 32 fixed read/write heads. Other features include a highly reliable, self-synchronizing clock recovery system and write protection (write lockout) for the data tracks. Three spare timing tracks are also provided
Pertinent interfacing and design criteria, plus recommended controller interface circuits, are provided in this man ual. In addition, the RS 64 Power Supply is capable of providing a controller with up to 4.5 A at +5 V .

13 PHYSICAL DESCRIPTION
1.3.1 General

The RS64 Disk File consists of two major assemblies: disk assembly RS64M, and power control and logic assembly RS64P. These assemblies and the elements comprising them are described in subsequent paragraphs.


Figure 1-1 RS64 Disk File

### 13.2 RS64M Disk Assembly

The disk assembly, Figure 1-2, consists of a 10 -in. diameter nickel-cobalt plated aluminum disk, a drive motor, and five head assemblies mounted on a deck plate. The deck plate is supported by four shock mounts. A cove protects the disk and heads from dust and foreign particles. Data connections are made via connectors on the underside of the deck plate. A 4 -wire power cord connects the drive motor to the RS64P power control and logic assembly.
1.3.3 RS64P Power Control and Logic Assembly

The power control and logic assembly, Figure 1-3, consists of a wired assembly for housing logic modules, a powe control panel, a disk select and write lockout panel, and a power supply. It also includes two data cable assemblies pand, a disk select and write tockout panel, and a power suppl. It aso bly and the read/write electronics.


Figure 1-2 RS64 Disk File Major Assemblies*
1.3.3.1 Wired Assembly - The wired assembly contains the read/write modules and provides the connectors for the data and timing cables, the power supply extender cable, and the controller cables. The assembly consists of a logic frame that houses six connector blocks each capable of accepting eight single-height modules or four double height modules. Wire-wrap connections are used between connector blocks. A fan, located on the module side provides forced-air cooling for the modules. The wired assembly is hinged at each end and can be rotated on it horizontal axis for convenient servicing
1.3.3.2 Power Control Panel Assembly - The power control panel assembly contains the receptacles for primary power connections, an RFI filter, and circuits for local/remote control of primary power. The assembly is attached to the chassis by four screws and can be removed readily for internal access. All electrical connections between the panel and other assemblies are made using connectors on the external portion of the assembly. The internal wiring of this assembly determines if the unit is used with 115 V or 230 V .
1.3.3.3 Disk Select and WLO Panel Assembly - This assembly contains the controls for selecting disk unit assignment and track write protection (write lockout). A 5 -position rotary switch is used for disk file assignment ( 0 through 3) and for placing the unit off-line (OFF). Five rocker switches are used for the write lockou unction. The upper rocker switch enables or disables the write lockout function. With this switch in the enable position, all tracks from 00 through the track number selected by the other four rocker switches are write protected. The rotary switch and the five rocker switches are mounted on a PC module located behind the panel. A flat Mylar cable connects this assembly to the wired assembly.

### 1.3.3.4 Power Supply

The power supply is located on the rear of the cabinet (Figure $2-5$ ). The supply provides $-15 \mathrm{~V},+5 \mathrm{~V}$ and +20 V for the read/write electronics. A power supply extender cable is used to connect the power supply and the main chassis of the drive unit. Primary ac power is routed from the power control panel to the supply via the extender cable. The dc output from the supply is routed to the wired assembly also via the extender. See Figure 2-6 for power supply cabling. Additional power supply information is given in Appendix B.
$\frac{\text { power supply cabling. Additional power supply information is given in Appendix B. }}{\text { *The Power Supply has been removed from the main chassis and located on the rear of the cabinet (Figure } 2-5 \text { ). }}$


Figure 1-3 Power and Control Logic Assembly*
1.3.3.5 Data and Timing Cable Assemblies - Two flat Mylar data cable assemblies (Figure 1-2) interconnect the data track heads with the read/write logic. Each data cable assembly handles the signals for two head shoe assemblies; it has two 8 -track matrix-connector modules at the head end. One timing matrix cable assembly (Figure $1-2$ ) interconnects the timing heads with the read/write logic. This cable has a 6 -track matrix module at the disk end and a connector module at the logic end.

### 1.4 SPECIFICATIONS

Storage Medium
Storage Capacity
Access Time
Minimum
Average
Maximum
Data Tracks
Bits Per Track
Recording Method
Bit Density

10-in. diameter nickel-cobalt plated disk with proprietary protective coating
Up to $1,280,000$ bits

| $\mathbf{6 0 ~ H z}$ Power | $\mathbf{5 0 ~ H z}$ Power |
| :--- | :---: |
| $260 \mu \mathrm{~s}$ | $260 \mu \mathrm{~s}$ |
| 16.9 ms | 20.3 ms |
| 33.6 ms | 40.3 ms |
| 32 |  |
| Up to 40,000 |  |
| Self-clocking one-of-N, NRZI code |  |
| 1700 bpi (maximum) |  |

Timing Tracks
Write Protection Features

Motor Bearing Life

Power Requirements

Operating Environment
Storage and Shipping Environment Physical Characteristics

| Height <br> Width <br> Depth <br> Weight | Drive Chassis only |
| :--- | :--- |
| Includes power supply |  |
| Vibration |  |

Vibration
Shock

3 plus 3 spare
switches provide write protection on all binary track addresses up to and including binary track address indicated by switch selections.
Expected operating life of at least 20,000 hours under a standard computer operating environment.
$115 / 230$ Vac $\pm 15 \%$, single-phase, 47 to 63 Hz . Starting current of 6 A ; nominal operating current of 2.2A.
$40^{\circ} \mathrm{F}$ to $125^{\circ} \mathrm{F}$, ambient. Relative humidity of $20 \%$ to $80 \%$ (non-condensing)
$-40^{\circ} \mathrm{F}$ to $135^{\circ} \mathrm{F}$ (non-condensing)
$10-1 / 2$ in
19 in.
19 in.
$18-3 / 4$
64 lb
$5-20 \mathrm{~Hz} 0.020$ in. D.A. $20-500 \mathrm{~Hz} \pm 1.5 \mathrm{~g}$, any plane.
5 g's Halfsine, 10 ms duration, any plane. Suitable for office, industrial, and large vessel operation.

## CHAPTER 2

INSTALLATION AND OPERATION

### 2.1 UNPACKING AND INSPECTION

The RS64 Disk File can be shipped in a cabinet as an integral part of a system or separately in its own container for mounting in an existing cabinet. If a unit is shipped as a separate item, the power supply and the drive chassis will be shipped separately. Remove the items from the container, remove packing materials (Figure 2-1), and inspect for shipping damage. Report any damage to the carrier. Retain packing materials for possible reshipment.
The RS64 is shipped with a motor lock installed to prevent rotation of the disk during shipment. In addition, four corosote shock mount yokes, Figure 2-1, prevent bottoming of the shocks during impact. These items must not be removed until the disk is correctly installed in a cabinet.

## CAUTION

## Exercise care in unpacking the unit. Do not drop unit or subject it to unreasonable impact

If the RS64 Disk File is shipped in a cabinet, the unit is retained in place by shipping brackets located at the rear of the chassis. These brackets must be removed to extend the unit from the cabinet. Remove the shipping brackets and any packing materials and inspect the unit for shipping damage. Report any damage to the carrier

## CAUTION

Do not remove motor lock or shock mount shippin yokes until cabinet is in final installation location.
these items in place.
these items in place

## 2.2 mechanical installation

The RS64 Disk File is designed for 19 -in. equipment rack mounting and requires $10-1 / 2 \mathrm{in}$. of front panel height. Up to four disk files can be installed in an H 950 cabinet as shown in D-SD-RS64-0-11 (see Chapter 6).

If the RS64 is to be installed in an existing cabinet, it may be necessary to install the cabinet portion of the track slide assembly. Cabinet hardware ( $10-32 \times 3 / 4$ screws and $10-32$ clip nuts) shipped with the file should be used to attach the track slide assembly to the cabinet.
Once the RS64 drive chassis is correctly mounted on track slides, extend the assembly and remove the four shock mount yokes used for shipping. Next, remove the motor lock on the bottom of the motor shaft. Retain these items and the shipping brackets (and the shipping container) for possible reshipment of disk

The H737 Power Supply is mounted on the rear of the cabinet. To mount the power supply proceed as follows.

Step
1

2
Attach mounting panel 5310507 to the rear of the cabinet with four mounting screws and speed nuts. Position the panel so the top edge is even with the lower edge of the drive unit chassis (Figure 2-4).
Attach the H 737 Power Supply to the panel with four mounting screws. The adjustments should be on top (Figure 2-5).

NOTE
wer supply mounted in
this cabinet, or if this is the second supply, it should be attached to its mounting plate upside down so that the adjustments will be accessible.
Connect the power supply extender cable (7009380) between the power supply and the drive chassis.

4 Attach the two Deklasp clamps (9008340), to the extender cable. Attach one clamp 3 inches and the other 11 inches from rear of drive chassis.

### 2.3 POWER REQUIREMENTS

Model RS64A operates from a $95-135 \mathrm{~V}, 47-63 \mathrm{~Hz}$ single-phase source and model RS64B operates from a 190 $260 \mathrm{~V}, 47-63 \mathrm{~Hz}$ single-phase source. The power control panel of each model provides the facilities for connecting primary power. Each panel contains a male receptacle for input power and a female outlet for extending primary power to other units. Drawing C-BD-RS64-0-10 illustrates a typical arrangement for primary power. A mating connector rated at 15 Amperes is recommended for power input-output connections.
The power control panel also provides the receptacle for remote control for primary power and extending remote control to other units. Drawing C-BD-RS64-0-10 also illustrates a typical arrangement for remote control of power; Figure 2-2 illustrates the circuits used for remote control.

### 2.4 SIGNAL CONNECTIONS

Drawing C-DB-RS64-0-9 shows a typical arrangement for connecting up to four RS64 Disk Files on a controller bus. This drawing also defines the cable types. Bus length should be 35 ft or less and a G739 terminator card should be used in the last RS64 unit on the bus.


Figure 2-1 RS64 Disk File Packaging

### 2.5 INSTALLATION CHECKOUT

The RS64 Disk File is thoroughly checked at the factory. However, complete diagnostics should be run after the unit is installed. Information for running the diagnostics is included with the controller

### 2.6 PREPARATION FOR MOVING AND SHIPPING DISK FILE

f the unit is to be moved or shipped in a cabinet, install motor lock and shock mount yokes. Lock the assembly in place using shipping brackets.

If the unit is to be shipped in a separate container, use the original shipping container where possible. Items used for shipping are depicted in Figure 2-1.

### 2.7 OPERATION

2.7.1 Power Control Panel Controls and Indicators

The power control panel, Figure 2-3, contains an input power indicator, a 15 A circuit breaker, and a LOCAL/OFF/ REMOTE switch. The input power indicator is lit whenever primary power is applied to input receptacle P1. Circuit breaker CB1 controls the application of primary power to the disk drive motor, the fan, the power supply relay, and the local/remote control circuits.

The LOCAL/OFF/REMOTE switch controls the application of primary power to the power supply. In the LOCAL position, it energizes the power supply relay to complete the primary power path. In the OFF position, this switch interrupts the control path for the power supply relay to remove primary power.


Figure 2-2 Remote Control and Interlock Connections

The REMOTE position permits power supply turn-on by a remote switch closure. When used in a remote turn-on chain with other units, the LOCAL and OFF positions complete the remote turn-on chain for other units. This feature permits any device to be controlled locally yet still maintain the remote turn-on control for other units.

### 2.7.2 Disk Select and WLO Panel Controls

This panel, Figure 2-3, provides the controls for establishing a disk drive unit number and for selecting tracks that are to be write protected (write lockout).
a. UNIT SELECT - This 5 -position rotary switch establishes a unit number ( 0 through 3 ) for a drive or places it logically off-line (OFF position) with respect to a controller or program. With this switch in other than OFF, the drive is selected by a corresponding unit number from a controller. This feature permits up to four disk units to be operated from one controller.
b. WRITE LOCKOUT - This rocker switch, when placed to the ENABLE position, permits the tracks designated by the TRK ADD switches to be write protected. When placed to the DISABLE position, this switch negates any write lockout function
c. TRK ADD $2^{0}-2^{4}-$ These binary-weighted rocker switches select the tracks that are to have write lockout or write protection. The write lockout function is provided for tracks selected by the binary combination of the switches plus any lower-number tracks. For example, with the $2^{0}$ switch in the logical 1 position and all others in the logical 0 position, tracks 1 and 0 have write lockout. Similarly, with the $2^{0}$ and $2^{1}$ switches in the logical 1 position, tracks 0 through 3 inclusive are write locked.


Figure 2-3 Power Control and WLO Panel

### 2.7.3 Operating Instructions

In general, the RS64 disk is an automatic device that does not require operator intervention. To operate the de vice, simply select a unit number ( 0 through 3 ) corresponding to program assignment and apply primary power.

To set up write lockout for tracks:

## Step

## Procedure

1 Press WRITE LOCKOUT switch to ENABLE.
2 Set up TRK ADD switches to binary equivalent of the highest track number that is to have write lockout. For example, to provide write lockout for tracks 0 hrough 16 , press the $2^{4}$ switch and leave $2^{0}$ through $2^{3}$ in 0 position. To p vide write lockout for track 0 only, set all switches to 0

To discontinue write lockout for previously selected tracks, simply return WRITE LOCKOUT switch to DISABLE position.


Figure 2-4 Power Supply Mounting Panel


Figure 2-5 Placement of Power Supply


Figure 2-6 Extender Cabling Diagram

## CHAPTER 3

THEORY OF OPERATION

### 3.1 SYSTEM RELATIONSHIPS

Figure 3-1 shows the general relationships of an RS64 Disk File with a controller. Up to four disk files can be operated with one controller. Each disk file is assigned a unit number and is selected by one of four lines from operated with one controller. Each disk file is assigned a unit number and is selected by one of four lines from
the controller. Only that disk file having the unit number designated by the controller responds to a selection. When a disk is selected, it acknowledges the selection and provides the controller with timing and address information recovered from the disk. Five binary-weighted lines from the controller select one of 32 data tracks. If the data track specified in the selection is write locked, the disk file also notifies the controller.


Figure 3-1 RS64 System Relationships
When the controller synchronizes with disk timing information and recognizes the address specified by the pro gram, it begins writing or reading information at that address. For a write operation, the controller enables the gram, it begins writing or reading information and the electronics and provides the disk with serial data. A read operation is implemented whenever a write operation is not specified. A synchronizing preamble is included with the address and data so that recovery synchronization can be independent of inherent skew between timing, address and data tracks.

### 3.2 DISK SURFACE AND TRACK ARRANGEMENT

Information is recorded on the lower side of the disk plate, Figure 3-2, at a perimeter beginning approximately Information is recorded on the lower side of the disk plate, Figure $3-2$, at a perimeter beginning approximately
$3 / 4 \mathrm{in}$. from the outer edge of the disk. Four head shoe assemblies, each containing eight read/write heads, store and retrieve data. One head shoe assembly, containing six read/write heads, is used for writing and recovery of timing and address information, i.e., timing tracks A, B, and C and three spares. These head shoe assemblies are located in the disk base plate as shown in Figure 3-3. Figure 3-4 depicts the arrangement of tracks.


Figure 3-2 Disk Assembly with Cover Removed

## 33 FUNCTIONAL DESCRIPTION

3.3.1 Functional Block Description

Figure 3 -5 illustrates the functional circuits that comprise the RS64 Disk File. The upper part of this diagram depicts the disk and track selection circuits and the read and write data paths. The lower part of the diagram de picts the circuits associated with the timing and address tracks.


Figure 3-3 Disk Assembly with Head Shoes Exposed
The disk utilizes three pre-recorded timing tracks (plus three spares) and 32 data tracks for recording and recovery of data. Bit timing (and bit cell width) is established by timing track A (TTA). With the exception of an origin gap, this track contains a continuous stream of logical 1's. Timing from this track is supplied to a selfsynchronizing phase-locked clock. The phase-locked clock is used as a three times frequency multiplier; it synchronizes its output to the phase of the TTA timing stream to enable separation of sync pulses, data ones, and data zeros recovered from the other tracks.

Timing track B conveys address and data markers. The address marker denotes the beginning of an address sector on timing track C ; it occurs at least six bit times before the address preamble. Similarly, the data marker signifies the beginning of a data sector of a track.
iming track C conveys the information for addressing portions of a data track, i.e., block addresses. A synchronizing preamble and an odd parity bit are included with each block address. The number of primary divisions or blocks assigned to the data tracks determines the number of address bits. For RC11 usage, for example, data is stored in 64 blocks; thus, a 6 -bit address is required. The synchronizing preamble provided with the address permits a controller to correctly synchronize with TTC information without having to compensate for skew between the clock timing track and the address track.
nformation is continuously read from timing tracks A, B and C; however, this information is not gated to the controller until the disk file is selected. For selection of a disk file, the controller enables one of four input lines


Figure 3-4 Track Arrangement
(DISK SEL 0-3) to the Disk Select/WLO panel. If the disk file is assigned a unit number corresponding to the controller selection, the Disk Select/WLO panel provides an SEL output. This output enables the gating of timing, address, and read data to the controller. Selection of a disk file also causes the selected unit to return a SEL ACK signal to the controller. This signal informs the controller the disk file is operable and has recognized the selection

Concurrent with selection of the disk file, the controller specifies which track is to be used. This information is provided as a 5 -bit track address (TK $2^{0}-2^{4}$ ) to the track decoder circuits and a write lockout (WLO) comparator. If the track designated by the controller is one of a group selected to be write-protected (no rewriting of the track), the WLO comparator disables the disk write circuits. Thus, only a read operation can be performed for the track. Since the write lockout disables the write driver, no combination of control signals can enter information on the write locked tracks.

The track address is decoded in two parts. One decoder circuit decodes the three LSB's ( $2^{0}-2^{2}$ ) and enables one of eight center tap selector circuits to select one of eight matrix lines ( $0-7$ ). Similarly, a second decoder circuit decodes the two MSB's of the track address and enables the corresponding series switch circuits to select one of four pairs of matrix lines (octal group $0-7,10-17,20-27$, or $30-37$ ). The combination provided by the center tap selector and the series switch selects the track for an ensuing read or write operation.

A read operation is specified by the negation of a write enable (WREN) input. This input disables the disk writer circuits to allow a read operation. When the controller recognizes the address for the desired block of the selected track, it begins accepting the serial read data.

For a write operation, the controller compares the address from timing track C with the address specified by the program. Upon recognizing the correct address, the controller asserts the WREN input and provides serial NRZ data to the disk write flip-flop. This flip-flop, clocked at mid-bit time with respect to the input serial NRZ data,


$$
\begin{aligned}
& R 8 m \\
& 18-j u c-75
\end{aligned}
$$



Figure 3-5 RS64 Functional Block Diagram
toggles on each binary 1 in the input. This action reverses the record head current each time a binary 1 is present and results in the recording of a binary 1 by reversing the flux saturation.

### 3.3.2 Timing Path Logic

Drawing D-BS-RS64-0-2 shows the circuits associated with disk timing. In general, these circuits reconstruct the digital form of disk timing tracks, synchronize an internal clock with the disk bit timing track (TTA), and provide timing information to a controller when the disk is selected by the controller. Bit timing is also provided to the write data path.
Differential inputs from timing track heads TTA, TTB, and TTC are applied to read amplifier-peak detector modules E-F08, E-F07, and E-F06, respectively. These modules convert the differential bipolar input pulses (representing logical 1's) into negative-true ( 0 V ) 300 -ns strobe pulses at output pin E2. The leading edge of a strobe pulse occurs at approximately the peak of the input pulse. The read amplifier-peak detector modules also produce an output at pin H 2 that signifies the polarity of the input pulse. This signal is negative-true ( 0 V ) for a positive-input pulse and has a pulse width corresponding to the duration of the input pulse. The strobe and polarity outputs of TTA and TTC are gated to the controller whenever the disk is selected. The strobe output (CLK S or ADR S) is used as a timing reference while the polarity output (CLK P or ADR P) is used for error checking functions.

The TTA read amplifier-peak detector also provides strobe pulses to a self-synchronizing phase-locked loop consisting of an M4201 phase-locked clock and two M205 D-type flip-flops connected as a divide-by-3 counter.

This loop synchronizes the output phase with the strobe pulses recovered from TTA. For this function, the M4201 phase-locked clock compares the time occurrence of the counter output (feedback) with the TTA strobe pulses and uses the result of these comparisons to correct the frequency of a VCO. Since this VCO drives the pulses and uses the result of these comparisons to correct the frequency of a
divide-by- 3 counter, the self-correcting loop phase-locks the output phase to the TTA strobes. Counter timing relationships are provided in Figure 3-6. Additional information on the phase-locked clock is provided in the module descriptions (Paragraph 3.4.16).


Figure 3-6 Counter Timing Relationships
As mentioned previously, TTB conveys the address and data markers signifying the beginning of address or data. The address marker is identified by a negative polarity pulse recovered from TTB and a data marker is identified by a positive polarity pulse recovered from TTB. For the detection of the markers, the strobe output of the TTB read amplifier-peak detector is ANDed with its polarity output. If the polarity output at $\mathrm{F} 07-\mathrm{H} 2$ is positive and a strobe pulse is present, the timing logic provides a 300 -ns, negative-true address marker pulse to the controller. Similarly, if the polarity output at $\mathrm{F} 07-\mathrm{H} 2$ is at 0 V and a strobe pulse is present, the timing logic provides a $300-$ ns , negative-true ( 0 V ) data marker pulse to the controller.

### 3.3.3 Data Path Logic

Drawing D-BS-RS64-0-3 shows the circuits for disk selection, write lockout, and the write and read data paths. For selection of a disk file, the controller ground-asserts one of four select lines (DSK $0-3$ ). If the UNIT SELECT switch on the Disk Select/WLO panel is in a corresponding position, the ground-asserted input generates a SEL L gating level; a SEL ACK output is also returned to the controller. The SEL L signal gates disk timing, read data, and other signals to the controller bus. The SEL ACK output informs the controller the disk file is not in a powerdown or off-line state so that the ensuing operation can proceed.

A write lockout function is implemented with an M167 comparator module. This module compares the controller track address (TK $2^{0}-2^{4}$ ) with inputs from the binary-weighted TRK ADD switches. If the track address specified by the controller is equal to or less than the address selected by the TRK ADD switches, the M167 comparator output is a ground level. This output prevents turn-on of the G291 disk writer; thus, information on the track cannot be erased or changed. The ground level from the M167 comparator also generates a WLO L signal to the controller. In contrast, if the track address specified by the controller is greater than the switch selection, the M167 comparator provides an enable level to the G291 disk writer

The upper part of D-BS-RS64-0-3 shows the circuit elements comprising the write and read data paths up to the data sense lines (+DSL and -DSL). From a logic viewpoint, these paths are straight-forward and, therefore, are not discussed in detail. However, the read/write electronics are described in subsequent paragraphs.

### 3.3.4 Read/Write Electronics

As mentioned previously, data is stored serially around the disk surface by 32 fixed data heads. The controlle selects the active data read/write head with five binary-weighted lines. Drawing D-BS-RS $64-0-4$ shows the circuit elements for track selection. Note that the track address is decoded in two parts. One octal group ( $0-7,10-17$, $20-27$, or $30-37$ ) enables a related G295 series switch while decoding the lower order track address bits enables one G296 center tap selector. Once selected, the head reads or writes according to inputs from the controller.
The RS64 disk uses the Non-Return-To-Zero Inverted (NRZI) recording technique. In this technique, a change in the direction of the magnetic flux along the disk track represents a binary 1 and no change in the magnetic flux represents a binary 0 . A binary 1 is written by reversing the direction of the write current in the recording head.
Figure 3-7 illustrates in simplified form the circuits used for writing and reading of data. A head winding is represented by coil L1. This coil forms the center leg of a bridge circuit consisting of resistors R1 and R2, isolation diodes D1 and D2, and switching transistors Q1 and Q2 in the G295 series switch module.


Figure 3-7 Read/Write Electronics
When the controller reads using this head, it does so by activating the appropriate G296 center tap selector module (to select one of eight matrix lines) and the appropriate G295 series switch module (to select one of four groups). This combination connects node A to +20 V , switches transistors Q1 and Q2 on, forward biases diodes D1 and D2,
and completes a 5 mA (approximate) current path through each leg of the bridge and the differential input of the read amplifier. With equal current in the legs, no current flows in the read/write head. When data is read, the changing magnetic field from the disk surface induces a voltage in the head that appears across the differential input of the G088 read amplifier-peak detector. This voltage is subsequently amplified and converted to a digital strobe. The polarity of the voltage across the coil is a function of the direction of flux change; thus, bipolar ana$\log$ pulses are provided to the read amplifier.

For a write operation, the recording head is selected the same as for a read operation, but the bridge is unbalanced by switching the emitter of Q 1 or Q 2 to -15 V via one of the transistors in the G 291 disk writer module. This ation forces approximately 45 mA through the head coil. The direction of current flow through the head is deter mined by which G291 transistor is active this transistor switching in turn, is controlled by the state of the write flip-flop.

Figure 3-8 shows the relationships of the read and write waveforms. For a write operation, the serial NRZ write (WRT) data is clocked by the positive transition in the bit rate ( $\mathrm{F} / 3$ ) timing. Each binary 1 in the NRZ input complements the flip-flop which, in turn, switches one of the transistors in the G291 disk writer module on and its counterpart off. As a result, head current is reversed and the magnetic field is reversed on the disk surface.

Figure 3-8 also shows the corresponding analog and digital waveforms for a read operation. Note that the read voltage consists of bell-shaped pulses that peak at the maximum change in the flux pattern. Note also that the NRZI format results in bipolar pulses having alternate polarities, i.e., no two successive pulses have the same polarity. This characteristic, through the use of the DATA P output, can be used to detect errors.


### 3.3.5 Power Control Panel

Drawing D-AD-7006868-0-0 is a schematic of the 115 V and 230 V power control panels. These panels are functionally identical; they differ primarily in the wiring for the primary of the local/remote power transformer (parallel connections for 115 V and series for 230 V ) drive motor connections and rating of various components. Each control panel contains:
a. a male receptacle for primary power
b. a female utility receptacle,
c. an RFI filter ( $\mathrm{L} 1, \mathrm{~L} 2$, and C 1 ),
d. a power input indicator,
e. 15-A circuit breaker CB 1 ,
f. step-down transformer T1,
g. local/remote switch assembly S1 and
h. power supply relay K1.

Transformer T1 provides an 18 Vrms potential that is rectified by diodes on local/remote switch assembly S1. The resulting potential is used as a supply voltage to energize K1. The LOCAL/OFF/REMOTE switch complete the energizing path for K 1 by providing a ground input to K 1 . This input can be supplied as a result of positioning the switch to LOCAL or by a remote switch closure when the switch is in the REMOTE position.

### 3.3.6 Power Supply

Refer to Appendix B for power supply coverage.

### 3.4 MODULE DESCRIPTIONS

### 3.4.1 G088 Read Amplifier-Peak Detecto

The read amplifier-peak detector reconstructs the digital form of bipolar analog pulses read from disk timing and data tracks. Disk head inputs are provided in differential form and all outputs are TTL compatible.
Functionally, the G088 module consists of a differential amplifier and a peak detector as shown in Figure 3-9, Drawing DS-C-G088-0-1 is a schematic of the G088 module.


Figure 3-9 G088 Read Amplifier-Peak Detector Simplified Diagram

The read amplifier portion is a 3-stage, discrete-component differential amplifier (Q1 through Q6) with a 3 dB bandwidth from 60 kHz to 700 kHz . The amplifier has linear gain characteristics (up to a maximum gain of 1000 ) for low-level inputs (up to 10 mV ) and nonlinear gain characteristics (gain compression) to prevent peak distortion at higher level inputs. Diodes D5, D6, D10, and D11 provide the gain compression features.

The differential output of the amplifier is ac-coupled to the peak detector. Figure 3-10 depicts the amplifier out put and the waveforms for the peak detector. The peak detector portion detects the peaks of the bipolar pulses provided by the read amplifier and generates a 300 -ns, negative-true strobe pulse for each peak. It also generates provided by the read amplifier and generates a $300-$ ns, negative-true strobe pulse for each peak. It also generates
a polarity output denoting the polarity of the peak; a negative pulse denotes a positive polarity input pulse. Two test points (AS2 and AT2) permit monitoring of the amplified output.


Figure 3-10 G088 Read Amplifier-Peak Detector Waveforms
Transistor stages Q8 and Q9 (with diodes D12 and D13) rectify the bipolar pulse input and provide a single-ended signal to the 100 -ns delay line and amplifier E3. Peak detection is accomplished by delaying the analog input by 100 ns then comparing the magnitude of the delayed signal with the undelayed signal. Stage E3 functions as an analog voltage comparator that is operated open-loop. Its output saturates positive whenever the delayed analog signal is more negative than the undelayed analog signal (Figure 3-10). Conversely, its output is negative whenever the difference in the analog inputs is zero or the undelayed input is more negative than the delayed input. Thus, its output approximates a digital form and is positive for each analog peak.

When both the delayed and undelayed analog inputs are at zero (no peaks), any noise that exceeds the input threshold of E3 causes spurious peaks in its output. To eliminate this aspect, the delayed analog signal is compared with a voltage reference (provided by R39 and R42) at operational amplifier E4 and the output of E4 remains negative unless the analog input exceeds the threshold reference. This threshold is set such that noise peaks cannot drive the output of E4 positive yet data peaks can. Since the output of E4 is ANDed with the output of E3, the net effect cancels noise peaks in the output of NAND gate E1 (Waveform 5, Figure 3-10). Test point BU2 is provided for adjusting the threshold. This reference is set to the midpoint between maximum noise peaks and minimum data peaks. Nominally, this reference is -1.2 V .

The pulsewidth of the strobe output is standardized by one-shot E2. This circuit, triggered by a negative transition, produces a nominal $300-\mathrm{ns}$ strobe pulse. The leading edge of this pulse denotes the data peak position. This pulse is inverted for a negative-true strobe output (Waveform 6, Figure 3-10).

Transistor stage Q7 produces a polarity pulse for each positive pulse in the disk head input. The output of Q7 is inverted for a negative-true pulse. This pulse has a duration corresponding to the width of the input pulse.

INPUTS:

Pin
$\mathrm{AE} 2, \mathrm{AF} 2$
AV2

Use
Head Differential Input
Head Center Tap

Drive or Load
5 to 10 mV
----

## OUTPUTS:

Pin
BE2
BH2
AS2, AT2
BU2
$\qquad$
$\qquad$
Read Amplifier Output Test
Points
Peak Detector Threshold Test
Point

## Drive or Load

0 TTL loads*
10 TTL loads
TL

POWER:
Pin
Use
BA2
25 mA at +5 V
AB2, BB2 $\quad 60 \mathrm{~mA}$ at -15 V
$\mathrm{AC} 2, \mathrm{BC} 2 \quad$ GND
AA2, BD2 $\quad 60 \mathrm{~mA}$ at +20 V
*One TTL unit load is 1.6 mA (maximum).

$$
\text { One TTL unit load is } 1.6 \mathrm{~mA} \text { (maximum). }
$$

$$
\text { One TTL unit load is } 1.6 \mathrm{~mA} \text { (maximum). }
$$

### 3.4.2 G291 Disk Writer

The disk writer records information on a disk. Functionally, it consists of an 80 -mA differential-current amplifier with two 4 -input AND gates for accepting complementary TTL data inputs (and gating signals) as shown in Figure 3-11. The module also contains a power-fail sensor that holds the writer off during power-up or power-down sequencing.


Figure 3-11 G291 Disk Writer Simplified Diagram
Transistor stages Q1 through Q4 (Drawing CS-G291-0-1) comprise the differential-current amplifier. Stages Q1 and Q4 are the differential input pair. Stages Q2 and Q3 function as the current sinks for writing. These stages complete the write current path between -15 V and the data sense lines (DSL). With the data input to pin U a logical 1 (and gating inputs at +3 V), Q3 completes the current path for the DSL $(-)$ line. Similarly, with the data complement at pin V a logical 1 , Q 2 connects -15 V to the DSL $(-)$ line.

Transistors Q5 and Q6 (with breakdown diodes D3 and D17) monitor the +5 V and -15 V for a power fail condition. When the sum of these potentials drops below 16.4 V , Q2 and Q3 are clamped off. This feature prevents the disk writer from recording extraneous information on the disk during power-up or power-down sequencing. A power fail output is also made available at pin P . This output is low ( 0 V ) whenever power is below the power-fail threshold.

INPUTS:

| Pin | Use | Drive or Load |
| :--- | :--- | :--- |
| U2 | Data Input | 1 TTL load |
| V2 | Complementary Data Input | 1 TTL load |
| R2, S2, T2 | Write Enable | 2 TTL loads each |

outputs:
Pin
F2
E2
P2
POWER:
Pin
A2
B2
C2
D2

| Use |
| :--- |
| Write Output |
| Complementary Write Output |
| Power Fail |

Drive or Load
80 mA (nominal) 80 mA (nominal) 10 TTL loads
3.4.3 G295 Series Switch

The G295 module is a single-height module containing two series switch circuits. It is used with the G296 center tap selector module to select disk track read/write heads. Functionally, each series switch circuit consists of an input level converter and a driver and two NPN current switches as shown in Figure 3-12


Figure 3-12 G295 Series Switch Simplified Diagram

Pin E (or V ) accepts a TTL track select input. When this input is a logical $1(+3 \mathrm{~V}$ ), the level converter-driver provides base drive for current switch pair Q1 and Q2. One of these switches, in turn, provides a current path between a Data Sense Line (DSL- or DSL+) and a track head selection matrix and passes either the $80-\mathrm{mA}$ write current or the 5 to $10-\mathrm{mV}$ read signal. This current path is completed by a G 296 center tape selector module.

| INPUTS: | TTL levels $(0 \mathrm{~V}$ and $+3 \mathrm{~V})$ to pins E and $\mathrm{V} ;-15 \mathrm{~V}$ and 0 V to pins L and M. |  |  |
| :--- | :--- | :--- | :--- |
|  | Pin | Use | Drive or Load |
|  | E and V | Track Select Enabling | 1 TTL load |
|  | L and M | Complementary Data Sense Line <br> outputs of Disk Write Module | Capable of sinking |
|  |  | 80 mA |  |

OUTPUTS: Voltage levels of 0 V or -15 V . Each series switch pole can drive up to 150 mA . At a load current of 100 mA , the internal voltage drop is approximately 1 V .

INPUT/OUTPUT DELAY: $1 \mu \mathrm{~s}$
POWER:

| Pin | Use |
| :--- | ---: |
| B2 | $81 \mathrm{~mA} \mathrm{at}-15 \mathrm{~V}$ |
| D2 | $2 \mathrm{~mA} \mathrm{at}+20 \mathrm{~V}$ |
| A2 | 20 mA at +5 V |

### 3.4.4 G296 Center Tap Selector

The G296 is a single-height module that is used with a G295 series switch module to select a disk read/write head The G296 module selects the center tap axis of this matrix, while the G295 module selects the other axis of the matrix. The module consists of four identical circuits. Each circuit uses a TTL input stage and driver and a PNP transistor switch as shown in Figure 3-13


Figure 3-13 G296 Center Tap Selector Simplified Diagram
With the TTL input at pin $E, K, N$, or $T$ at $0 V$, the circuit connects the respective output (pin $J, M, R$, or $U$ ) to the +20 V source. This action, with that of the G295 series switch, provides a current path for reading or writing

Conversely, when the TTL input is at +3 V , this circuit provides $\mathrm{a}-15 \mathrm{~V}$ potential to the head selection matrix. INPUTS: $\quad$ TTL levels $(0 \mathrm{~V}$ and $+3 \mathrm{~V})$ to pins E and $\mathrm{V} ;-15 \mathrm{~V}$ and 0 V to pins L and M

| Pin | Use | Drive or Load |
| :--- | :--- | :--- |
| $\mathrm{E}, \mathrm{K}, \mathrm{N}$ and T | Digital Input <br> (Track Select) | 1 TTL load each |

OUTPUTS: $\quad$ Each output provides 150 mA (maximum) at +10 V when respective input is 0 V .

POWER:
Pin
A2
B2
D2
C2
Use
11 mA at +5 V
22 mA at -15 V
81 mA at +20 V
GND

### 3.4.5 G738 Terminator

The G738 is a single-height module used as a cable bus terminator at the controller end of an RS64 Disk File inter face. Ten pins terminate the "fast" signal bus lines, i.e., lines that convey information by signal transition or signals having a duration less than 100 ns. These pins provide an 82 -ohm termination to ground. Fifteen pins provide termination for the "slow" signal bus lines (signals strobed by fast signals). These pins provide a termination of 180 -ohms to +5 V and 330 ohms to ground, yielding a Thevinin termination of 117 ohms and 3.25 V .

INPUTS:

Pin
D2, E2, H2
K2, M2, P2
D1, E1, F1, H1, J
K1, L1, M1, N1
P1, R1, S1, A1, B1
and $V$
F2, J2, L2, N2
R2 and U2
POWER:
Pin
A2
C2

Use
82 ohms pulldown to ground

80 ohms to +5 V and 330 ohms to ground

GND

Ise
20 mA at +5 V
GND

### 3.4.6 G739 Peripheral Terminator

The G739 is a single-height module used as a cable terminator for the last drive on the bus. Ten pins terminate the "fast" signal bus lines. These pins provide an 82 -ohm pullup to +5 V . Fifteen pins provide termination for the "slow"
signal bus lines. These pins provide a termination of 180 ohms to +5 V and 330 ohms to ground, yielding Thevinin termination of 117 ohms and 3.25 volts.

## INPUTS:

Pin
Use
A1, D2, E2, H2
K2, M2, P2
S2, T2 and V2
D1, E1, F1, H1, J1
K1, L1, M1, N1
P1, R1, S1, B1
and V 1
F2, J2, L2, N2
R2 and U2
82 ohms pullup to +5 V

180 ohms to +5 V and 330 ohms to ground

GND

POWER:
Pin
A2
C2
20 mA at +5 V
GND

### 3.4.7 G8002 Ac/Dc Low Voltage Detecto

This module monitors the rectified and filtered, but unregulated voltage from the positive winding of the power supply transformer. The AC LO signal is generated 7 ms or more before the +5 V output drops to approximately 65 percent of its nominal value. The DC LO signal is then asserted. For power up, the above sequence is reversed.

This module drives the Unibus directly, and may therefore be used for the processor to initiate a power restore routine.

## inPut:

| Pin | Use | Load |
| :---: | :---: | :---: |
| E2 | Unregulated positive supply voltage | 7 mA |
| C2 | Ground |  |
| Pin | Use | Load |
| H2 | AC LO | $\begin{aligned} & \text { Low: Sink } 20 \mathrm{~mA} \\ & \leqslant 0.3 \mathrm{~V} \\ & \text { High: Open collector } \end{aligned}$ |
| F2 | DC LO | $\begin{aligned} & \text { Low: Sink } 20 \mathrm{~mA} \\ & \leqslant 0.3 \mathrm{~V} \\ & \text { High: Open collector } \end{aligned}$ |

### 3.48 M111 Inverter

The M111 contains sixteen independent inverters.
INPUTS: Voltage levels of 0 V and +3 V (typical). Each input presents one TTL unit load.
OUTPUTS: Voltage levels of 0 V and +3 V (typical). Each output can drive 10 TTL unit loads.

POWER: $\quad 87 \mathrm{~mA}(\max )$ at +5 V .

### 3.49 M113 2-Input NAND Gat

The M113 contains ten 2-input NAND gates used for general-purpose gating functions. The module also contains a divider network so that any unused inputs of a gate can be connected to +3 V for maximum noise immunity. Pins U 1 and V 1 are provided for this function; each can supply up to 40 TTL unit loads.

$$
\begin{array}{ll}
\text { INPUTS: } & \begin{array}{l}
\text { Voltage levels of } 0 \mathrm{~V} \text { and }+3 \mathrm{~V} \text { (typical). Each input presents } 1 \text { TTL } \\
\text { unit load. }
\end{array} \\
\text { OUTPUTS: } & \begin{array}{l}
\text { Voltage levels of } 0 \mathrm{~V} \text { and }+3 \mathrm{~V} \text { (typical). Each output can drive } 10 \\
\text { TTL unit loads. }
\end{array}
\end{array}
$$

Propagation Delay: $\quad 15 \mathrm{~ns}$ (typical)
POWER: $\quad 71 \mathrm{~mA}(\max )$ at +5 V

### 3.4.10 M163 Dual Binary-To-Decimal Decoder

The M163 consists of two independent binary-to-decimal decoding structures on a single-height module (see Fig ure 3-14). Each decoder produces a negative-true ( 0 V ) output for the decimal equivalent of the binary input.


Figure 3-14 M163 Decoder Simplified Diagram
Each decoder can also be used for octal or quad decoding by grounding the most significant bit (MSB) line or MSB and next MSB input lines. Each decoder has a propagation delay of $40 \mu \mathrm{~s}$ (maximum) for input-to-output turn-on or turn-off.

[^0]
### 3.4.11 M167 Magnitude Comparator

The M167 module compares the magnitude of two 8 -bit binary numbers and provides four outputs defining the relationships of these numbers. For example, for two numbers designated A and B , the comparator defines whether $\mathrm{A}=\mathrm{B}, \mathrm{A}>\mathrm{B}, \mathrm{A} \geqslant \mathrm{B}$, or $\mathrm{B} \geqslant \mathrm{A}$. In addition, an EQUAL IN input enables cascading of modules so th hether $\mathrm{A}=\mathrm{B}, \mathrm{A}>\mathrm{B}, \mathrm{A} \geqslant \mathrm{B}$, or $\mathrm{B} \geqslant \mathrm{A}$. In addion, an LQUAL Ninput enables cascading of modules so that used comparison inputs are connected to +3 V and the EOUAL IN input is connected to ground.

The basic logic structure for a binary stage consists of an EXCLUSIVE OR, two 2-input NAND/NOR gates (one used as an inverter) and one 4 -input NAND/NOR as shown in Figure 3-15. The remaining logic elements in Fig ure 3-15 are common to all stages. A truth table is provided for the stage; it assumes all higher order inputs are equal (EQUAL IN in 0 V ).


Figure 3-15 M167 Comparator Simplified Diagram
A principle use of this module is to compare track addresses for a write lockout function. For this application, a track address is connected to the "A" input, write lockout switch levels are connected to the "B" inputs, and the A $>$ B output controls the write operation. With this arrangement, a write operation is disabled whenever the rack address is equal to or less than the write lockout switch setting. In addition, the write lockout function can be disabled entirely by simulating a track address-greater-than-switch input to the MSB stage. For this function, the MSB " B " input is connected to ground and the MSB " A " input is switched to +3 V . Conversely, to enable the write lockout function, the MSB "A" input need only be switched to OV.

INPUTS:

Voltage levels of 0 V and +3 V (typical) for all TTL inputs.

| Pin | Use |
| :--- | :--- |
| F2 | $A_{0}($ MSB $)$ |
| H1 | $A_{1}$ |
| E2 | $A_{2}$ |
| F1 | $A_{3}$ |
| C1 | $A_{4}$ |
| J1 | $A_{5}$ |
| K1 | $A_{6}$ |
| B1 | $A_{7}$ (LSB) |$\} \quad$| Drive or Load |
| :--- |

## NPUTS

(cont) Pin
H2

## $\left.\begin{array}{l}\mathrm{B}_{0}(\mathrm{MSB}) \\ \mathrm{B}_{1} \\ \mathrm{~B}_{2} \\ \mathrm{~B}_{3} \\ \mathrm{~B}_{4} \\ \mathrm{~B}_{5} \\ \mathrm{~B}_{6} \\ \mathrm{~B}_{7} \text { (LSB) } \\ \mathrm{E}^{2}\end{array}\right\}$ <br> EQUAL IN

oUTPUTS:
Pin
P1
R1
V1
L1
oltage levels of 0 V and +3 V (typical) for all outputs.

| Use | Drive or Load |
| :--- | :--- |
| EQUAL OUT (L) | 7 TTL loads |
| EQUAL OUT $(H)$ | 10 TTL loads |
| A $>\mathrm{B}(\mathrm{H})$ | 8 TTL loads |
| $\mathrm{B} \geqslant \mathrm{A}(\mathrm{H})$ | 9 TTL loads |
| $\mathrm{A} \geqslant \mathrm{B}(\mathrm{H})$ | 10 TTL loads |

POWER
Pin
Use
20 mA at +5 V
C2, T1
GND

### 3.4.12 M205 D-Type Flip-Flop

The M205 module contains five D-type flip-flops. Each flip-flop has independent DATA, CLOCK, SET, and CLEAR inputs. Information must be present on the DATA input 20 ns (maximum) before the CLOCK pulse and the information should remain at the input at least 5 ns (maximum) after the CLOCK pulse has passed the threshold voltage. Data transferred into the flip-flop by the previous CLOCK pulse will be present on the 1 output of the flip-flop. Typical time duration of the CLOCK pulse preset and reset pulses is 30 ns each. Maximum delay through the flip-flop is 50 ns .

INPUTS: D inputs present 1 TTL unit load each.
C inputs present 2 TTL unit loads each.
C inputs present 2 TTL unit loads each.
SET inputs present 2 TTL unit loads each.
CLEAR inputs present 3 TTL unit loads each.
OUTPUTS: Each output ( 0 and 1 ) is capable of driving 10 TTL unit loads. Two +3 V supplies (U1 and V1), capable of 25 unit loads, are available.
POWER $\quad 100 \mathrm{~mA}$ (maximum) at +5 V .

### 3.4.13 M623 Bus Driver

The M623 module contains twelve 2-input bus drivers capable of driving the positive input bus of a compute Drivers are arranged in six pairs, with each pair having a common gating line and two data bit inputs. For simultaneous gating of data bits, the common gating lines of each pair are connected to a single gating source. For direct output (without gating), the common gating lines are connected to signal ground. The driver output is then at ground when both inputs are at ground. Output rise and fall times are 30 ns (maximum) for a $100-\mathrm{mA}$ resistive load.

INPUTS: Pins C1, J1, P1, F2, M2, and T2 present two unit loads, when used for pair gating. Pin C1 presents 12 unit loads when connected to all other common gati R2 and S2 each present one unit load.

OUTPUTS: All outputs can sink 100 mA to ground. An open-collector NPN transistor is used as an output stage, and all output lines are protected from negative voltage of -0.3 V or greater. A maximum collector voltage of +20 V can be used.

POWER: $\quad 71 \mathrm{~mA}$ at +5 V (max) plus external load

### 3.4.14 M901 Flat Mylar Cable Connector

This connector module allows 36 lines to be used for signals and grounds. The 100 -ohm resistors connected in series with pins $\mathrm{A} 2, \mathrm{~B} 2, \mathrm{U} 1$, and V 1 provide some measure of protection if these pins are inadvertently connected to a source voltage.

INPUTS: Recommended current per line is 100 mA maximum.

### 3.4.15 M908 Ribbon Connector

The M908 cable connector consists of a single-height, double-sided board that contains 36 split pins for the connection of 36 separate wires. All connections are made on the component side of the module.

### 3.4.16 M4201 Phase-Locked Clock

The M4201 clock synchronizes disk read/write operations with the bit timing strobes recovered from a disk timing track. Basically, it consists of a phase error detector and a VCO operated in a self-synchronizing phase-lock loop track. Basically, it consi


Figure 3-16 M4201 Phase-Locked Clock Simplified Diagram

The VCO has a natural (or center) frequency of approximately 3.6 MHz ; it drives an external divide-by- 3 counter that provides a bit rate reference for the phase-lock loop. A phase error detector compares the time occurrence of that provides a bit rate reference for the phase-lock loop. A phase error detector compares the time occurrence of
the clock strobes from a disk with the bit rate reference. Errors resulting from the comparison are then integrated the clock strobes from a disk with the bit rate reference. Errors resulting from the comparison are then integrated
and converted to an analog voitage that adjusts the VCO frequency accordingly. This loop synchronizes the VCO with the clock strobes within a nominal $300 \mu$ s.
The phase error detector consists of a digital comparator stage, fast-integrator E4, long-term integrator E5, and inear amplifier E6, as shown in Drawing D-CS-M4201-0-1. The digital comparator stage consists of two D-type ip-flops in IC E2 and a NAND latch in IC E3. These logic elements accept the clock strobe input (pin BE) it rate reference input ( pin BH ) and senerate pulse outputs that drive the differential inputs of E4. Fizu 317 shows the waveforms produced by these logic elements for both a phase lead and a phase lag. The shaded areas depict the error inputs applied to the differential inputs of E4. The output of E4 is proportional to the difference between the two inputs and thus represents the bit-by-bit phase error. Integrator E5, in turn, averages the bit-bybit phase error for long-term stability. The outputs of E4 and E5 are added. The output at AV2 thus contains a component from E4 that corrects phase errors and a component from E5 that provides frequency lock. Amplifie E6 functions as a unity-gain inverting amplifier to provide the correct drive to VCO. Its output at pin AV2 is neg ative for a phase lead and positive for phase lag.


Figure 3-17 M4201 Phase-Locked Clock Waveforms
The VCO is a discrete-component RC oscillator consisting of transistor stages Q1 through Q7. It has a natural frequency of approximately 3.6 MHz (determined primarily by the network comprised of C18, R9, R26, and R11). Integrated circuit E1 buffers the VCO output and provides the necessary output drive. The clock output at pin BK is a square wave with a near 50 percent duty cycle.

INPUTS: Voltage levels of 0 V and +3 V (typical)
Pin
BE2
BH2

Drive or Load
TTL load
TTL

Feedback (Bit Rat
Reference) Reference)

OUTPUTS: Voltage levels of 0 V and +3 V (typical) for all digital outputs.

|  | Pin | Use |
| :--- | :--- | :--- |
|  | BK2 | Phase Lock Clock |
|  | BD2 | Digital Comparator Test Point |
| OUTPUTS: |  |  |
| (cont) | Pin | Use |
|  | BN2 | Digital Comparator Test Point |
|  | AV2 | Phase Detector Analog Output |
|  | AU2 | VCO Control Input |

CLOCK STABILITY: Phase jitter between clock strobe and phase-lock clock is less than 100 ns .
SYNCHRONIZING TIME: $300 \mu \mathrm{~s}$ or less

## POWER.

| Pin | Use |
| :--- | :--- |
| AK2 | 15 mA at +20 V |
| BA | 100 mA at +5 V |
| AH | $10 \mathrm{~mA} \mathrm{at}-15 \mathrm{~V}$ |
| AC, BC | GND |

### 3.4.17 8-Track Matrix 5408996

This module is part of a data cable assembly that connects the track selection logic to the data track read/write heads. It contains current-limiting resistors and isolation diodes for an 8 -track data matrix.
3.4.18 Timing Head Matrix 5408937

This connector module is part of a timing cable assembly that connects the timing head shoe to the read amplifierpeak detector modules. It contains current-limiting resistors and connections for six timing heads.

## CHAPTER 4

## INTERFACING

### 4.1 BUS VOLTAGE SPECTRUM

The recommended voltage spectrum for an RS64 controller interface is shown in Figure 4-1.


Figure 4-1 Voltage Spectrum for Controller Bus

### 4.2 BUS PHILOSOPHY

A cable assembly consisting of two 19 -conductor flat Mylar cables is used for the RS64 controller bus. One cable should be used to convey 10 "fast" bus signals, i.e., signals that convey information via a signal transition or that can be 100 ns or less in duration. This cable should have alternate signal and ground conductors and be terminated with 82 ohms to +5 V at the RS64 and 82 ohms to ground at the controller as shown in Figure 4-2.


Figure 4-2 "Fast" Bus Configuration
The second 19 -conductor cable should be used to convey 16 "slow" bus signals, i.e., signals that are strobed by the "fast" signals or used only as a level. These signals should be terminated by 180 ohms to +5 V and 330 ohms to ground at each end of the cable as shown in Figure 4-3.


Figure 4-3 "Slow" Bus Configuration
The two cables should be separated by a solid Mylar shield and attached to one M901 connector at one end to form an assembly capable of handling at least 24 signals. Signal polarity is chosen to minimize logic and to make the bus fail-safe for a power failure or unplugging of the bus cable.

### 4.3 INTERFACE SIGNALS

Figure 4-4 defines: $(a)$ the signals for an RS64-controller interface, $(b)$ the signal assertion level, $(c)$ the source of the signal and ( $d$ ) the pin usage at the RS64 Disk File end. Each interface signal is described in subsequent paragraphs.

### 4.3.1 Disk Select (DSK SEL) 0-3

Up to four disk files can be used with one controller, thus each file must be assigned a unit number. Each RS64 has a 5 -position rotary switch ( $0-3$ and OFF) for assigning a unit number or placing the unit off-line. The four DSK SEL lines are wired to corresponding positions on this switch. To select a disk for a read or write operation, the controller ground-asserts the select line corresponding to the disk unit number. No interlocks are provided to prevent multiple disk files from being assigned the same unit number

### 4.3.2 Select Acknowledge (SEL ACK)

This signal indicates that a disk file (or files) has been selected and that the selected unit does not have a powerfail condition. This line is negative-true ( 0 V ) for a select acknowledge condition.


Figure 4-4 RS64 Controller Interface

### 4.3.3 Track Select (TK SEL) $2^{0}-2^{4}$

These five binary-weighted lines select one of $32\left(00_{8}-37_{8}\right)$ data tracks for a read or write operation. Each disk file decodes these lines regardless of the file selected. Positive-true inputs are used.

### 4.3.4 Write Lockout (WLO)

This signal denotes that the write lockout feature is enabled for the selected track. This signal is negative-true ( 0 V ) for a write lockout condition.

### 4.3.5 Clock Strobe (CLK S)

This signal line conveys the bit timing information recovered from the disk. The negative-going leading edge of each 300 -ns pulse occurs at the peak of the recovered data (at each transition).

### 4.3.6 Clock Polarity (CLK P)

This signal indicates the polarity of the peak for each clock strobe. A negative-true ( 0 V ) pulse denotes a positive peak and the absence of a pulse denotes a negative peak. The clock polarity pulse can be strobed by the leading edge of the clock strobe for error detection since two or more successive pulses of the same polarity indicate an error.

### 4.3.7 Address Mark

This signal line conveys 300 -ns pulses denoting the start of the address portion of a sector. The leading edge of each negative-true pulse corresponds to the peak of the address mark recovered from the disk.

### 4.3.8 Data Mark

This signal line conveys 300 -ns pulses denoting the start of a data sector. The leading edge of each negative-true pulse corresponds to the peak of the data mark recovered from the disk.

### 4.3.9 Address Strobe (ADR S)

This signal line conveys the address information (sync, address, and parity bits) recovered from the disk. Each 300 -ns negative-true strobe signifies a logical one and the absence of a pulse signifies a logical zero. The leading edge of each strobe corresponds to the peak of a detected bit

### 43.10 Address Polarity (ADR P)

This signal indicates the polarity of the peak for each address strobe. A negative-true ( 0 V ) pulse indicates a positive peak; the absence of a pulse denotes a negative peak. The address polarity pulse can be strobed by the address strobe for error detection.

### 4.3.11 Read Data Strobe

This signal line conveys 300 -ns negative-true ( 0 V ) pulses denoting logical ones in data read from the disk; a logical zero is denoted by the absence of a strobe pulse. As with the timing strobes, the leading edge of each pulse cor responds to the peak of the detected pulse
4.3.12 Read Data Polarity

This signal indicates the polarity of the data peak for the read data strobe. A negative-true ( 0 V ) pulse denotes a positive peak; the absence of a pulse denotes a negative peak. This signal can be strobed by the read data strobe for error detection.

### 4.3.13 Write Enable (WREN)

This signal controls the writing of data on the disk. A low-level signal ( 0 V ) enables a write operation if the writ lockout feature is not enabled for the selected track. Write current is turned on as soon as WREN is asserted Write current 10 -percent turn-off and 90 -percent turn-on levels are established $200 \pm 100$ ns after a change in WREN. Therefore, WREN should be switched on and off with the Address Parity bit (at least 300 ns before the DATA MARK) to ensure adequate write current transition time.

### 43.14 Write (WRT) Dat

This signal line conveys the serial NRZ data to be written on the disk. A positive-true ( +3 V ) signal denotes a logical one in the data stream. Write data should be clocked with the leading edge of CLK S

### 4.3.15 Phase-Locked Clock (PLC)

This signal line conveys clock timing having a frequency of three times that of the CLK S frequency or 3 X bit rate (approximately 3.6 MHz ) and is in phase with CLK S. Phase jitter between CLK S and PLC is less than $\pm 100 \mathrm{~ns}$ over the full operating speed.

### 4.3.16 Master Clear (M CLR)

This signal clears the disk write flip-flop and disables the disk writer circuits. This negative-true ( 0 V ) signal ove rides any other disk signals and can be used for power-up control

### 4.3.17 AC Low (AC LO)

This signal, when ground-asserted, signifies an impending loss of dc power for the disk file and the controller Approximately 3 ms of usable power remains after this signal is switched to 0 V , thus a processor can use this sig nal to enter a power-fail routine for saving pertinent data.

### 4.4 FORMAT REQUIREMENTS

The overall requirements for disk formatting are as follows:
a. Recording Technique - NRZI recording will be used and data will be recovered using a self synchronizing phase-locked clock. The peak of a logical one flux transition, when read, is defined as the nominal data bit location.
b. Disk Speed - The disk maintains a speed from approximately 1400 to 1800 rpm for worst case input voltage and frequency extremes.
c. Origin Gap - An origin gap of sufficient length ( $50 \mu \mathrm{~s}$ or greater) will be used to facilitate writing of timing tracks.
d. Phase-Locked Clock - The phase-locked clock synchronizes with the bit timing track of the disk. This clock re-synchronizes with the bit timing within $300 \mu \mathrm{~s}$ after the origin gap.
e. Sector Gaps - Sector gaps should be long enough to tolerate worse-case speed variation and to overlap the writer turn-off functions.
f. Synchronizing Preamble - Each address and data sector will begin with a logical one - zero synchronizing pattern to provide intersymbol interference - free synchronization.
g. Clock Skew - Total dynamic and static skew (any clock to any other clock) is less than $\pm 2$ $\mu$ from the nominal bit position.
h. Data-Clock Skew - Total dynamic and static skew (any clock to any data) less than $\pm 4 \mu$ s from nominal bit position.
i. Amplifier Recovery - An interval of at least $300 \mu \mathrm{~s}$ should be allotted for write-to-read switchover or for switching of tracks.
j. Synchronization - Data on a track should be segmented in no fewer than 32 equal-sized blocks and should be synchronized for each block.

### 4.5 SYNCHRONIZING LOGIC

### 4.5.1 Write Synchronization

## The primary requirements for synchronizing a write operation are as follows:

## . WRT DATA must be clocked by the leading edge of CLK S .

b. WREN must be asserted at least 300 ns before DATA MARK. WREN can be negated at the en of the last word to be written or at the next ADDRESS MARK denoting the start of another sector.

Figure $4-5$ shows the timing for synchronization.

### 4.5.2 Read Synchronizatio

The read synchronizing logic generates read clock pulses for reading of data addresses. These clock pulses are synchronized with the phase-locked clock of the RS64 Disk File.

Figures 4-6 and 4-7 show the logic circuits and timing recommended for read synchronization. Although the circuits and timing are labeled for data usage, the same circuits and timing can be used for reading address informa tion. If the disk format does not require simultaneous usage of the circuit for both data and address, then the same circuit can be used with input gating of ADDRESS STROBE or DATA STROBE. If, however, simultaneous usage is required duplicate circuits can be used.

The read synchronizing logic generates READ CLK pulses only during the reading of the data or address portion of a block. The READ signal provides the primary control for this function. This signal is clocked by the DATA MARK or ADDRESS MARK as shown in Figure 4-7. With this signal at a ground level, the DATA, START SYNC, SYNC DATA, and START BIT flip-flops are held reset and READ CLK pulses are negated. With the READ signal asserted, these circuits provide a READ DATA output and generate the READ CLK pulses for strobing data.

The DATA flip-flop, Figure 4-6, accepts the data input from the read amplifier-peak detector. Each DATA STROBE (denoting a logical one in the data stream) triggers a 50 -ns one-shot; this stage, in turn, direct sets the DATA flip-flop. The START SYNC and SYNC DATA flip-flops select the correct phase of the phase-locked clock to be used for READ CLK pulses. The PA and PB flip-flops form a 3-state counter. A count of one is decoded to control the output gating of the selected phase. The START BIT flip-flop bypasses or prevents generation of READ CLK pulses for the sync pattern so that the first READ CLK pulse occurs with the first data bit.

The trailing edge of each READ CLK pulse is used to sample or clock the READ DATA output. With this usage the system results in data being sampled midway between the nominal DATA STROBE position as defined by the sync bits.


Figure 4-5 Write Synchronization



Figure 4-6 Read Synchronizing Interface Logic


Figure 4-7 Read Synchronizing Interface Timing

## CHAPTER 5

## MAINTENANCE

### 5.1 GENERAL

This chapter contains instructions for maintaining the RS64 Disk File. The instructions are intended for field level servicing by the user, but exclude any cleaning, repairs, or replacements internal to the disk assembly.

### 5.2 RECOMMENDED TEST EQUIPMENT

Table 5-1 lists the test equipment recommended for field servicing of the RS64 Disk File
Table 5-1

| Recommended Test Equipment |  |
| :--- | :--- |
| Equipment Manufacturer and Model/Part No. <br> Multimeter Triplett 310 or Simpson 360 <br> Oscilloscope Tektronix 453 <br> Oscilloscope Probes  <br> Voltage Tektronix P6010 <br> Current Tektronix P6019 clip-on with passive terminator <br> Wire Wrap Tool (24-gauge) DEC H811 <br> Unwrapping Tool (24-gauge) DEC H812 <br> Wire Wrap Tool (30-gauge) DEC H811A <br> Unwrapping Tool (30-gauge) DEC H812A <br> Module Extender Board DEC H982 |  |

### 5.3 PREVENTIVE MAINTENANCE

The following preventive maintenance procedures should be performed every six months or more often if deemed necessary.

Clean exterior surfaces with a soft cloth.
2 Clean the interior of equipment. Use a small brush to loosen dirt or, if necessary, the brush can be moistened with a commercial solvent. The solvent must be nonflammable, nonconducting, and not injurious to paint, plastic, and electronic components. Fumes from some solvents can be harmful to personnel and therefore should be used only in adequately ventilated areas and according to manufacturer's instructions.
Vacuum all loose dirt and other foreign particles from equipment interior Inspect all wiring and cables for cuts, breaks, kinks, fraying, mechanical security or other signs of damage or deterioration. Re-wrap or re-solder any loose con nections. When replacing wire runs, duplicate wire length and route

Inspect the power supply, modules, and panel assemblies for evidence of damaged components. Replace components that show signs of deterioration
Ensure that all modules and connectors are properly seated

### 5.4 CORRECTIVE MAINTENANCE

### 5.4.1 Module and Pin Designatio

Figure 5-1 illustrates the matrix scheme used to locate a module from the wire-wrap pin side of the wired assembly This figure also shows the pin arrangement for a connector block.
5.4.2 Power Control Panel Connector-Pin Identification

Figure 5-2 identifies the connectors and pins for the power control panel.

### 5.4.3 Power Supply Adjustments

The power supply should be checked when it is repaired or replaced. To adjust the supply outputs for optimum operation, proceed as follows:

| Step | Procedure |
| :---: | :--- |
| 1 | Turn off primary power to power supply by positioning LOCAL/OFF/REMOTE <br> switch to OFF. |
| 2 | Open rear door of cabinet to gain access to power supply. Extend the disk chassis <br> as necessary to expose power supply adjustments (Figure 5-3). <br> (continued on page 5-3) |



Figure 5-1 Module and Pin Designations


Figure 5-2 Power Control Panel Connector-Pin Identification

3 Remove power supply loads by disconnecting output connector, Figure 5-3, on top of supply.
4 Turn on primary power to the supply.
5 With no loads, adjust power supply outputs to values shown below. (Refer to Figure 5-3 for the location of adjustments and access points.)

| Output | Connector Pin | Value |
| :--- | :--- | :--- |
| +20 V | 7 or 8 | +22 V |
| +5 V | 1,2 or 3 | +5.15 V |
| -15 V | 11 or 12 | -16 V |

6 Turn off primary power to the supply and reconnect loads.
7 Turn on primary power to the supply and recheck power supply outputs under load. Readjust outputs if necessary, as indicated below.

| Output | Access Point | Readjustment |
| :--- | :---: | :---: |
| +5 V | A08-A2 | If $+5 \leqslant \mathrm{~V} \leqslant+5.15$, set to +5 V |
| +20 V | A08-S2 | If $+20 \leqslant \mathrm{~V} \leqslant+22$, set to +20 V |
| -15 V | A08-R2 | If $-15 \geqslant \mathrm{~V} \geqslant=16$, set to -15 V |

8 A08-R2
8 Turn off primary power.


Figure 5-3 Power Supply Adjustments and Connector Pin Assignments

### 5.4.4 Read Amplifier-Peak Detector Adjustments

The following adjustments should be performed when: $a$. A read amplifier-peak detector is replaced. $b$. The disk writer, any track selector modules, or timing or data cables are replaced. $c$. The disk is replaced or heads are realigned.

Initially, the read amplifier-peak detectors are statically adjusted for a nominal operating point. Next, each is dynamically adjusted using a controller for bit patterns and for error detection. The dynamic adjustment entails locating a mean point between data peaks and noise peaks. To perform these adjustments:

1 Using an oscilloscope or VOM, adjust all four read amplifier-peak detectors for static threshold operating value of -1.2 V . Access points for the read amplifierpeak detectors are as follows

| Read Amplifier-Peak Detector | Access Point |
| :---: | :---: |
| Clock | F08-U2 |
| Sector Mark | F07-U2 |
| Address | F06-U2 |
| Data | D07-U2 |

2 Write a pattern (all 1 's, for example) on one complete data track then begin a repetitive read and comparison operation for that track.
3 Connect an oscilloscope or VOM at the clock read amplifier-peak detector test point (F08-U2).
4 While monitoring for errors, slowly adjust clock threshold potentiometer for a more positive indication. When an error occurs, record the threshold indication as $\mathrm{V}_{\text {High }}$.
5 Adjust potentiometer for a more negative threshold value and observe where error occurs. Record this value as $\mathrm{V}_{\text {Low }}$.

## Pocedure

Calculate mean threshold as follows and set potentiometer for that value.

$$
V_{\text {mpt }}=\frac{V_{\text {High }}+V_{\text {Low }}}{2}
$$

Using steps 2 through 6 , set up threshold for sector mark and address read amplifier-peak detectors. Test points are as follows

$$
\begin{aligned}
& \text { Sector Mark - F07-U } \\
& \text { Address }
\end{aligned}
$$

8 For the data read amplifier-peak detector adjustment, write an all-zero pattern in every track. Next, initiate a repetitive read and comparison for track 17 (the en every track. Next, initiate a repetitive read and comparison for track $17_{8}$ th noise).
9 Connect the oscilloscope to data read amplifier-peak detector test point (D07-U2) While observing data comparison result, adjust data threshold potentiometer (for While observing data comparison result, adjust data threshold potentiometer (for ing slightly until no errors occur.

Read and compare data for all other tracks. If no errors are detected for the ther tracks, proceed with Step 11. If errors are detected (signifying tracks with greater amounts of noise than track $17_{8}$ ), record track numbers containing errors. eadjust data threshold while reading and comparing data from these tracks and ocate the noisiest track on disk.

11 Record the threshold voltage ( $\mathrm{V}_{\text {High }}$ ) for track $17_{8}$ or the noisiest track on the disk.
12 To define the lowest threshold $\left(\mathrm{V}_{\text {Low }}\right)$, write all ones for every track. Initiate a repetitive read and comparison operation for track $30_{8}$ (the innermost track will probably have lowest amplitude data peaks). Adjust data threshold potentiomete for a more negative threshold) until error occurs. Decrease threshold setting slightly until no errors occur
Read and compare data from all tracks. If no errors are detected for the other tracks, proceed with Step 14. If errors are detected (signifying tracks having data peaks less than the threshold) record track numbers. Readjust data thres old while reading and comparing data from these tracks. Locate the lowest data peak track and set up threshold for this track
14 Record the threshold voltage $\left(\mathrm{V}_{\mathrm{Low}}\right)$ for track $30_{\mathrm{s}}$ or the track having the lowest data peaks.

Calculate the mean threshold as follows and set the potentiometer for that value.

$$
\mathrm{V}_{\mathrm{mpt}}=\frac{\mathrm{V}_{\text {High }}+\mathrm{V}_{\text {Low }}}{2}
$$

### 5.4.5 Timing Track Changeover

To use the spare timing tracks

## Procedur

1 Turn off dc power to logic by placing LOCAL/OFF/REMOTE switch to OFF.

## Procedure

isconnect timing cable assembly at head shoe 1 , rotate head matrix connector $180^{\circ}$, then reconnect cable

```
Turn on dc power to logic.
```


## NOTE <br> Readjust read amplifier-peak detector threshold for all timing tracks before attempting further operation

### 5.4.6 Rewriting Timing Track

Timing tracks should be rewritten whenever the disk surface is replaced or the timing tracks are partially or com pletely destroyed. To rewrite RS64 timing tracks:

## Procedure

Remove dc power from RS64 logic by placing the LOCAL/OFF/REMOTE switc on RS64 power control panel to OFF. The ac power to the drive motor should remain on
2 Disconnect timing cable assembly from module slot E09 and connect it to the timing track writer I/O connector.
Disconnect the dc power connector on top of RS64 power supply and connect track writer power cable to power supply
On track writer, select 50 Hz or 60 Hz timing, as applicable, then place all othe switches to OFF position.
Apply dc power to the track writer by placing the LOCAL/OFF/REMOTE switch to LOCAL.
On the track writer, place the WRT ENABLE switch to ON and observe that WRITE VLT indicator lights.
7 Place MAINT switch to ON and observe gap width indicators. If the INCREASE indicator is flashing, turn gap ADJ clockwise until GAP OK indicator flashe Similarly, turn gap ADJ counterclockwise until GAP OK indicator flashes. Place MAINT switch OFF. To write timing track, depress PUSH-TO-WRITE switch.
9 Turn off WRT ENABLE switch. Remove dc power by placing the LOCAL/ OFF/REMOTE switch to OFF.
Disconnect track writer power cable at RS64 power supply. Disconnect timing Disconnect track writer power cable at RS64 power supply. Disconnect timing Connect RS64 logic dc power cable at top power supply, then apply dc power by returning the LOCAL/OFF/REMOTE to the normal operating position.
Adjust all timing track read amplifiers (refer to Paragraph 5.4.4 for procedures) Following these adjustments, thoroughly test the operation of the disk.

### 5.4.7 Troubleshooting Recommendations

5.4.7.1 General - The following remedial action is recommended when a malfunction is detected.

Investigate all available information concerning the malfunction.
2 Where possible, substitute a known operable disk file to isolate malfunction between the controller and the suspected malfunctioning unit.
3 If an error occurs for a group of addresses, always check the write lockout switches to ensure that the group is not included in write lockout function.

4 In general, diagnostic error printouts classify errors in four primary categories These error categories and the recommended isolation approach are described in subsequent paragraphs.
5.4.7.2 Track Address Errors - Track address errors can be of two primary types, i.e., those involving a group of tracks or individual tracks.

Step

## Procedure

For errors associated with octal groups $0-7,10-17,20-27$, and $30-37$, initiate repetitive write operation for the malfunctioning group. Check the series switch output associated with that group for a write transition. Refer to D-BS-RS64-0-4 for access points and track group circuits.
2 For errors associated with octal groups $0,10,20$, and 30 or $1,11,21$, or 31 , etc., initiate a repetitive write operation for the malfunctioning group. Check the center top module associated with the grouping. Refer to D-BS-RS64-0-4 for access points.

3 For individual track errors, initiate a repetitive write operation and check the M163 decoder output for the selected track for a negative-true ( 0 V ) pulse. Also check cable connections and wiring for the track. Refer to D-BS-RS64-0-4 for access points, levels, and wiring connections.
5.4.7.3 Sector Address Errors - To check and further isolate sector address errors:

Step
Procedure
1 Check address marks and address strobes at digital interface. Refer to Figure 5-4 for oscilloscope set up and waveforms. This figure depicts the last address ( $77_{8}$ ) of track. Beginning at address 0 or $77_{8}$, verify the remaining addresses are presen by changing the delay interval.

2 If address marks or strobes are not present, check for at least a 6 V p-p analog signal at TTB or TTC read amplifier peak-detector. Figure $5-5$ shows the address strobes and analog waveform for address $75_{8}$. If analog signal is good, readjust related read amplifier-peak detector (Paragraph 5.4.4).

3 If the analog signal is abnormal, substitute the read amplifier-peak detector. If the analog signal is still abnormal, reverse the timing cable to use spare tracks (Paragraph 5.4.5) or rewrite timing tracks (Paragraph 5.4.6).
4 If malfunction is isolated to the disk or disk heads, only authorized personnel should attempt repair


A deLared by b
B SYC - origin gap
SYNC-ADDRESS MARK EO3-S2
Figure 5-4 Address Mark and Address Strobe

 $\qquad$
Figure 5-5 Address Strobe and Analog Signal
5.4.7.4 Timing Errors - To check and isolate clock timing errors

## Procedure

Check the relationship of CLK S and PLC. Figure $5-6$ shows the relationship o these signals plus access points and oscilloscope setup. The negative transitions of each clock strobe should occur within 100 ns of a negative transition in the phase-locked clock.
continued on next page)


Figure 5-6 Clock Timing Signals
Step

## Procedure

2 If the phase-locked output is abnormal, check the M4201 Clock (module slo CD1) and the divide-by-3 counter (module slot D02).
3 If the CLK S is abnormal, check its associated read-amplifier-peak detector. This check can be made in the same general manner as described for sector address (Paragraph 5.4.4).
4 If the malfunction is isolated to the disk, reverse timing cable to use spare tracks (Paragraph 5.4.5). If this action does not correct the problem, rewrite the timing tracks (Paragraph 5.4.6).
5 If malfunction is isolated to disk or disk heads and cannot be corrected by writing timing tracks, only authorized personnel should attempt repair
54.7.5 Data Errors - Data errors are generally classified as hard (equipment failure) or random (occurring without any recognizable pattern). Random errors are generally caused by marginal supply voltages, marginal timing marginal disk writer current, or misadjustment of the data read amplifier-peak detector. A general approach to isolating data errors is as follows:

Step

## Procedure

1 Check the write lockout switches to ensure that data error is not caused by write lockout function.
2 Check $+5 \mathrm{~V},-15 \mathrm{~V}$, and +20 V potentials. Refer to Paragraph 5.4.3 for operating limits and adjustment procedures.
3 Check clock timing. Refer to Paragraph 5.4.7.4 for timing error checks.
4 Continuously write an alternating one-zero pattern or another readily recognizable pattern and check the disk write circuits. Figure 5-7 depicts the relationship of write (WRT) Data and the disk writer output.


SYNC-wREN bo3-F2
Figure 5-7 WRT Data and DSL Relationships

Step
5
If the disk writer output is normal, check the data read amplifier-peak detector strobe and analog signals and adjust peak detector threshold if necessary. (Refer to Paragraph 5.4.7.3 for typical read amplifier-peak detector checks.)
6 If malfunction is isolated to the disk assembly, only authorized personnel should attempt repair.

### 5.5 REMOVAL AND REPLACEMENT

5.5.1 Removal of Disk Assembly

## CAUTION

Do not attempt removal of disk assembly without motor lock installed.

## Procedure

Remove primary power and disconnect drive motor cable at power control panel.
Disconnect four data head matrix connectors and timing head connector at disk base.
Install motor lock on base of motor shaft.
Disconnect ground strap. Retain hardware.
Using a $5 / 32$ Hexagon wrench, remove four bolts that attach deck plate to shock absorber mounts. Retain bolts and nuts for reassembly
Disk assembly is now ready for removal.

## CAUTION

Exercise care in handling disk assembly. Do not
drop or subject disk assembly to heavy impact be cause heads can be damaged or misaligned.

### 5.5.2 Reinstallation of Disk Assembly

## Procedure

1 If power control panel, and disk select/WLO panel have not been removed, remove these items to gain working access.

2 Position disk assembly over shock mounts and attach shock mounts to base plate.
3 Connect head matrix connector for head shoe 2 first, then continue in a counter clockwise direction with balance of head matrix connectors. The shorter cable from module slot B09 mates with the head shoe 2 connector. Similarly, the shorter cable from module slot C 09 mates with the head shoe 3 connector. Refer to Drawing D-BS-RS64-0-6 for the location of head shoes.

4 Reconnect ground strap.
5 Remove motor lock on base of motor shaft.
6 Install power control panel, and disk select/WLO panel
7 Reconnect disk drive motor and disk select/WLO panel. Connect fan and any remote control lines.

## .6 RECOMMENDED SPARE PARTS

Table 5-2 lists the spare parts recommended for the RS64 Disk File.
Table 5-2
Recommended Spare Parts

| DEC Type/Part No. | Figure | Description | Quantity |
| :--- | :---: | :--- | :---: |
| $1210167-0$ | $5-2$ | Breaker, Circuit (APL-11-1-6-0-502 Air Pax) | 1 |
| $7007049-0-0$ | $1-2$ | Cable Assembly, Data | 1 |
| $7006111-01$ | - | Cable, I/O | 1 |
| $7007238-0-0$ | - | Cable Assembly, Power | 1 |
| $7007050-0-0$ | $1-2$ | Cable Assembly, Timing | 1 |
| 1002153 | $5-2$ | Capacitor; 2X 0.1 mfd, 600 Vdc | 1 |
| 1005767 | $5-2$ | Capacitor, GE \#72F6211, $10 \mathrm{mfd}, 330 \mathrm{~V}, 60 \mathrm{~Hz}$ | 1 |
| 1209378 | - | Contact, Male, Mate-N-Lock | 6 |
| $7408624-0-0$ | - | Cover, Module | 1 |
| $1205033-01$ | $1-3$ | Fan | 1 |

Table 5-2 (Cont)
Recommended Spare Parts

| DEC Type/Part No. | Figure | Description | Quantit |
| :---: | :---: | :---: | :---: |
| 9009039 | 5-2 | Fuse, 2/10 Amp, Slo-Blow | 5 |
| 9007242 | - | Holder, Fuse, HKP | 1 |
| 1209351-12 | - | Housing, Pin, 1-480278-0 | 1 |
| 1201280 | 5-2 | Lamp, Pilot 1020C55, 125V | 1 |
| M623 | D-MU-RS64-0-8 | Module, Bus Driver | 1 |
| G296 |  | Module, Center Tap Selector | 1 |
| M205 | $\downarrow$ | Module D-Type Flip-Flop | 1 |
| G291 | D-MU-RS64-0-8 | Module, Disk Writer | 1 |
| M163 |  | Module, Dual Binary-to-Decimal Decoder | 1 |
| M111 |  | Module, Inverter | 1 |
| G8002 |  | Module, Low-Voltage Detector | 1 |
| M167 |  | Module, Magnitude Comparator | 1 |
| M4201 |  | Module, Phase-Locked Clock | 1 |
| G739 |  | Module, Peripheral Terminator | 1 |
| G088 |  | Module, Read A nplifier-Peak Detector | 1 |
| G295 |  | Module, Series Switch | 1 |
| G738 |  | Module, Terminator | 1 |
| M113 | $\downarrow$ | Module, 2-Input NAND Gate | 1 |
| H737 | 1-3 | Power Supply | 1 |
| None | 5-2 | Relay, (\#KRP-1 1DE Potter and Brumfield) | 1 |
| 1302407 | - | Resistor, 47K, 1/2W | 1* |
| 5409182 | 5-2 | Switch Assembly, Remote/Local | 1 |
| 1102915 | - | Thyrector, 115V | 1* |
| 1100106 | - | Thyrector, 230V | 1* |
| 161050-0 | 5-2 | Transformer | 1 |
| 1605147 | - | Tube, Ferrite | 1 |

Table 6-1 lists the mechanical and electrical drawings supplied with this manual. A set of engineering drawings is also supplied with each disk file. If drawing differences are observed, the drawings supplied with the equipment take precedence. Table 6-2 defines the signal mnemonics used on the block schematics.

| Table 6-1 <br> Drawings |
| :--- |
| Drawing Number Title Page <br> D-SD-RS64-0-11 Maximum Configuration $6-3$ <br> C-BD-RS64-0-9 Signal Bus Configuration $6-4$ <br> C-BD-RS64-0-10 Power Cable Configuration $6-5$ <br> D-MU-RS64-0-8 Module Utilization $6-6$ <br> D-BS-RS64-0-2 Timing Path $6-7$ <br> D-BS-RS64-0-3 Data Path $6-8$ <br> D-BS-RS64-0-4 Track Selectors $6-9$ <br> D-BS-RS64-0-5 I/O Connectors $6-10$ <br> D-BS-RS64-0-6 Head Matrices $6-11$ <br> D-AD-7006858-0-0 Control Panel $6-12$ <br> D-CS-G088-0-1 G088 Read Amplifier-Peak Detector Schematic $6-16$ <br> CP-0048 G088 Read Amplifier-Peak Detector Component Location $6-17$ <br> C-CS-G291-0-1 G291 Disk Writer Schematic $6-18$ <br> CP-0052 G291 Disk Writer Component Location $6-18$ <br> B-CS-G295-0-1 G295 Series Switch Schematic $6-19$ <br> CP-0047 G295 Series Switch Component Location $6-19$ <br> B-CS-G296-0-1 G296 Center Tap Selector Schematic $6-20$ <br> CP-0046 G296 Center Tap Selector Component Location $6-20$ <br> B-CS-G738-0-1 G738 Terminator Schematic $6-21$ <br> CP-0109 G738 Terminator Component Location $6-21$ <br> B-CS-G739-0-1 G739 Peripheral Terminator Schematic $6-22$ <br> CP-0045 G739 Peripheral Terminator Component Location $6-22$ <br> B-CS-G8002-0-1 G8002 Low Voltage Detector Schematic $6-23$ <br>  G8002 Low Voltage Detector Component Location $6-23$ <br> B-CS-M111-0-1 M111 Inverter Schematic $6-24$ <br> CP-0039 M111 Inverter Component Location $6-24$ <br> B-CS-M113-0-1 M113 2-Input NAND Gate Schematic $6-25$ <br> CP-0042 M113 2-Input NAND Gate Component Location $6-25$ <br> B-CS-M163-0-1 M163 Dual Binary-to-Decimal Decoder Schematic $6-26$ |

## Table 6-1 (Cont)

Drawings

| Drawing Number | Title | Page |
| :--- | :--- | :--- |
| CP-0044 | M163 Dual Binary-to-Decimal Decoder Component Location | $6-26$ |
| D-CS-M167-0-1 | M167 Magnitude Comparator Schematic | $6-28$ |
| CP-0037 | M167 Magnitude Comparator Component Location | $6-29$ |
| B-CS-M205-0-1 | M205 D-Type Flip-Flop Schematic | $6-30$ |
| CP-0053 | M205 D-Type Flip-Flop Component Location | $6-30$ |
| C-CS-623-0-1 | M623 Bus Driver Schematic | $6-31$ |
| CP-0059 | M623 Bus Driver Component Location | $6-31$ |
| B-CS-M901-0-1 | M901 Flexprint Cable Connector Schematic | $6-32$ |
| CP-0040 | M901 Flexprint Cable Connector Component Location | $6-32$ |
| B-CS-M908-0-1 | M908 Ribbon Connector Schematic | $6-33$ |
| CP-0043 | M908 Ribbon Connector Component Location | $6-33$ |
| D-CS-M4201-0-1 | M4201 Phase-Locked Clock Schematic | $6-34$ |
| CP-0038 | M4201 Phase-Locked Clock Component Location | $6-35$ |
| B-CS-5408998-0-1 | RS64 Disk Select | $6-36$ |
| CP-0051 | Write Lockout Panel Component Location | $6-37$ |
| B-CS-5408996-0-1 | 8-Track Matrix 5408996 Schematic | $6-38$ |
| CP-0049 | 8-Track Matrix 5408996 Component Location | $6-38$ |
| B-CS-5408937-0-1 | Timing Head Matrix 5408937 Schematic | $6-39$ |
| CP-0050 | Timing Head Matrix 5408937 Component Location | $6-39$ |
| D-UA-H737-0-0 | H737 Power Supply (sheet 1 of 2) | $6-40$ |
| D-UA-H737-0-0 | H737 Power Supply (sheet 2 of 2) | $6-41$ |
| D-CS-H737-0-1 | Power Supply (H737) | $6-42$ |
| E-IA-5409484-0-0 | 8 to 20V Regulator (sheet 1 of 2) | $6-43$ |
| E-IA-5409484-0-0 | 8 to 20V Regulator (sheet 2 of 2) | $6-44$ |
| D-CS-54094840-1 | 8 to 20V Regulator | $6-45$ |
| E-IA-5409503-0-0 | +5 Volt Power Regulator | $6-46$ |
| D-CS-5409503-0-1 | +5 Volt Regulator | $6-47$ |
|  |  |  |

Table 6-2

| Mnemonic | RS64 <br> Source Drawing | Meaning |
| :---: | :---: | :---: |
| AC LO | -0-3 | $A C$ Low; level change denoting an imminent loss of dc power for disk and controller. |
| ADR P | -0-2 | $A D$ dRess Polarity; polarity pulse from the address track read amplifier-peak detector. |
| ADR S | -0-2 | $A D \mathrm{~d} R$ ess $S$ trobe; strobe pulse from the address track read amplifier-peak detector. |
| CLK P | -0-2 | $C L o c K$ Polarity; polarity pulse from the clock track read amplifier-peak detector. |
| CLK S | -0-2 | $C L$ ocK $S$ trobe; strobe pulse from the clock track read amplifierpeak detector. |
| DSK 0 - DSK 3 SEL | -0-5 | DiSK SELect; discrete selection levels for selecting disk files 0 through 3. |
| DSL (+) | $\begin{aligned} & -0-3, \\ & -0-4 \end{aligned}$ | $D$ ata Sense $L$ ine (positive); positive data line for selected read/ write head. |
| DSL (-) | $\begin{aligned} & -0-3, \\ & -0-4 \end{aligned}$ | $D$ ata $\operatorname{Sense} L$ ine (negative); positive data line for selected read/ write head. |
| F/3 | -0-2 | Phase-Lock Clock Frequency divided by three. |
| LOCK DIS | -0-3 | Write LOCK DISable; disable line for write lockout function. |
| M CLR | -0-5 | Master $C L$ ear ; initializing signal for write electronics. |
| PLC | -0-2 | Phase Lock Clock; output of phase-locked clock (3 times bit rate). |

Table 6-2 (Cont)
Signal Glossary

| Signal Glossary |  |  |
| :---: | :---: | :---: |
| Mnemonic | RS64 <br> Source Drawing | Meaning |
| READ DATA P | -0-3 | READ DATA Polarity; polarity pulse from data read amplifierpeak detector. |
| READ DATA S | -0-3 | READ DATA Strobe; strobe pulse from data read amplifierpeak detector. |
| SEL | -0-3 | SELect; output level of drive select switch denoting selection this drive. |
| SEL ACK | -0-3 | SELect $A C K$ nowledge; acknowledge signal for selected drive. |
| SW 0-SW 4 | -0-3 | Write Lockout SWitch; SW 0 corresponds to LSB $\left(2^{\circ}\right)$ of track address selected for write lockout; SW 4 corresponds MSB $\left(2^{4}\right)$. |
| TK $2^{0}-$ TK $2^{4}$ | -0-5 | TracK Address Bits defining one of 32 tracks. |
| TK 0 - TK 7 | -0-4 | TracK $0-7$; center tap lines for octal groups X0 through X7 of data head matrix. |
| $\begin{aligned} & \text { TRK } 0-7,10-17 \text {, } \\ & 20-27,30-37 \end{aligned}$ | -0-4 | $T R a c K$; series switch selection lines for data head matrix groups $0_{8}$ through $7_{8}, 10_{8}$ through $17_{8}, 20_{8}$ through $27_{8}$, and $30_{8}$ through $37_{8}$. |
| wLO | -0-3 | Write $L$ ock $O$ ut; control level that denotes a write lockout condition is established for the selected track. |
| WREN | -0-5 | $W R$ ite $E N$ able; control level that enables the writing of data. |
| WRT DATA | -0-5 | WRiTe DATA; serial NRZ data input to be written on selected track. |















| DIGITAL EOUIPMENT CORPORATION PARTS LIST |  |  |  |  | jantity / variatio |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  | 场 |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  | DESCRIPTION |  |  |  |  |  |  |
| 23 | 9006560 |  |  | NUT KEPS \#6-32 |  |  |  |  |  |  |  |  |  |
|  | 9007242 | FUSE HoLDER \#\#IP |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
| 26 | C-IA-5409182 | FUSE $2 / 10 \mathrm{AMP} \mathrm{S,B}$, |  | 1 |  |  |  |  |  |  |  |
|  | 9006776 | Comv sowierubss |  | ${ }^{18}$ |  |  |  |  |  |  |  |
| 28 | 9007917 | Conv Soldencess, SPADE |  | 1515 |  |  |  |  |  |  |  |
|  | $9107430-29$ |  |  |  |  |  |  |  |  |  |  |
|  | 9107430 | WIRE \#18 AWG, TWISTED PR RED/WHI |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  | SRes |  |  |  |  |  |  |  |
| 32 | 9107360-22 |  |  | a/8a/B |  |  |  |  |  |  |  |
|  | 9107360-99 | WIRE \#18 AMG |  | (8a/8 |  |  |  |  |  |  |  |
| 34 | 1605147 |  |  | 22 |  |  |  |  |  |  |  |
| 35 | 9007235 |  |  | ${ }^{1} 1$ |  |  |  |  |  |  |  |
| 36 | 1102915 | THYRECTOR 230V (6RS20SP989) |  | 02 |  |  |  |  |  |  |  |
|  | 1100106 | THYRECTOR IISV (6RS205P4B4) |  | 20 |  |  |  |  |  |  |  |
| 38 | 9107256 |  |  | 2/Re/B |  |  |  |  |  |  |  |
|  |  | HEAT SHRINK TUBING |  |  |  |  |  |  |  |  |  |
| 40 | 1270453 |  |  | $\square$ |  |  |  |  |  |  |  |
| 41 | D-7409066 | DECALS |  |  |  |  |  |  |  |  |  |
| 42 | 9008152 | INSULATOR CAP |  | 22 |  |  |  |  |  |  |  |
|  | 9006633 |  |  | 88 |  |  |  |  |  |  |  |
|  | 44 9008143 |  |  |  |  |  |  |  |  |  |  |
|  | CONTROL PANEL A |  |  |  | NUMBER$7006858 \div 0-\theta$ |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |





















$\underset{\substack{\text { NOTE: } \\ \text { R25 } \\ \text { IS ENG'S OPTION }}}{ }$













## APPENDIX A

## RC11 FORMAT AND RS64 TIMING TRACK WRITER

A. 1 RC11 FORMAT
A.1.1 Data Organization

Data is organized in block format on the disk as follows:
a. 32 data tracks per disk
b. 64 data blocks per track
c. 32 data words per block

With this arrangement, the storage capacity of the disk is 65,53616 -bit words.

## A.1.2 Disk Timing Tracks

There are six prerecorded timing tracks ( 3 timing tracks are spares) on the disk. The timing tracks (designated A, B, and C) are used as follows
a. TTA - Clock timing track
b. TTB - Address and data sector marker track
c. TTC - Sector address code track

## A.1.3 Addressing Data on Disk

The following parameters are used for addressing disk content
a. A 2-bit code selects any one of four disk files assigned a corresponding unit number
A. A 5 -bit track select code addresses any one of the 32 data tracks.
c. A 6 -bit address code on the prerecorded address track (TTC) defines 64 data blocks.
d. An address code on TTC and the data block for this address is designated a sector

## A.1.4 Address and Data Demarkation

The address and data marker track (TTB) is prerecorded with address and data markers that identify the beginning of an address on TTC or data on one of the data tracks. These markers are logical ones recorded at appropriate places on TTB as shown in Figure A-1. Address and data markers are distinguishable by the polarity of the induced signal.

## A.1.5 Controller Clockin

With the exception of the origin gap, the A timing track contains a continuous stream of clock pulses as shown in Figure A-1. All controller major events are derived from the master clock signals recovered from this track.


Figure A-1 RC11 Format

All address codes and data blocks are written with a 2 -bit synchronizing preamble consisting of a logical one followed by a logical zero. The synchronizing preamble enables self-clocking of address and data to eliminate inherent skew between tracks.

## A.1.6 Disk Track Format

For control purposes, the disk surface is divided into 65 equal blocks plus an origin gap (Figure A-1). Each block consists of a segment of 600 TTA pulses. Data can be recorded in all blocks except the block immediately following the origin gap. This block is used for synchronizing the RS64 phase-locked clock with TTA pulses.
An address marker is recorded on TTB the seventh clock time of each data block. The sector address on TTC begins at the 13th clock time of each block. The first two bits are the synchronizing preamble. The 6 -bit address begins at the 15 th clock time and is recorded with the LSB first. A parity bit follows the MSB
A data marker is recorded on TTB the 27th clock time of each data block and data begins on the 34th clock pulse The first two clock times are allotted for the synchronizing preamble. The last word in a block is a block parity word and ends on the 596th clock pulse.

As denoted in Figure A-1, the disk write circuits are enabled at the 21 st clock time. This action ensures that logical zeros are written on the data track shortly before and after sensing the data mark. This action prevents any spurious transitions appearing in that area of the data track from creating a false sync pattern.

## A. 2 RS 64 TIMING TRACK WRITER

The RS64 timing track writer records timing tracks A (clock), B (address and data marks), and C (address) on an RS64 Disk. Three spare timing tracks are written at the same time.

To write the timing tracks, the RS64 timing cable assembly is disconnected at the logic assembly and is connected to the timing track writer outputs shown in Figure A-2. A track writer cycle begins when the PUSH-TO-WRITE switch is depressed. As a result of this action, the track writer erases the timing tracks by writing zeros for at leas 50 ms . Following this action, the track writer starts writing timing track A (TTA) and TTA Spare. These tracks establish the bit cell or basic clock timing for the disk as shown in Figure A-1.

After writing one block of 600 clock pulses for TTA (this block is allotted for disk clock resynchronization), the track writer begins recording address and data sector marks on TTB, consecutive addresses on TTC, and continue the recording of clock pulses on TTA. Figure A-1 shows the location of address and data marks within a block and the arrangement of address bits on TTC.
The track writer continues writing of TTA, TTB, and TTC until 64600 -bit blocks (and one 600 -bit block for clock synchronization) have been written. Upon sensing that 65 equal length blocks have been recorded, the track writer concurrently disables the TTA, TTB, and TTC disk writers and triggers its gap detection circuits to signify the start of an origin gap. The track writer determines gap length by using the first TTA clock pulse after the gap to reset the detection circuits. An incorrect gap is corrected by adjusting the frequency of the clock and rewriting the timing tracks.


Figure A-2 Timing Track Writer Block Diagram

## APPENDIX B

POWER SUPPLY

The power supply produces regulated $+5 \mathrm{~V},-15 \mathrm{~V}$, and +20 V operating potentials for the RS64 Disk File. The +5 V supply can also provide the operating potentials for an external logic load (for example, a controller) of up to 4.5 A .

The power supply can be operated from a 115 V or 230 V source by changing the connections of the power trans former windings. Input power ranges are

100 to $135 \mathrm{Vac}, 47$ to 63 Hz
200 to $250 \mathrm{Vac}, 47$ to 63 Hz
Load current rating for the three supplies is as follows:
+5 Vdc at 6 A
+20 Vdc at 1 A
-15 Vdc at 1.5 A
The outputs are regulated to within the voltage bands specified below with full input voltage and frequency variations and from zero to full load current:

| Output | Regulation |
| :--- | :--- |
| +5 V | $+5 \pm 0.15 \mathrm{Vdc}$ |
| +20 V | $+20 \pm 2 \mathrm{Vdc}$ |

$+20 \mathrm{~V} \quad+20 \pm 2 \mathrm{Vdc}$ $-15 \mathrm{~V}-15 \pm 1 \mathrm{Vdc}$

The power supply regulators (Drawing Nos. 5409503 and 5409484 ) contain the following features:
a. Positive switching
$b$. Internal crowbars
c. No remote sensing
d. Output power is limited and adjustable ( $8-20 \mathrm{Vdc}$ regulator)
e. Adjustable output current ( +5 Vdc regulator)

Table B-1 lists the regulator module adjustments.
Table B-1
Regulator Module Adjustmen

| Regulator Module Adjustment |  |  |
| :---: | :---: | :---: |
| Regulator | Adjustment | Potentiometers |
| $8-20 \mathrm{Vdc}$ | Output voltage | R17 |
|  | Output power | R2 |
| +5 Vdc | Output voltage | R13 |
|  | Output current | R7 |




[^0]:    INPUTS: Voltage levels of 0 V and +3 V (typical). All inputs present 1 TTL unit load each.

    OUTPUTS: Voltage levels of 0 V and +3 V (typical). All outputs are capable of driving 10 TTL unit loads.

