

IDENTIFICATION

PRODUCT CODE:	MAINDEC-12-D3GA-D
PRODUCT NAME:	PDP-12 TAPE CONTROL TEST (PART 2 OF 2)
DATE CREATED:	MAY 1, 1970
MAINTAINER:	DIAGNOSTICS GROUP
AUTHOR:	JAMES KELLY

1. ABSTRACT

The tape control diagnostics Part 2 is designed to test all Controller Logic not tested by Part 1. Specifically this includes, Inter-Processor Signals, Tape Control States and Instruction, Tape States, Tape Trap and the Transfer of Data between the Computer and the Tape Controller via the Data break facilities. It should be noted that Part 1 of this diagnostic should have been successfully run prior to running Part 2, because Part 2 assumes that the logic associated with Part 1 is functioning normally.

2. REQUIREMENTS

2.1 Equipment

- 1) A Standard Basic PDP-12
- 2) A TC-12, PDP-12 Linc Tape Controller
- 3) At least 1 Linc-Tape Transport
- 4) An ASR-33 Teletype or Equivalent

2.2 Storage

This program is designed to run in Memory Field 0 only and it occupies virtually all of Field 0 not occupied by the Binary and Rim Loaders.

2.3 Preliminary Programs

All PDP-8 and 12 mode basic instruction diagnostics and exercisers must have been successfully run prior to running the program.

3. LOADING PROCEDURE

3.1 Method

This program must be loaded with the binary loader. If you are unfamiliar with the proper binary loading procedures refer to Appendix A of this document, otherwise procede with the following:

- A) Set the teletype reader switch to FREE.
- B) Open the teletype reader and insert the program tape so that the arrows on the tape are visible to and pointing toward the operator.
- C) Close the reader and set the reader switch to START.
- D) Set the teletype front panel switch to START.
- E) Set the left switches to 7777.
- F) Set the right switches to 4000.
- G) Set the mode switch to 8 mode.
- H) Depress I/O preset.
- I) Depress start LS.
- J) When the program tape has been read in the ACCUMULATOR must be 0000, if it is not, a read-in error has occurred and one might try reloading the binary loader.

See Appendix A.

- K) Remove the program tape from the reader.

4. STARTING PROCEDURES

This preliminary set up procedure is critical and any omission will result in an error.

- A) Set one and only one of the Linc-tape transport number thumbwheels to 0 - on some transports the 0 position is actually represented by 8.
- B) Set all other transports, if available, to all different numbers i.e. no two transports have the same unit number.
- C) No TRANSPORT may be set to unit 1 as this number is used to generate a non-select signal.
- D) Set the WRITE ENABLE switch on every transport to the disabled condition.
- E) Set all transport switches to OFF.
- F) Remove any Linc-tapes currently on the transport.
- G) Set the left switches to 0200.
- H) Set the right switches to 0000.

NOTE: Setting the right switches to configurations other than 0000 will cause the computer to scope loop, halt on error, and perform other options. These options are discussed later.

- I) Set the MODE switch to 8 mode.
- J) Depress I/O preset.
- K) Depress START LS.

The program is running.

4.1

Control Switch Settings

A set of 6 optional mode switches consisting of right switches 0-6 has been included for the convenience of the test engineer, they are:

TAPE MARK
SWITCH DOWN!

SR00 = 1 suppress error halts
 SR01 = 1 suppress type outs ring bell on error
 SR02 = 1 scope loop on a failing test
 SR03 = 1 scope loop on a non-failing test
 SR04 = 1 unit does not have extended tape fields (unused in
 part 2)
 SR05 = 1 suppress the bell
 SR06 = 1 suppress the pass counter.

The switches have an order of precedence associated with them. For example, if the option switches were set so as to cause a typeout and an error halt, it is obvious that the typeout must precede the halt. Right switch 00 if set to a one will prevent the computer from halting when an error is detected. Depending on the condition of the other switches, we may:

- 1) go on to the next test after typing out a message
- 2) stay in the same test.

Right switch 01, if set to a one, will prevent the computer from typing anything out and instead causes a bell to ring at every detected error. The purpose of this is merely to inform the operator that an error has occurred and nothing more.

Right switch 02, if set to a one, will prevent the computer from exiting the current failing test.

Using switches 00, 01, 02 several use full combinations of error analysis present themselves:

SR0	SR1	SR2	Explanation
0	0	0	Type error data and halt
0	1	0	Ring bell and halt
1	0	0	Continuous typing of data with no halt
1	1	0	Ring bell at every failure
1	0	1	Continuous typing of data in current test

In general, an error halt is useful for scoping status of the machine immediately following an error.

Right switch 03, if set to a one, will cause the program to remain in the current test, so long as no failures occur.

Right switch 04, if set to a one, will cause the program not to test the extended tape field register. (4K System)

Right switch 05, if set to a one, will inhibit the bell from ringing. Under normal operation the program will ring the bell about once every 1 and 1/2 minutes.

5. MESSAGE FORMAT

- 1) The message format is designed to yeild the maximum possible information with the minimum amount of typing. To that end the following format has been selected as the best of both worlds; i.e., amount of information vs. the amount of typing.

Example:

LTR AC RWB (VIA TB) Failed

AC RWB

0001 0000

0002 0000

- LTR 2) The first item typed, in this case LTR, refers to the logic page on which the logic which is being tested is drawn. In this case the message tells us that the logic under test is located in the (LTR) Linc Tape Register logic.

It should be understood that the trouble is associated with the Linc tape register logic but not necessarily on the page referenced. For example, on this test the data transfered may not have gotten from the computer to the tape control or it may not have been read back properly. Both of these problems would cause a typeout such as this, indicating a bad register, when in fact, the trouble was in getting data to or from a register.

AC RWB 3) The second items typed AC RWB indicate that the two registers involved, the AC, referring to the computer AC, and the RWB, referring to the tape control read write buffer, are involved in the test.

(VIA TB) 4) The third item, enclosed in brackets, is a modifier.

In this example, the program is capable of loading the RWB in one of three (3) ways, from the tape transport, from the AC serially via a maintenance gate, and from the AC via the TB. Obviously three different trouble shooting techniques are required depending on which of the three data paths are bad. The modifier in this case points out which one of three data paths failed.

FAILED 5) The word "failed" is typed to be sure the operator understands that this message indicates trouble and is not interpreted as a status report.

AC RWB 6) The two registers whose data are shown are named on the second line of the typeout to ensure that the operator is aware that the data type out is AC and RWB and not the TB. Usually the registers involved do not have their names typed out unless there is a possibility of confusion.

0001 0000 7) The numerical data type outs also in a special format.

When more than one number is typed the first number is always the source number. In this typeout the 0001 is the number in the AC after the contents of the RWB were read back into the AC. An engineer must always refer to this document and locate the exact type in order to properly interpret any message or data typeout.

6. MONITORS

This program contains two monitors, an error monitor and a non-error monitor. The error monitor handles scope looping on errors, message typeouts, and determines what data shall be used in a failing test. The non-error monitor is an extremely simple subroutine whose only function is to allow a test to loop continuously even when no error exists. The following example will be used to illustrate a typical coding sequence, involving the comparing of a true number with the actual results of an operation.

1)	TESTX,	TAD	REGB	/Fetch Received data
2)		CIA		/Negate
3)		TAD	REGA	/Subtract from sent number
4)		SNA	CIA	/Were they equal
5)		JMS	I NERROR	/AC was zero, they were equal
6)		JMS	I ERROR	/Sent Data Received data unequal
7)		GOOF		/Message TAG
8)		HLT		/Error HALT
9)		SKP CIA		/EXIT
10)		TESTX		/Scope Loop Pointer

The numbers shown in the left margin are for reference purposes only and are not part of the coding.

The first three lines performed in order (1) fetch the resultant of the test from "REGB". This could have been any memory register or any hardware register which can be read under computer control. The test data is converted to twos' complement form (2) and subtracted from the correct results (3) The test of the data (i.e. were they equal) takes place on line (4) and based on this test we go either to the non-error (NERROR) subroutine or if the ACCUMULATOR is not zero the error (ERROR) monitor. It should be obvious that any decision making instruction can be used to ascertain which monitor we hand control too.

Lines (5), (6), are the actual monitor calling instructions. Line (7) (GOOF) is the address of the first memory location of the error message which will be typed out in case of a failure. Line (8) is an error halt. If an error should occur and the switches are set so as to allow an error halt this address will be the one at which it will halt.

Line (9) is an exit. If an error halt occurs, pressing continue will cause the computer to execute the skip and exit to the next test.

Line (10) contains the address at which this test is begun again. For example, after completing one pass thru this test routine the monitors will execute an effective Jump Indirect the contents of line (10) and redo this test routine.

6.1 Non Error Monitor

The non error monitor has two functions. The first is to increment "REGA". "REGA" is a common tally register used to count 4096 passes thru a test and to notify the non-error monitor via an "ISZ" loop when the required number of passes have been performed and thereby causing an exit. The second function is to examine RSW 03 and if set, inhibit exiting to the next test.

In some tests, particularly those associated with time delays, or mechanical delays it becomes prohibitive to make 4096 passes thru a test. To circumvent this it is possible to preset "REGA" to "7777" so as to only make a single pass thru a test, or any number of passes from 1 through 4096.

6.2 Error Monitor

The error monitor is the major monitor responsible for all modes of communicating errors to the operator. The usage of switch inputs has been completely discussed under part 4.1 control switch settings and will not be discussed here. Several salient features of the error monitor are as follows. The first "scope loop on failing test" (SR02=1), is designed to cause the monitor to inhibit incrementation of "REGA", and to inhibit the advance of the random number generator. An example of its use might be in testing any of the 12 bit registers. Assume that bit 00 can never be set to a one because of some as yet unknown hardware error. This malfunction will become known the first time the number 4000 is loaded into it because the read back will show 0000 - normally the next number to be tried will be 4001, 4002 etc. with each being typed out and each causing

different data to be transferred. To facilitate scope testing of this problem, we must eliminate type outs and prevent the data from changing. This is easily accomplished as explained under switch settings.

An error message is always formatted such that all of the non numeric characters are typed out first followed by the numerics. The contents of some memory register, other than those selected by the programmer, may be of interest to the field engineer. For example, in a random data transfer test it is impossible to determine the number of successful data transfers, because only the errors are typed out. Lets presume that the engineer wishes to type out the pass counter i.e. "REGA" memory address 0004. It is necessary to modify the message type out string as follows:

BEFORE	AFTER
GOOF, 0001 0001	GOOF, 0001 0001
0203 0203	0203 0203
EXITA 7777	EXITA 7777
REGB 0005	REGB 0005
REGC 0006	REGC 0006
EXIT 0000	REGA 0004
	EXIT 0000

The following shows the before and after type out.

ABC 7351 7350 ABC 6773 6253 0037

The type out on the right shows the contents of the pass counter and will indicate if all random numbers failed or if only some of them failed. It is absolutely necessary to restore the

toggled in modifications to the message type out in order to prevent erroneous type outs in other messages.

7. MAINTENANCE INSTRUCTION SET

MNEMONIC	CODE	MODE	OPERATION
LMR	6151	PDP-8	Load maintenance register
AC			
0	TO MAINT INST REG		
1	TO MAINT INST REG		
2	TO MAINT INST REG		
3	TO MAINT INST REG		
4	CLEAR TAPE DONE FLOP		
5	SKIP ON TAPE DONE		
6	GENERATE A SIMULATED TT0, TT1, TT2, PULSES		
7	GENERATE A SIMULATED TT3, TT4, PULSES		
8	SIMULATE MARK INPUT		
9	SIMULATE DATA 1 INPUT		
10	SIMULATE DATA 2 INPUT		
11	SIMULATE DATA 3 INPUT		

Bits 0,1,2,3

The contents of ACCUMULATOR bits 0, 1, 2, 3, are loaded as a command into the maintenance instruction register. The command will be executed if and only if the XFR IOT (6154) is generated; the function of these commands are discussed later.

Bit 4

Executing the LMR command with 'AC bit 4 set will unconditionally clear the tape done flag.

Bit 5

Executing the LMR command with AC bit 5 set will cause the computer to skip the next instruction in sequence if the tape done flip-flop were set.

Example:	CLA CLL	/Clear AC, L
	TAD K0100	/Set Bit 5
	LMR	/IOT 6151
	HLT	/Tape done was zero
	HLT	/Tape done was one

It should be noted that these commands are not designed to be microprogrammed; for example, setting both Bit 4 and 5 and executing LMR in an attempt to SKIP and clear on the tape done flag is unwise.

Bit 6

Executing the LMR command with AC bit 6 set will generate in order the timing pulses TT0, TT1, TT2 regardless of the state of the tape control logic.

Bit 7

Executing the instruction LMR with bit 7 set will generate in order TT3 and TT4. It should be noted that to generate an entire timing stream consisting of pulses TT0, TT1, TT2, TT3, and TT4, it is necessary to generate TT0, TT1, and TT2 first followed by a second command to generate TT3 and TT4.

Bit 8

Is used to simulate an input to the mark window, see bits 9, 10, 11 below.

Bits 9, 10, 11

Executing the instruction LMR with data in AC bits 9, 10, 11 will simulate reading data of the data heads into the Read-write buffer. This feature is useful in testing the tape control without a transport.

TRC 6152

PDP-8

Tape Register Clock

AC

0	Generate tape preset
1	Shift RWB once left with no end around carry
2	Transfer TB to RWB
3	Add TB and TAC place the results in TAC
4	0 Tape word flip flop
5	Set Forward
6	Set unit 1
7	Set Backward
8	Set write sync flip flop
9	Set 8 mode tape motion
10	Select 8 tape mode
11	AC11 LTP8 Write if AC10 is set

The tape register control command TRC (6152) in conjunction with selected bits in the AC can perform a number of direct non-conditional operations. Several of the commands are useful primarily for logic testing the rest although they are tested, are used in normal machine operation.

Bit 0:

Executing the command tape register control TMR (6152) in conjunction with AC bit 0 set to a one generates the internal signal tape preset. Tape preset, in general, sets all control flops to a null state, which may be either a one or a zero.

Bit 1:

TMR in conjunction with AC bit 1 will cause the Read-write buffer (RWB) to be shifted once to the left, observing it from the computer accumulator, or once up on the logic drawings. Data shifted out of RWB is lost and a logic 0 is shifted into the low order bit.

Bit 2:

TMR in conjunction with AC Bit 2 will cause the contents of the TB to be copied into the RWB. The previous contents of the RWB are lost, the TB remains unchanged. It should be noted that the only path by which the RWB may be loaded in parallel is via the TB register.

Bit 3:

AC bit 3 causes the contents of the TB register to be added to the contents of the TAC register, with the resultant being retained in the TAC.

Example:

BEFORE	AFTER
TB = 7321	TB = 7321
TAC = 0412	TAC = 773

Bit 4:

Clear the tape word flip flop. This bit generates an unconditional clear.

Bit 5:

Set forward. The direction flip flop is set to a one unconditionally. This command is useful for diagnostics.

Bit 6:

Set unit 1. When executed this command will select tape transport unit 1. It should be noted that this command can only select unit 1, if the extended transport select register (part of extended operations register bits 10, 11) are set to a zero. If the extended transport select register is not zero, the appropriate odd numbered unit is selected.

Bit 7:

Set Backward. The direction flip flop is set to zero unconditionally. This command is useful for diagnostics.

Bit 8:

Set write sync. This command unconditionally sets the write sync flip flop.

Bit 9:

Set 8 tape motion is used with the TC12-F option. This option allows the reading and writing of tapes written in PDP-8 Linc tape format.

Bit 10:

Set 8 write selects 8 tape mode.

Bit 11:

Set LTP8 write, AC bit 11 is provided as a data input to the 8 tape write flip-flop. If AC bit 10 is set, the bit is clocked into the flop.

XFR 6154 PDP-8 Transfer

Maintenance register

00	AC to TB
01	AC to TBN
10	AC to TAC
11	AC to TMA
20	TMA setup to AC
21	TBN to AC
30	TB to AC
31	RWB to AC
40	Mark window to AC
41	States to AC
50	Units and motion to AC
51	Tape instruction register to AC
60	Misc status 1 to AC
61	Misc status 2 to AC
70	TMA to AC
71	Unused, returns all zeros to AC

In general all data transfers into the AC using maintenance commands are 1's transfers, that is, they do not clear the AC prior to inserting data. All data transfers from the AC into tape control register are jam transfers. Any data which was in a tape control register is lost.

00 AC to TB

The current contents of the AC are transferred into the TB (Tape Buffer). The AC data is unaffected the previous contents of the TB are lost.

01 AC to TBN

The current contents of the AC are transferred into the TBN (Tape Block Number). The AC is unaffected, the previous contents of the TBN are lost.

10 AC to TAC

The current contents of the AC are transferred into the TAC (Tape Accumulator). The AC is unaffected, the previous contents of the TAC are lost.

11 AC to TMA

The contents of the AC are transferred into the TMA (Tape Memory Address). The AC is unaffected the previous contents of the TMA are lost.

20 TMA setup to AC

The contents of the TMA setup register is "ORED" into the AC. The contents of the TMA setup register is unaffected.

21 TBN to AC

The contents of the TBN register is "ORED" into the AC. The contents of the TBN are unaffected.

30 TB to AC

The contents of the TB register is "ORED" into the AC. The contents of the TB is unaffected.

31 RWB to AC

The contents of the RWB (Read write buffer) is "ORED" into the AC. The contents of the RWB are unaffected.

40 Mark Window to AC

The contents of the tape mark window and its associated mark decoding gates are "ORED" into the AC. The contents of the Mark window register is unaffected. The data format is as follows:

AC

00	Window shade
01	Window 00
02	Window 01
03	Window 02
04	Window 03
05	End Zone mark
06	Check mark
07	Guard mark
08	Data mark
09	Final mark
10	Block mark
11	Intermediate zone mark

41 States to AC

The contents of several flops and the levels of several gates are "ORED" into the AC. Reading the data does not affect its state. The data format is shown below:

AC

00 TAC = 7777
 01 IDLE Mode = 1
 02 Search mode = 1
 03 Block Mode = 1
 04 Check word mode = 1
 05 Turn around mode = 1
 06 Write flop = 1
 07 Write cycle flop = 1
 08 Acip delay not timed out
 09 Tape timing OK
 10 Timing OK gate set
 11 Tape fail delay

50 Units + MTN to AC

The data concerning transport selection, motion, direction, unit select, and write enable is "ORED" into the AC.

AC

00	UNIT 0	Selected
01	UNIT 1	Selected
02	UNIT 2	Selected
03	UNIT 3	Selected
04	UNIT 4	Selected
05	UNIT 5	Selected

06	UNIT 6	Selected
07	UNIT 7	Selected
08	MOTION FLOP	(1)
09	DIRECTION FLOP	(1)
10	UNIT SELECT	
11	WRITE ENABLE	

Bit 10 Unit Select

This bit indicates that one and only one unit is selected at a time.

51 TINST to AC

The contents of the tape instructions register decoder, the I bit and the group register are transferred to the AC. The contents of these datum are unaffected; however, the previous contents of the AC are lost.

AC

00	RDC
01	RCG
02	RDE
03	MTB
04	WRC
05	WRE
06	WRI
07	CHK
08	I BIT
09	GP0 (1)
10	GP 1 (1)
11	GP 2 (1)

60 Misc Status 1 to AC

This command transfers the status of several important levels to the AC. The format is shown below:

AC

00	PHASE GATE
01	PROGRESS FLOP (1)
02	LC 00 (1) Line Counter
03	LC 01 (1) Line Counter
04	MARK CHANNEL WRITE
05	DATA CHANNEL 1
06	DATA CHANNEL 2
07	DATA CHANNEL 3
08	GP CNT = GP FLOP
09	GP CNT 0 (1)
10	GP CNT 1 (1)
11	GP CNT 2 (1)

61 Misc Status 2 to AC

Bit 0 of the AC is set to a one if the LTP8 tape select flip-flop is set.

70 TMA to AC

The contents of the TMA register is transferred to the AC. The contents of the TMA are unchanged, the original contents of the AC is lost.

71 Unused

General Information

This program will test the PDP-12 tape control logic on a gate by gate basis. This was made possible by including a 16 instruction maintenance register in the basic desing. The linc tape maintenance register (LTMR) facilitates examination of all major registers and the majority of status bits, control levels etc., associated with the tape control. It is usually possible to isolate the fault to no more than one or two modules by analizing the diagnostic type out and referring to the appropriate logic diagram.

This program is written in several major and minor sections designed to point to a failure on an appropriate page in the logic drawings. The four major sections in order are:

- 1) Test out, in so far as possible, the maintenance logic. This includes the maintenance mode flop, maintenance instruction register, tape preset and the tape buffer to computer accumulator (TB to AC) data read back portion. This group of tests are a necessary preliminary diagnosis in order to be reasonably certain that the following tests fail because of logic failures and not because of failures in the maintenance instruction register
- 2) Test out the 12 bit registers TAC, TB, TMA, TMA setup, RWB and TBN. Two tests are performed on each register; the first test is a binary up count sequence; the second a random number sequence. The binary sequence ascertains that all flops can be both set to a one and set to a zero. In addition it also proves mutual independence of the data paths i.e. the flops can move independently of one another and the input and output data paths

are not shorted in any way. The random number test causes each bit of the registers to toggle at a relatively high speed, in contrast to the binary sequence wherein only the low order bits toggle at high speed. A second useful effect of the random number sequence is that it leaves the tested register in a random state, a technique sometimes useful for discovering grossly illogical wiring errors.

3) Test all minor registers; i.e., registers with less than 12 bits. These include unit select registers, mark window, extended positions register, etc. In this series of tests an attempt is made to diagnose all flops and all sequenceable flops such as the major state generator. In most cases random number tests are not performed due to the fact that an unknown state in any control flop might have an adverse affect on the succeeding tests.

4) Test all gates using as many as possible input combinations. For example, AND gates are first tested with all inputs true to determine if the gate will function. Next each individual input is set false in turn to see if each input is expressed in the output. OR gates are tested by allowing at least one input and maybe more to become true and monitoring the output for a true condition. This is followed by setting all inputs to false monitoring the output for false, followed by setting each input in turn to true and checking the output.

A significant number of gates in the tape control can not be directly tested tape state logic TC12-Ø-LTS, for example. These untestable gates are evaluated indirectly by logical deduction; i.e., all testable inputs to these gates are tested as inputs to other gates. An example:

Block mark (BM) is a functional input to the LTS logic. As previously stated it is extremely difficult to prove that a correct (BM) appears at the LTS logic, however, it is each to prove that a correct (BM) signal itself is functional, that other gates using the (BM) signal function, and that the (BM) signal is not shorted, either to logical low or logical high. The technique used to circumvent the apparent difficulty in testing multilevel logic is as follows:

- a) Attempt to set all inputs to a group of logic to a state which will cause a true output at some software observable point.
- b) Attempt to disqualify the output by causing one input at a time to change to a state which will cause the output to become false.
- c) In many cases a gate will be qualified or disqualified, as the case may be for a specific period of time regardless of what the diagnostic program does. An example of this is any gate whose inputs are a function of tape delays.

The following four (4) error messages are associated with tests of the: TAPE DONE FLOP

LIP TAPE DONE FAILED TO SET

The LIP TAPE DONE M216 C31 flip-flop failed to set. The tape done flop is set by toggling the progress flop from a 1 to a 0. This test is accomplished by setting progress via MTP Setup, clearing progress via MTB, BM, ACIP-NOT and TP2, and testing the TAPE DONE flop via the TAPE SKIP Maintenance Instruction.

LIP MTP SETUP FAILED TO CLEAR TAPE DONE

The signal, MTP SETUP, failed to clear the Tape done flop. The tape done flip-flop was set as discussed above, and cleared via direct clear input, by MTP SETUP. The results are checked via the TAPE SKIP Maintenance Instruction.

LIP TAPE PRESET FAILED TO CLEAR TAPE DONE

The signal, TAPE PRESET, failed to clear the tape done flop. The tape done flip-flop was set as discussed above, and cleared via direct clear input, by TAPE PRESET. The results are checked via the TAPE SKIP Maintenance Instruction.

LIP CLEAR TAPE DONE FAILED

The signal, CLEAR TAPE DONE, failed to clear the tape done flop. The tape done flip-flop was set as discussed above, and cleared via direct clear input, by CLEAR TAPE DONE. The results are checked via the TAPE SKIP Maintenance Instruction.

The following three (3) messages are associated with the Linc mode command STD, STD i and Tape interrupt.

LIP STD FAILED TAPE DONE = 1

The Linc mode command STD (0416) failed to SKIP or STD i (0436) skipped in error when the TAPE DONE flop was on a 1.

LIP STD FAILED TAPE DONE = 0

The Linc mode command STD (0436) failed to skip when the TAPE DONE flop was on a 0.

LIP TAPE INTERRUPT FAILED INT ENB = 1

The tape processor failed to cause a tape interrupt. The TAPE DONE flop and the INTERRUPT ENABLE flop in the extended operations register were both set to a 1.

The following eight (8) messages are associated with tests of the PROGRESS and IN-PROGRESS flops. Specifically whether MTP SETUP sets the flops and that the clock input gating will zero the flops.

LIP MTP SETUP FAILED TO SET IN-PROGRESS

A non-paused tape instruction was executed to set the IN-PROGRESS M216, D19 flop. The resulting state of the flop is checked by reading it back into the AC, bit 01 via a Misc status 1 to AC Maintenance Instruction.

LIP TAPE PRESET FAILED TO 0 IN-PROGRESS

The IN-PROGRESS flop was set via a non-paused tape instruction then cleared via a TPAE PRESET. The resulting state of the flop is check by reading it back into the AC, bit 01 via a Misc status 1 to AC Maintenance Instruction.

LIP LCS (MTB * BM * SEARCH) FAILED TO 0 IN-PROGRESS

The IN-PROGRESS flop was set via a non-paused MTB tape instruction. The Mark window was loaded to BM (16) and a simulated TP1 pulse was generated to set search mode. The transition from IDLE mode to SEARCH mode.

LIP M115 C25 PIN S2 FAILED TO 0 IN-PROGRESS

The IN-PROGRESS flop was set by a MTP SETUP and an attempt was made to clear it via END INST signal which is generated by gate M115, C25, PINS N2, P2, R2 and S2.

LIP END INST FAILED TO Ø PROGRESS

The progress flop was set by a MTP SETUP and an attempt was made to clear it via END inst signal generated as discussed in the previous type out.

LIP CHK OK FAILED TO Ø PROGRESS

The progress flop was set by a MTP SETUP and an attempt was made to clear it via CHK OK generated by M119 C22 PIN P2. The resulting state of the progress flop is detected by examining the TAPE DONE flop to see if the transition of progress to a zero did in fact set TAPE DONE.

LIP M113, C16, H1 WRITE CYCLE (Ø) FAILED TO Ø IN PROGRESS

This test as in the previous test ascertains if the signal LIP CHK OK can in fact Ø the in progress flip-flop. In this case the input to gate M113 C16 PIN J1 is disabled i.e. LIN TINR 9 (1) and LCS write cycle (Ø) PIN H1 is true.

LIP STW FAILED TAPE WORD = 1

The tape word flip-flop is tested by the Linc command STW (457) and STW I (477). The tape done flop is kept in the one state during this test.

LIP STW FAILED TAPE WORD = Ø

The tape word flip-flop is tested by the LINC command STW (457) and STW I (477). The tape done flop is kept in the zero state during this test.

LIP TAPE WORD TOGGLES FAILED

The Tape Word flop failed to toggle as the result of the action of line counters LC01, LC00 on the clock and data inputs.

LIP DATA BREAK FAILED

0176 0000 0000

The DATA BREAK facility has failed. The first number typed is the address in memory which was referenced by the tape control this is always address 0176. It was necessary to use a fixed address rather than all addresses because almost any error in data break will wipe out the controlling program. The second number typed is the data which was transferred from the tape control to the computer. The last number is the actual number received.

LCX MARK FLOP

0000 0000

An attempt was made to set the mark flip-flop. The first number typed indicates the data sent to the extended operations register this number is either 0000 or 0200. The second number typed indicates the status of the mark flop as read back from the extended operations register this number also is either 0000 or 0200. This error may also indicate that the operator failed to set the mark key.

LCX MARK FLOP TAPE PRESET FAILED

0000

The mark flip-flop was set. An attempt was made to clear it via a tape preset pulse.

LIN TAC=7777, DIR = REV FAILED

The program attempted to set the tape control major state generator to the Block state. In order to go from Idle to search to block, it is necessary for the TAC register to equal 7777 and the direction to be forward. In this case we have purposely set the direction flop to a reverse condition so that the major state generator should be inhibited from going from search to block.

LIN TAC = 0000 DIR = FWD FAILED

Same as the previous test except that we are testing to see if TAC not equal to 7777 will inhibit going to the Block state.

LIT MARK CLOCK FAILED TO GENERATE TP3

An attempt was made to see if the mark clock can generate computer timing. The LC01 Line counter is on a zero, the mark window is set at a Block mark, and sufficient time is allowed for the mark clock to generate TP3, TP4 to set LC01. This test will fail if the mark key is not set.

LCS IDLE SEARCH FAILED

An attempt was made to change the major state generator transfer from idle to search.

LCS SEARCH BLOCK FAILED

The major state generator is initially set to Idle. A routine is executed to set the generator first to search then to block. The primary test is from search to block, because the Idle to search has already been tested.

LCS SEARCH TURN AROUND FAILED

An attempt was made to go from the Idle to the search, to the turn around major state.

LCS TURN AROUND IDLE FAILED

The major state generator was set to the turn around state as in the previous test. An attempt to go from turn around to IDLE was made. The gate M115 A32 PIN H2 was used to generate the timing to cause the transition to the IDLE state.

LCS BLOCK CHK WRD FAILED

The major state generator was set to block mode in a manner similar to the search Block Test previously discussed and attempt was made to go from Block to CHK WRD Mode.

LCS CHK WRD IDLE FAILED

The major state generator was set to CHK WRD mode and attempt was made to Idle mode via gate M16Ø, B29, PIN V2.

LCS SEARCH IDLE (MTB+I) FAILED

The major state generator was set to search mode with the (I) bit set. This test tries to set idle mode using LIN I (1) and LCS MTP END at gate M16Ø, B29 PINS V1, U2 and V2.

LRL; LRE; EN TAC, EN TB, OR LOAD TAC

This type out indicates an error in the function TB+TAC to TAC. The adders and this function have previously been tested using the maintenance logic in tape control test PART 1. We can therefore presume that the trouble only occurs when the controller performs under its own control. The four (4) names typed out indicate the suspected logic. The three (3) numbers typed out indicate in order the contents of the TB, TAC and TAC after the addition has been performed.

LTS PHASE GATE FAILED

Each of the two gates which generate the PHASE signal are tested individually first with both inputs false then with each input set true in turn. The two inputs consist of CHK WRD and LCØ2.

LWN MARK WRITE GATE FAILED

The mark write test is similar in principle to the phase gate test above.

LTR DATA CHANNEL RWB 0, 4, 8 FAILED

4210 0160

The Data channel output from the RWB was tested and failed. Bits 0, 4, 8 of the RWB are alternately set to all ones then all zeros. The first number typed out shows bits 0, 4, 8, set to ones. The second number shows them as they are read back via the data channel on bits 5, 6, 7.

LTT MARK CLOCK FAILED TO GENERATE TP0

The timing logic is tested to ascertain if the mark clock can generate TP0, TP1, TP2. The results are detected by determining if TP2 will set the GP=GPC flip-flop.

LTS LINE COUNTER FAILED TO COUNT

0000

The 3 Line counter flops were set to all ones an attempt was made to ripple a carry thru it i.e. set is to all zeros. The number printed in bits 02, 03 indicate the value of LC00, and LC01.

LMU TURN AROUND BM FAILED TO 0 MOTION

The motion flip-flop was set via a Linc tape instruction. The major state generator was set to turn around the window to block mark and time pulses 0, 1, 2 were used to try to clear the motion flop.

LMU TAPE PRESET FAILED TO Ø MOTION

The motion flip-flop was set as discussed above. An attempt was made to clear it by generating a tape preset.

LMU CLR PROGRESS FAILED TO Ø MOTION

The tape flop was set an attempt was made to clear it using CLR progress. CLR is made up of MTB, I (Ø) and BM

LRR TP3 FAILED TO SHIFT RWB

ØØØØ ØØØØ

The RWB was set to the value of the first number typed. A TP3 pulse was used to shift RWB. The second number is the resulting value of the RWB. It should be noted that the shift logic i.e. the logic which handles the data which is being shifted has previously been tested. So a failure will be indicated by no shifting rather than bad data.

LRL EN WRITE LD RWB FAILED TO SHIFT RWB

ØØØØ ØØØØ

A test of the RWB shift logic has failed. The two numbers indicate the before and after contents of the RWB.

LRL TB+TAC=TAC FAILED

ØØØØ ØØØØ ØØØØ ØØØØ

The add function of the Tape processor is tested. The numbers typed are in order TAC, TB RESULTANT and the resultant as computed by the central processor.

LRL LOAD TAC FAILED TP3, SEARCH

0000

The TAC register was set to 7777. The major state generator was set to search. TP3 was used to try to clear TAC ie. generate. LOAD TAC with no data on the BUSS. The number typed out indicates taht data which was left in the TAC after the transfer.

LCS WRITE CYCLE FLOP TEST FAILED

The write cycle flop was both set and cleared with the result read back and tested after each change.

LTS TIMING OK GATE FAILED

The timing OK gate failed to indicate that all machine timing was OK after the program had set all inputs to the timing OK gate to true.

TMA failed to increment during tape break

was is

A tape break was executed; at the completion of the break cycle, the TMA was not equal to the previous address plus one.

TC12-Part 2 Pass--(PASS)

The octal number indicates the number of completed passes executed since the last "Start 20".

1
2 /PDP-12 TAPE CONTROL TEST PART II, MAINDEC 12-03GA-L
3 /COPYRIGHT 1970, DIGITAL EQUIPMENT CORP., MAYNARD, MASS.
4 /

5 /AUTHOR: JAMES KELLY
6 /

7 /THIS PROGRAM, OPERATING IN BOTH 8 AND LINC MODE,
8 /IS DESIGNED TO COMPLETE CHECKOUT OF THE PDP-12
9 /TAPE CONTROL LOGIC. TAPE CONTROL TEST PART I
10 /MUST RUN SUCCESSFULLY PRIOR TO EXECUTION OF PART II
11 /THIS PORTION.
12 /

13 /SPECIAL INSTRUCTIONS:

14 / 1. REMOVE LINC TAPES FROM ALL DRIVES
15 / 2. SET TRANSPORT THUMBWHEELS TO "OFF LINE"
16 / 3. SET TRANSPORT SELECT SWITCHES TO "OFF"
17 / 4. DEPRESS AND HOLD THE MARK KEY
18 / 5. I/O PRESET TO 8 MODE
19 / 6. DEPRESS START 20,
20 /

21 /THE TEST IS CONTROLLED BY A MONITOR RESIDENT
22 /IN PAGE 24. OPTIONAL SETTINGS ARE AVAILABLE
23 /FOR MODIFICATION OF ERROR CONTROL.
24 /

25 /SWITCH SETTINGS: (NORMALLY 0000)

26 /
27 /RSW00=1, INHIBIT ERROR HALT.
28 /RSW01=1, INHIBIT ERROR TIMEOUT.
29 /RSW02=1, SCOPE LOOP ON ERROR.
30 /RSW03=1, SCOPE LOOP ON NONERROR.
31 /RSW05=1, INHIBIT BELL.
32 /RSW06=1, INHIBIT PASS COUNTER TIMEOUT.
33 /

34 /AT THE COMPLETION OF A PASS, THE CONTENTS
35 /OF THE PASS COUNTER WILL BE TYPED OUT.
36 /
37 /

```
38
39      0001      *1
40      0001 5402      JMP I   RETURN
41      0002 0000      RETURN, 0000
42      0003 4000      K4000, 4000
43      0004 3400      K3400, 3400
44      0005 0250      K0250, 0250
45      0006 7400      K7400, 7400
46      0007 0017      K0017, 0017
47
48      /COMMAND IDENTIFICATION
49      /
50      6141      LINC=0141
51      0000      EXIT=0000
52      7777      EXITA=7777
53      0002      PDP=0002
54      6151      LMR=6151
55      6152      TRC=6152
56      6154      XFR=6154
57      0416      STD=0416
58      0017      COM=0017
59      0001      AXO=0001
60      0457      STW=0457
61      0003      TAC=0003
62
63      0011      CLR=0011
64      0021      XQA=0021
65      0004      ESF=0004
```

```

66
67      0010 0010 *10
68      0010 0000 PINT, 0000
69      0020 0020 *20
70      0020 7300 CLA CLL /START 20
71      0021 3065 DCA PASS
72      0022 5423 JMP I ,+1
73      0023 0177 0177 /THIS LOCATION MAY POINT TO ANY TEST
74      0024 0000 LSTERR, 0000 /THE OPERATOR DESIRES
75      0025 0000 TPEPRE, 0000
76      0026 7330 CLA CLL CHL RAR
77      0027 6152 TRC TAPE PRESET
78      0030 7200 CLA
79      0031 5425 JMP I TPEPRE
80      0032 3134 MAINT1, MAINT2
81      0033 0016 K0016, 0016
82      0034 3144 LOADR, LOADS
83      0035 0040 K0040, 0040
84      0036 5000 NERROR, NERROS
85      0037 5021 ERROR, ERRORS
86      0040 0002 K0002, 0002
87      0041 0160 K0160, 0160
88      0042 4210 K4210, 4210
89      0043 5000 K5000, 5000
90      0044 3040 K3040, 3040
91      0045 5216 RAN, RANDOM
92      0046 0000 REGE, 0000
93      0047 7000 K7000, 7000
94      0050 7030 K7030, 7030
95      0051 7777 K7777, 7777
96      0052 3334 M4444, -4444
97      0053 4140 K4140, 4140
98      0054 7770 K7770, 7770
99      0055 0100 K0100, 0100
100     0056 0200 K0200, 0200
101     0057 0150 K0150, 0150
102     0060 0450 PNTA, LOCA
103     0061 3027 PNTB, WRCFLB
104     0062 1302 PNTC, LOCC
105     0063 3133 PNTJ, LOCU
106     0064 5054 OUTPAS, ASCII
107     0065 0000 PASS, 0000
108     0066 2000 K2000, 2000
109     0067 6040 K6040, 6040
110     0070 6000 K6000, 6000
111     0071 1000 K1000, 1000
112     0072 0400 K0400, 0400
113     0073 0077 K0077, 0077
114     0074 7740 M40, -40

```

115					
116	0075	0240	K240,	240	
117	0076	7774	K7774,	7774	
118	0077	1026	K1026,	1026	
119	0100	0215	K0215,	0215	
120	0101	0212	K0212,	0212	
121	0102	0177	K0177,	0177	
122	0103	5200	BELLA,	BELL	
123	0104	0207	K0207,	0207	
124	0105	5210	TYPE,	TYP0UT	
125	0106	0000	SPACE,	0000	
126	0107	0050	K0050,	0050	
127	0110	0020	K0020,	0020	
128	0111	7773	K7773,	7773	
129	0112	0010	K0010,	0010	
130	0113	0000	TEMPB,	0000	
131	0114	0000	REGD,	0000	
132	0115	0000	REGA,	0000	
133	0116	0000	REGB,	0000	
134	0117	0000	REGC,	0000	
135	0120	0000	REGF,	0000	
136	0121	0376	LIA004,	L18004	
137	0122	4440	K4440,	4440	
138	0123	3700	K3700,	3700	
139	0124	7400	M0400,	-0400	
140	0125	7000	M1000,	-1000	
141					
142	0126	0000	DELAY,	0000	
143	0127	1162	TAD	K7737	/GET TALLY
144	0130	3025	DCA	TPEPRE	/SET TALLY
145	0131	3024	DCA	LSTERR	/0 LAST ERROR
146	0132	2024	ISZ	LSTERR	/WAIT
147	0133	5132	JMP	,=1	
148	0134	2025	ISZ	TPEPRE	/WAIT
149	0135	5133	JMP	,=2	
150	0136	5526	JMP I	DELAY	/WAIT FOR ACIP TO TIME OUT
151	0137	0177	K177,	177	

152	0140	*140	
153	0140	7777	7777
154	0141	0002	PDP
155	0142	5543	JMP I ,+1
156	0143	3105	LOCTRP
157	0144	0050	C0050, 0050
158	0145	1400	K1400, 1400
159	0146	0013	K0013, 0013
160	0147	3000	K3000, 3000
161	0150	7700	M0100, -0100
162	0151	6000	M2000, -2000
163	0152	7600	M0200, -0200
164	0153	0011	K0011, 0011
165	0154	3440	K3440, 3440
166	0155	6020	K6020, 6020
167	0156	0007	K0007, 0007
168	0157	7040	K7040, 7040
169	0160	0012	K0012, 0012
170	0161	3020	K3020, 3020
171	0162	7737	K7737, 7737
172	0163	0003	K0003, 0003
173	0164	3420	K3420, 3420
174	0165	3427	K3427, 3427
175	0166	0001	RNA, 0001
176	0167	0000	RNB, 0000
177	0170	0176	C0176, 0176
178	0171	7356	K7356, 7356
179	0172	2224	LWA104, LWB104

/P MODE
/EXIT

```

180
181      0176      *176
182
183      0176      7777      LOC176, 7777      /TEST ADDRESS FOR DATA BREAKS
184      0177      4434      JMS I      LOADR      /SET REVERSE
185      0200      4503      JMS I      BELLA      /RING BELL
186      0201      4126      JMS      DELAY      /WAIT FOR ACIP
187
188      /
189      /TC12-0-LIP INTERPROCESSOR SIGNALS
190      /SKIP ON TAPE DONE TEST #113 C29 PIN U1 PULSES TO LOW
191      /THE NEXT 17 TESTS DIAGNOSE THE TAPE DONE LOGIC
192      /
193      0202      4025      LIP000, JMS      TPEPRE      /0>PROGRESS, 0>TAPE DONE
194      0203      1071      TAD      K1000      /GET AC > TAC
195      0204      6151      LMR      /LOAD MAINT REG
196      0205      7330      CLA CLL CML RAR      /SET AC00
197      0206      6154      XFR      /SET TAC00
198      0207      4432      JMS I      MAINT1      /SET MAINT MODE
199      0210      6141      LINC      /L MODE
200      0211      0713      0713      /MTB
201      0212      7000      7000      /NO PAUSE FAILED TO SET.
202      0213      0002      POP      /P MODE SET PROGRESS
203      0214      1033      TAD      K0016      /GET BM
204      0215      4434      JMS I      LOADR      /SET MARK WINDOW TO BLOCK MARK
205      0216      1035      TAD      K0040      /GENERATE TP2
206      0217      6151      LMR      /TP2
207      0220      7104      RAL CLL      /SET AC BIT 05
208      0221      6151      LMR      /TRY TO SKIP
209      0222      7610      SKP CLA      /INVERT SENSE OF SKIP
210      0223      4436      JMS I      NERROR      /IT SKIPPED GOOD
211      0224      4437      JMS I      ERROR      /NO GOOD
212      0225      6006      LIM000      /MESSAGE TAG
213      0226      7402      HLT      /ERROR HALT
214      0227      7610      SKP CLA      /EXIT
215      0230      0202      LIP000      /SCOPE LOOP

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216
217
218      /DOES MTP SETUP CLEAR TAPE DONE M113,B16,L1,M1,N1
219      /
220      LIP001, JMS      TPEPRE      /0>PROGRESS, 0>TAPE DONE
221      TAD      K1000      /GET AC > TAC
222      LMR      /LOAD MAINT REG
223      CLA CML CLL RAR      /SET AC00 (1)
224      XFR      /SET TAC00
225      JMS I     MAINT1      /SET MAINT MODE
226      LINC      /L MODE
227      0713      /MTB
228      7000      /WASTED MEMORY
229      PDP      /P MODE
230      TAD      K0016      /GET BM
231      JMS I     LOADR      /SET MARK WINDOW TO BLOCK
232      TAD      K0040      /GENERATE TPR
233      LMR      /LOAD MAINTENANCE REGISTER
234      CLA CLL      /CLEAR AC,L
235      LINC      /L MODE
236      0703      /DOES MTP SETUP 0 TAPE DONE
237      7000      /TAPE AREA
238      PDP      /P MODE
239      TAD      K0100      /SET AC05
240      LMR      /SKIP ON ERROR
241      JMS I     NERROR      /TEST OKAY
242      JMS I     ERROR      /TEST FAILED
243      LIM001      /MESSAGE TAG
244      HLT      /ERROR HALT
245      SKP CLA      /EXIT
246      LIP001      /SCOPE LOOP

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0264 4025
0265 1071
0266 6151
0267 7330
0270 6154
0271 4432
0272 6141
0273 0713
0274 7000
0275 0002
0276 1033
0277 4434
0300 1035
0301 6151
0302 4025
0303 1055
0304 6151
0305 4436
0306 4437
0307 5261
0310 7402
0311 7610
0312 0264

/
/DOES TAPE PRESET CLEAR TAPE DONE M113,B16,M1,N1

/LIP002, JMS TPEPRE
TAD K1000
LMR
CLA CML CLL RAR
XFR
JMS I MAINT1
LINC
0713
7000
PDP
TAD K0016
JMS I LOADR
TAD K0040
LMR
JMS TPEPRE
TAD K0100
LMR
JMS I NERROR
JMS I ERROR
LIM002
HLT
SKP CLA
LIP002

/0>PROGRESS, 0>TAPE DONE
/GET AC > TAC
/LOAD MAINT REG
/SET AC00 (1)
/SET IAC00
/SET MAINT MODE
/L MODE
/MTB
/WASTED MEMORY
/P MODE
/GET 0H
/SET MARK WINDOW TO BLOCK
/GENERATE TP2
/LOAD MAINTENANCE REGISTER
/DOES TAPE PRESET 0 TAPE DONE
/SET AC05
/SKIP ON TAPE DONE
/TEST OKAY
/TEST FAILED
/MESSAGE TAG
/ERROR HALT
/EXIT
/SCOPE LOOP

274					
275					
276					/DOES LMR=ACB5 CLEAR TAPE DONE
277					/
278	0313	4025	LIP003, JMS	TPEPRE	/0>PROGRESS, 0>TAPE DONE
279	0314	1071	TAD	K1000	/GET AC > TAC
280	0315	6151	LMR		/LOAD MAINT REQ
281	0316	7330	CLA CML CLL RAR		/SET ACB0 (1)
282	0317	6154	XFR		/SET TACB0
283	0320	4432	JMS I	MAINT1	/SET MAINT MODE
284	0321	6141	LINC		/L MODE
285	0322	0713	0713		/MTB
286	0323	7000	7000		/WASTED MEMORY
287	0324	0002	PDP		/P MODE
288	0325	1033	TAD	K0016	/SET BM
289	0326	4434	JMS I	LOADR	/SET MARK WINDOW TO BLOCK MARK
290	0327	1035	TAD	K0040	/SET TP2
291	0330	6151	LMR		/GENERATE TP2
292	0331	7300	CLA CLL		/CLEAR AC,L
293	0332	1056	TAD	K0200	/0>TAPE DONE
294	0333	6151	LMR		/ZERO TAPE DONE
295	0334	7110	RAR CLL		/SET ACB5
296	0335	6151	LMR		/SKID ON TAPE DONE
297	0336	4436	JMS I	NERROR	/TEST OKAY
298	0337	4437	JMS I	ERROR	/TEST FAILED
299	0340	5307	LIP003		/MESSAGE TAG
300	0341	7402	HLT		/ERROR HALT
301	0342	7510	SKP CLA		/EXIT
302	0343	0513	LIP003		/SCOPE LOOP

```

303
304 /DOES STD AND STD+20 WORK TAPE DONE = 1 PROGRESS = 1
305 /
306 0344 4025 LIP004, JMS TPEPRE /GENERATE TAPE PRESET
307 0345 1071 TAD K1000 /GET AC > TAC
308 0346 6151 LMR /LOAD MAINT REG
309 0347 7330 CLA CLL CML RAR /SET AC00
310 0350 6134 XFR /SET TAC00(0)
311 0351 4432 JMS I MAINT1 /SET NO PAUSE
312 0352 6141 LINC /L MODE
313 0353 0713 0713 /MTB
314 0354 7000 7000 /WASTED MEMORY
315 0355 0002 PDP /P MODE
316 0356 6151 LMR /GENERATE TP2
317 0357 7300 CLA CLL /CLEAR AC,L
318 0360 6141 LINC /GO TO LINC MODE
319 0361 0416 STD /SKIP ON TAPE MODE
320 0362 0017 COM /SET AC TO CLEAR LATER
321 0363 0017 COM /SET OR CLEAR
322 0364 0002 PDP /GO TO 8 MODE
323 0365 7640 SZA CLA /TEST IF=7777 IT SKIPPED
324 0366 5521 JMP I LIA004 /STD FAILED
325 0367 6141 LINC /GO TO LINC MODE
326 0370 0436 STD 20 /STD+20
327 0371 0017 COM /SET AC TO CLEAR LATER
328 0372 0017 COM /SET OR CLEAR
329 0373 0002 PDP /GO TO 8 MODE
330 0374 7640 SZA CLA /TEST FOR ALL 0000
331 0375 4436 JMS I NERROR /ALL 0000 NO ERROR
332 0376 4437 LIB004, JMS I ERROR /TROUBLE
333 0377 5326 LIM004 /MESSAGE ID
334 0400 7402 HLT /ERROR HALT
335 0401 7610 SKP CLA /EXIT
336 0402 0344 LIP004 /SCOPE MODE

```

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337
338
339      /DOES STD AND STD+20 FUNCTION TAPE DONE = 0 PROGRESS = 0
340      /
341      0403  4025  LIP005, JMS      TPEPRE      /0>TAPE DONE
342      0404  6141      LINC      /GO TO LINC MODE
343      0405  0416      STD      /STD SHOULD NOT SKIP
344      0406  0017      COM      /IT DIDN'T SO SET THE AC
345      0407  0017      COM      /CLEAR AC IF IT DIDN'T SKIP
346      0410  0002      PDP      /GO TO 8 MODE
347      0411  7650      SNA CLA      /TEST FOR ALL ZEROS
348      0412  5222      JMP      LIB005      /STD FAILED
349      0413  6141      LINC      /GO TO LINC MODE
350      0414  0436      STD 2      /STD SHOULD SKIP
351      0415  0017      COM      /SET AC TO 7777
352      0416  0017      COM      /CLEAR IF NO SKIP
353      0417  0002      PDP      /GO TO 8 MODE
354      0420  7650      SNA CLA      /TEST FOR ALL ZEROS
355      0421  4436      JMS I      NERROR      /NO ERROR
356      0422  4437  LIB005, JMS I      ERROR      /ERROR
357      0423  5345      LIM005      /MESSAGE ID
358      0424  7402      HLT      /ERROR HALT
359      0425  7610      SKP CLA      /SCOPE LOOP
360      0426  0403      LIP005      /ERROR HALT
361
362      /
363      /DOES LIP TAPE INTERRUPT FUNCTION M113,C16,L2,M2,N2
364      /
365      0427  1060  LIP006, TAD      PNTA      /GET INTERRUPT RETURN
366      0430  3002      DCA      RETURN      /SET UP INTERRUPT RETURN
367      0431  1057      TAD      K0150      /SET MAINT, TAPE INT, NO PAUSE
368      0432  3107      DCA      K0050      /RESET MAINT
369      0433  4432      JMS I      MAINT1      /SET MAINT
370      0434  6141      LINC      /L MODE
371      0435  0713      0713      /MTB
372      0436  7000      7000      /WASTE SPACE
373      0437  0002      PDP      /P MODE
374      0440  1033      TAD      K0016      /GET BM
375      0441  4434      JMS I      LOADR      /SET MARK WINDOW TO BLOCK MARK
376      0442  1035      TAD      K0040      /GET TP2
377      0443  6151      LMR      /GENERATE TP2
378      0444  6001      ION      /TURN ON INTERRUPT
379      0445  7000      NOP      /WASTE TIME
380      0446  6002      IOF      /TURN OFF INTERRUPT
381      0447  7610      SKP CLA      /SKIP TO ERROR IF NO INT
382      0450  4436  LOCA, JMS I      NERROR      /TEST OKAY
383      0451  4437      JMS I      ERROR      /TEST FAILED
384      0452  5364      LIM006      /MESSAGE TAG
385      0453  7402      HLT      /ERROR HALT
386      0454  7610      SKP CLA      /EXIT
387      0455  0427      LIP006      /SCOPE LOOP
388      0456  1144      TAD      C0050      /GET 0050
389      0457  3107      DCA      K0050      /RESET

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390
391
392
393
394 0460 4025
395 0461 4432
396 0462 6141
397 0463 0710
398 0464 7000
399 0465 0002
400 0466 1070
401 0467 6151
402 0470 7300
403 0471 6154
404 0472 0066
405 0473 7640
406 0474 4436
407 0475 4437
408 0476 5410
409 0477 7402
410 0500 7610
411 0501 0460
412
413
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415 0502 4432
416 0503 6141
417 0504 0710
418 0505 7000
419 0506 0002
420 0507 4025
421 0510 1070
422 0511 6151
423 0512 7300
424 0513 6154
425 0514 0066
426 0515 7650
427 0516 4436
428 0517 4437
429 0520 5435
430 0521 7402
431 0522 7610
432 0523 0502

/DOES MTP SETUP SET THE IN PROGRESS FLOP M216,D19
LIP007, JMS      TPEPRE      /O PROGRESS
          JMS I    MAINT1     /SET NO PAUSE
          LINC     /L MODE
          0710     /TAPE COMMAND
          7000     /WASTE
          PDP      /P MODE
          TAD      K6000      /GET MISC STATUS 1 TO AC
          LMR      /LOAD MAINTENANCE REGISTER
          CLA CLL   /CLEAR AC,L
          XFR      /READ STATUS
          AND      K2000      /SAVE IN PROGRESS BIT
          SZA CLA   /WAS IT SET
          JMS I    NERROR     /TEST OKAY
          JMS I    ERROR      /TEST FAILED
          LIM007    /ERROR MESSAGE
          HLT       /ERROR HALT
          SKP CLA   /EXIT
          LIP007    /SCOPE LOOP

/DOES TAPE PRESET ZERO IN PROGRESS FLOP M216,C19
LIP008, JMS I    MAINT1     /SET NO PAUSE
          LINC     /L MODE
          0710     /TAPE COMMAND
          7000     /WASTE
          PDP      /P MODE
          JMS      TPEPRE     /TRY TO CLEAR IN PROGRESS
          TAD      K6000      /GET MISC STATUS 1 TO AC
          LMR      /LOAD MAINT REGISTER
          CLA CLL   /CLEAR AC,L
          XFR      /READ STATUS
          AND      K2000      /SAVE IN PROGRESS BIT
          SNA CLA   /DID IT CLEAR
          JMS I    NERROR     /TEST OKAY
          JMS I    ERROR      /TEST FAILED
          LIM008    /MESSAGE TAG
          HLT       /ERROR HALT
          SKP CLA   /EXIT
          LIP008    /SCOPE LOOP

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433
434
435 /DOES LCS(MTB*BM*SEARCH) ZERO IN PROGRESS M115 C25 PIN L2,M2
436 /
437 0524 4025 LIP009, JMS TPEPRE /ZERO EVERY THING
438 0525 4432 JMS I MAINT1 /SET NO PAUSE
439 0526 6141 LINC /L MODE
440 0527 0713 /TAPE COMMAND (MTB)
441 0530 7000 /WASTE
442 0531 0002 POP /P MODE
443 0532 1033 TAD K0016 /SET AC TO BLOCK MARK
444 0533 4434 JMS I LOADR /SET MARK WINDOW TO BM
445 0534 1067 TAD K0040 /SET MISC STATUS 1 TO AC AND TP1
446 0535 6151 LMR /1>SEARCH, 0> IN PROGRESS
447 0536 7300 CLA CLL /CLEAR AC,L
448 0537 6154 XFR /READ STATUS
449 0540 0066 AND K2000 /SAVE IN PROGRESS BIT
450 0541 7050 SNA CLA /TEST
451 0542 4436 JMS I NERROR /TEST OKAY
452 0543 4437 JMS I ERROR /TEST FAILED
453 0544 5464 LIM009 /MESSAGE TAG
454 0545 7402 HLT /ERROR HALT
455 0546 7010 SWP CLA /EXIT
456 0547 0524 LIP009 /SCOPE LOOP
457
458 /DOES M115 C25 PINS N2,P2,R2,S2 CLEAR IN PROGRESS
459 /
460 0550 4025 LIP010, JMS TPEPRE /ZERO EVERYTHING
461 0551 4432 JMS I MAINT1 /SET NO PAUSE
462 0552 6141 LINC /L MODE
463 0553 0712 /SET TINR 10 (1)
464 0554 7000 /WASTE
465 0555 0002 POP /P MODE
466 0556 1033 TAD K0016 /GET BLOCK MARK
467 0557 4434 JMS I LOADR /SET MARK WINDOW TO BM
468 0560 1055 TAD K0100 /GET SET FWD BIT
469 0561 6152 TRC /SET DIRTY TO FORWARD
470 0562 7300 CLA CLL /CLEAR AC,L
471 0563 1071 TAD K1000 /GET AC>TAG
472 0564 6151 LMR /LOAD MAINT REG
473 0565 7240 CLA CMA /SET AC=7777
474 0566 6154 XFR /SET IAC
475 0567 7300 CLA CLL /CLEAR AC,L
476 0570 1035 TAD K0040 /GET TP0,1,2
477 0571 6151 LMR /1>BLOCK
478 0572 7110 RAR CLL /SET AC = 0020
479 0573 6151 LMR /SET LC01 SO WE CAN DECODE CM
480 0574 7300 CLA CLL /CLEAR AC,L
481 0575 4434 JMS I LOADR /CLOSE WINDOW
482 0576 1035 TAD K0040 /SET TP0,1,2
483 0577 6151 LMR /GEN IP0,1,2

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484					
485	0600	7201	CLA	IAC	/SET OM
486	0601	4434	JMS	I LOADR	/SET MARK WINDOW TO CM
487	0602	1035	TAD	K0040	/GET TP0,1,2
488	0603	6151	LMR		/1>CHKWRD
489	0604	1070	TAD	K5000	/ADD MISC STATUS 1 TO AC
490	0605	6151	LMR		/GENERATE TP0,1,2 0>IN PROGRESS
491	0606	7300	CLA	CLL	/CLEAR AC,L
492	0607	6154	XFR		/READ DATA
493	0610	0066	AND	K2000	/SAVE IN PROGRESS BIT
494	0611	7650	SNA	CLA	/TEST
495	0612	4436	JMS	I NERROR	/TEST OKAY
496	0613	4437	JMS	I ERROR	/TEST FAILED
497	0614	5516	LIM010		/MESSAGE TAG
498	0615	7402	HLT		/ERROR HALT
499	0616	7610	SKP	CLA	/EXIT
500	0617	0550	LIP010		/SCOPE LOOP

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501
502
503 /DOES LIP PROGRESS FLOP GET ZEROED BY TAPE PRESET
504 /IF THIS TEST FAILS THE COMPUTER WILL HANG UP WITH
505 /NO TYPE OUT DUE TO TAPE PAUSE
506 /
507 0620 4432 LIP011, JMS I MAINT1 /SET NO PAUSE
508 0621 6141 LINC /L MODE
509 0622 0700 0700 /TAPE INSTRUCTION 1 SET PROGRESS
510 0623 7000 7000 /WASTE
511 0624 0002 PDP /P MODE
512 0625 4025 JMS TPEPRE /0>PAUSE, 0>PROGRESS
513 0626 2115 IS2 REGA /DONE YET
514 0627 5220 JMP LIP011 /REDO

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515
516
517 /DOES M115 C25 PINS N2,P2,R2,S2 ZERO PROGRESS FLOP
518 /
519 LIP012, JMS TPEPRE /0>TAPE DONE
520 0630 4025 JMS I MAINT1 /SET NO PAUSE
521 0631 4432 LINC /L MODE
522 0632 6141 0712 /SET TJNR 10(1)
523 0633 0712 7000 /WASTE
524 0634 7000 PDP /P MODE
525 0635 0002 TAD K0016 /GET BLOCK MARK
526 0636 1033 JMS I LOADR /SET MARK WINDOW TO BM
527 0637 4434 TAD K0100 /GET SET FWD BIT
528 0640 1055 TRC /SET DIR FWD
529 0641 6152 CLA CLL /CLEAR AC,L
530 0642 7300 TAD K1000 /GET AC>TAC
531 0643 1071 LMR /LOAD MAINT REQ
532 0644 6151 CLA CMA /SET AC=7777
533 0645 7240 XFR /SET IAC
534 0646 6154 CLA CLL /CLEAR AC,L
535 0647 7300 TAD K0040 /GET TP0,1,2
536 0650 1035 LMR /1>BLOCK
537 0651 6151 RAR CLL /SET AC = 0020
538 0652 7110 LMR /SET LC01
539 0653 6151 CLA CLL /CLEAR AC,L
540 0654 7300 JMS I LOADR /CLOSE WINDOW
541 0655 4434 TAD K0040 /SET TP0,1,2
542 0656 1035 LMR /GEN TP0,1,2
543 0657 6151 CLA IAC /SET CM
544 0660 7201 JMS I LOADR /SET MARK WINDOW TO BM
545 0661 4434 TAD K0040 /GET TP0,1,2
546 0662 1035 LMR /1>CHDWRK
547 0663 6151 LMR /0>PROGRESS
548 0664 6151 CLA CLL /CLEAR AC,L
549 0665 7300 TAD K0100 /SET AC05
550 0666 1055 LMR /SKIP ON TAPE DONE (1)
551 0667 6151 SKP CLA /REVERSE
552 0670 7010 JMS I NERROR /TEST OKAY
553 0671 4436 JMS I ERROR /TEST FAILED
554 0672 4437 LIM012 /MESSAGE TAG
555 0673 6025 HLT /ERROR HALT
556 0674 7402 SKP CLA /EXIT
557 0675 7610 LIP012 /SCOPE LOOP
558 0676 0630

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0677	4025	LIP013, JMS	TPEPRE	/0 EVERYTHING
0700	4432	JMS I	MAINT1	/SET NO PAUSE
0701	6141	LINC		/L MODE
0702	0712	0712		/TAPE SET WRITE CYCLE
0703	7000	7000		/WASTE
0704	0002	PDP		/P MODE LIN TINR 09 (0)
0705	1035	TAD	K0040	/SET FOR TP2
0706	6151	LMR		/GP EQ GPC (1)
0707	7300	CLA CLL		/CLEAR AC,L
0710	1071	TAD	K1000	/GET AC>TAC
0711	6151	LMR		/LOAD MAINT REGISTER
0712	7240	CLA CMA		/SET AC
0713	6154	XFR		/SET TAC
0714	7300	CLA CLL		/CLEAR AC, L
0715	1033	TAD	K0016	/GET 0M
0716	4434	JMS I	LOADR	/LOAD WINDOW
0717	1035	TAD	K0100	/SET FWD
0720	6152	TRC		/SET FORWARD
0721	7300	CLA CLL		/CLEAR AC,L
0722	1035	TAD	K0040	/SET TP0,1,2
0723	6151	LMR		/SET BLOCK STATE
0724	7110	RAR CLL		/SET AC = 0020
0725	6151	LMR		/SET LC01
0726	7300	CLA CLL		/CLEAR AC,2
0727	4434	JMS I	LOADR	/SET WINDOW SHUT
0730	1035	TAD	K0040	/SET TP0,1,2
0731	6151	LMR		/GEN TP0,1,2
0732	7301	CLL CLA	IAC	/SET AC
0733	4434	JMS I	LOADR	/SET CM
0734	1035	TAD	K0040	/SET TP0,1,2
0735	6151	LMR		/1> CHK WRD
0736	7300	CLA CLL		/CLEAR AC,L
0737	1071	TAD	K1000	/GET AC>TAC
0740	6151	LMR		/LOAD MAINT REG
0741	7240	CLA CMA		/SET AC
0742	6154	XFR		/SET TAC
0743	7300	CLA CLL		/CLEAR AC,L
0744	1110	TAD	K0020	/GET TP3
0745	6151	LMR		/0 IN PROGRESS
0746	7300	CLA CLL		/CLEAR AC,L
0747	1070	TAD	K6000	/GET MISC STATUS 1 TO AC
0750	6151	LMR		/LOAD MAINT REG
0751	7300	CLA CLL		/CLEAR AC,L
0752	6154	XFR		/READ DATA
0753	0066	AND	K2000	/SAVE IN PROGRESS
0754	7650	SNA CLA		/TEST
0755	4436	JMS I	NERROR	/TEST OKAY
0756	4437	JMS I	ERROR	/TEST FAILED
0757	5544	LIM013		/MESSAGE TAG
0760	7402	HLT		/ERROR HALT

/PDP-12 TAPE CONTROL TEST PART II, MAINDEC 12-D3GA-L

PAL10 V141

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613 0761 7610
614 0762 0677

SKP CLA
LIP013

/EXIT
/SCOPE LOOP

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615 /
616 /DOES M119,C22 PIN P2 CLEAR PROGRESS FLOP
617 /
618 0763 4025 LIP015, JMS TPEPRE /O>EVERYTHING
619 0764 4432 JMS I MAINT1 /SET NO PAUSE
620 0765 6141 LINC /L MODE
621 0766 0712 0712 /TAPE
622 0767 7000 7000 /WASTED MEMORY SPACE
623 0770 0002 PDP /P MODE LIN TINR 09 (0)
624 0771 1071 TAD K0000 /GET AC>TAC
625 0772 6151 LMR /LOAD MAINT REG
626 0773 7240 CLA CMA /SET AC=7777
627 0774 6154 XFR /SET TAC=7777
628 0775 7300 CLA CLL /CLEAR AC,L
629 0776 1033 TAD K0016 /GET BM
630 0777 4434 JMS I LOADR /LOAD WINDOW
631 1000 1055 TAD K0100 /SET FWD
632 1001 6152 TRC /SET FORWARD
633 1002 7300 CLA CLL /CLEAR AC,L
634 1003 1035 TAD K0040 /SET TP0,T,2
635 1004 6151 LMR /SET BLOCK STATE
636 1005 7104 CLL RAL /SET TP3
637 1006 6151 LMR /GENERATE TP3
638 1007 7300 CLA CLL /CLEAR AC,L
639 1010 4434 JMS I LOADR /CLEAR MARK WINDOW
640 1011 1035 TAD K0040 /SET FOR TP0, 1, 2
641 1012 6151 LMR /GENERATE TP0, 1, 2
642 1013 7301 CLL CLA IAC /SET AC=1
643 1014 4434 JMS I LOADR /SET CM
644 1015 1035 TAD K0040 /SET TP0,1,2
645 1016 6151 LMR /1>CHK WRD
646 1017 7300 CLA CLL /CLEAR AC,2
647 1020 1071 TAD K1000 /GET TAC>AC
648 1021 6151 LMR /LOAD MAINT REG
649 1022 7240 CLA CMA /SET AC=7777
650 1023 6154 XFR /SET TAC
651 1024 7300 CLA CLL /CLEAR AC,L
652 1025 1110 TAD K0020 /GET TP0
653 1026 6151 LMR /O>PROGRESS
654 1027 7300 CLA CLL /CLEAR AC,L
655 1030 1055 TAD K0100 /SET AC05
656 1031 6151 LMR /SKIP ON TAPE DONE
657 1032 7610 SKP CLA
658 1033 4436 JMS I NERROR /TEST OKAY
659 1034 4437 JMS I ERROR /TEST FAILED
660 1035 5567 LIM015 /MESSAGE TAG
661 1036 7402 HLT /ERROR HALT
662 1037 7610 SKP CLA /EXIT
663 1040 0763 LIP015 /SCOPE LOOP

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664
665 /DOES M113 C16,PINS M1,J1,K1 WRITE CYCLE (0) CLEAR IN PROGRESS
666
667 1041 4025 LIP017, JMS TPEPRE /0>EVERYTHING
668 1042 4432 JMS I MAINT1 /SET NO PAUSE
669 1043 6141 LINC /L MODE
670 1044 0716 0716 /SET TINR 09 (1)
671 1045 7000 7000 /WASTED MEMORY
672 1046 0002 PDP /SET WRITE CYCLE
673 1047 1033 TAD K0016 /GET BM
674 1050 4434 JMS I LOADR /SET WINDOW TO BM
675 1051 1071 TAD K1000 /GET AC>TAC
676 1052 6151 LMR /LOAD MAINT REG
677 1053 7240 CLA CMA /SET AC=7777
678 1054 6154 XFR /SET TAC=7777
679 1055 7300 CLA CLL /CLEAR AC,L
680 1056 1056 TAD K0200 /GET DIRECTION BIT
681 1057 6152 TRC /SET DIRECTION FORWARD
682 1060 7300 CLA CLL /CLEAR AC,L
683 1061 1035 TAD K0040 /SET UP FOR TP0,TP1,TP2
684 1062 6151 LMR /1>SEARCH, 1>BLOCK
685 1063 7344 CLA CMA CLL RAL /SET AC=7776=CM
686 1064 4434 JMS I LOADR /SET MARK WINDOW TO BLOCK MARK
687 1065 1035 TAD K0040 /SET UP FOR TP2
688 1066 6151 LMR /1>CHK WRD
689 1067 6151 LMR /0>WRITE CYCLE
690 1070 7201 CLA IAC /SET RWD BM
691 1071 4434 JMS I LOADR /SET MARK WINDOW
692 1072 1035 TAD K0040 /SET UP FOR TP0,1,2
693 1073 7344 CLA CLL CMA RAL /SET AC=7776=CM
694 1074 4434 JMS I LOADR /SET MARK WINDOW TO CM
695 1075 1035 TAD K0040 /SET FOR TP0,TP1,TP2
696 1076 6151 LMR /SET 1>CHK-WRD
697 1077 7110 CLL RAR /SET AC=0020
698 1100 6151 LMR /GEN TP3,TP4
699 1101 7300 CLA CLL /CLEAR AC,L
700 1102 1070 TAD K6000 /GET MISC STATUS 1 TO AC
701 1103 6151 LMR /LOAD MAINT REG
702 1104 7300 CLA CLL /CLEAR AC,L
703 1105 6154 XFR /READ DATA
704 1106 0066 AND K2000 /SAVE IN PROGRESS FLOP
705 1107 7640 SZA CLA /TEST
706 1110 4436 JMS I NERROR /TEST OKAY
707 1111 4437 JMS I ERROR /TEST FAILED
708 1112 5611 LIM017 /MESSAGE TAG
709 1113 7402 HLT /ERROR HALT
710 1114 7610 SKP CLA /EXIT
711 1115 1041 LIP017 /SCOPE LOOP

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712		/		
713		/DOES CLEAR TAPE WORD AND STW WORK		
714		/		
715	1116	4025	LIP018, JMS	TPEPRE
716	1117	6141	LINC	/GENERATE TAPE PRESET
717	1120	0457	STW	/GO TO LINC MODE
718	1121	0017	COM	/SKIP ON TAPE WORD
719	1122	0017	COM	/SET AC TO CLEAR LATER
720	1123	0002	PDP	/SET OR CLEAR
721	1124	7650	SNA CLA	/GO TO 8 MODE
722	1125	7040	CMA	/TEST IF=7777 IT SKIPPED
723	1126	6141	LINC	/ERROR AC=0000
724	1127	0477	STW 20	/GO TO LINC MODE
725	1130	0017	COM	/STW *20
726	1131	0017	COM	/SET AC TO CLEAR LATER
727	1132	0002	PDP	/SET OR CLEAR
728	1133	7650	SNA CLA	/GO TO 8 MODE
729	1134	4436	JMS I	/TEST FOR ALL 0000
730	1135	4437	JMS I	/ALL 0000 NO ERROR
731	1136	5647	LIM018	/TROUBLE
732	1137	7402	HLT	/MESSAGE ID
733	1140	7610	SKP CLA	/ERROR HALT
734	1141	1116	LIP018	/EXIT
				/SCOPE MODE

735					
736					
737			/	/DOES TAPE WORD FUNCTION	
738			/		
739	1142	1056	LIP019,	TAD	K0200
740	1143	6152		TRC	
741	1144	4432		JMS I	MAINT1
742	1145	6141		LINC	
743	1146	0710		0710	
744	1147	7000		7000	
745	1150	0457		STW	
746	1151	0017		COM	
747	1152	0017		COM	
748	1153	0002		PDP	
749	1154	7640		SZA CLA	
750	1155	7040		CMA	
751	1156	6141		LINC	
752	1157	0477		STW 20	
753	1160	0017		COM	
754	1161	0017		COM	
755	1162	0002		PDP	
756	1163	7640		SZA CLA	
757	1164	4436		JMS I	NERROR
758	1165	4437		JMS I	ERROR
759	1166	5666		LIM019	
760	1167	7402		HLT	
761	1170	7610		SKP CLA	
762	1171	1142		LIP019	
763					

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/SET AC04(1)
/GENERATE CLEAR TAPE WORD
/SET NO PAUSE
/TO LMODE

/RDC U
/STW SHOULD NOT SKIP
/IT DIDN'T SO SET THE AC
/CLEAR AC IF IT DIDN'T SKIP
/GO TO 8 MODE
/TEST FOR ALL ZEROS
/ERROR AC=7777
/GO TO LINC MODE
/STW SHOULD SKIP
/SET AC TO 7777
/CLEAR IF NO SKIP
/GO TO 8 MODE
/TEST FOR ALL ZEROS
/NO ERROR
/ERROR
/MESSAGE TAG
/ERROR HALT
/SCOPE LOOP
/ERROR HALT

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764				
765				
766			/	/DOES LC00 AND LC01 CONTROL TAPE WORD
767			/	
768	1172	4025	LIP022, JMS	TPEPRE /SET IAPE WORD
769	1173	1033	TAD	K0016 /GET BLOCK MARK
770	1174	4434	JMS I	LOADR /SET MARK WINDOW TO BM
771	1175	1110	TAD	K0020 /GET TP3,TP4 TO SET LINE COUNTERS
772	1176	6151	LMR	/SET BOTH LINE COUNTERS
773	1177	7104	CLL RAL	/SET UP FOR TP0
774	1200	6151	LMR	/GENERATE TP0,TP1,TP2
775	1201	7110	CLL RAL	/SET UP FOR TP3
776	1202	6151	LMR	/THIS CLEARS TAPE WORD
777	1203	7300	CLA CLL	/CLEAR AC,L
778	1204	6141	LINC	/L MODE
779	1205	0457	STW	/SKIP ON TAPE WORD
780	1206	0017	COM	/SET IT
781	1207	0017	COM	/CLEAR IT
782	1210	0002	PDP	/P MODE
783	1211	7050	SNA CLA	/TEST RESULTS
784	1212	4436	JMS I	NERROR /TEST OKAY
785	1213	4437	JMS I	ERROR /TEST FAILED
786	1214	5705	LIM022	/MESSAGE TAG
787	1215	7402	HLT	/ERROR HALT
788	1216	7610	SKP CLA	/EXIT
789	1217	1172	LIP022	/SCOPE LOOP

790					
791			/	/DOES TAPE BREAK FUNCTION WITH (DM)	
792			/		
793	1220	4025	LIP024, JMS	TPEPRE	/0 EVERYTHING
794	1221	4432	JMS I	MAINT1	/SET NO PAUSE
795	1222	1145	TAD	K1400	/GET AC TO TMA
796	1223	6151	LMR		/LOAD MAINT REG
797	1224	7300	CLA CLL		/CLEAR AC,L
798	1225	1170	TAD	00176	/FETCH THE TEST ADDRESS
799	1226	3116	DCA	REGB	/STORE FOR TYPING
800	1227	1116	TAD	REGB	/FETCH IT
801	1230	6154	XFR		/SET TEST ADDRESS IN TMA
802	1231	6141	LINC		/L MODE
803	1232	0710	0710		/SET TINR 09 (0)
804	1233	7000	7000		/WASTE MEMORY
805	1234	0002	PDP		/P MODE
806	1235	7300	CLA CLL		/CLEAR AC,L
807	1236	1115	TAD	REGA	/FETCH DATA TO BE XFERED
808	1237	3117	DCA	REGC	/STORE IT
809	1240	1071	TAD	K1000	/GET AC TO TAC
810	1241	6151	LMR		/LOAD MAINT REG
811	1242	7240	CLA CMA		/SET AC=7777
812	1243	6154	XFR		/SET TAC
813	1244	7300	CLA CLL		/CLEAR AC,L
814	1245	1033	TAD	K0016	/GET BM
815	1246	4434	JMS I	LOADR	/SET BLOCK MARK
816	1247	1055	TAD	K0100	/GET FWD
817	1250	6152	TRC		/SET FWD
818	1251	7300	CLA CLL		/CLEAR AC,L
819	1252	1035	TAD	K0040	/GET TP0,1,2
820	1253	6151	LMR		/GEN TP0,1,2 SET BLOCK MODE
821	1254	7300	CLA CLL		/CLEAR
822	1255	1117	TAD	REGC	/GET DATA
823	1256	1040	TAD	K0002	/ADD TWO FOR CORRECTION
824	1257	6154	XFR		/AC>TB
825	1260	7300	CLA CLL		/CLEAR

826			TAD	K0011	/GET DM
827	1261	1153	JMS I	LOADR	/LOAD WINDOW
828	1262	4434	TAD	K0040	/GET TP0,1,2
829	1263	1035	LMR		/GO TO TAPE BREAK
830	1264	6151	CLA CLL		/CLEAR AC,L
831	1265	7300	TAD	LOC176	/GET CELL 0176
832	1266	1176	DCA	REGD	/STORE FOR TYPING
833	1267	3114	TAD	REGD	/FETCH IT
834	1270	1114	CIA		/NEGATE
835	1271	7041	TAD	REGC	/SUBTRACT DATA SOURCE
836	1272	1117	SNA CLA		/TEST
837	1273	7650	JMP I	PNTC	/TEST OKAY, NOW CHECK THAT TMA INCREMENTED (,+6)
838	1274	5462	JMS I	ERROR	/TEST FAILED
839	1275	4437	LIM023		/MESSAGE TAG
840	1276	5725	HLT		/ERROR HALT
841	1277	7402	SKP CLA		/EXIT
842	1300	7610	LIP024		/SCOPE LOOP
843	1301	1220	LOC.	TAD K7000	/GET COMMAND "TMA TO AC"
844	1302	1047	LMR		/LOAD IT
845	1303	6151	CLA CLL		
846	1304	7300	XFR		/GET TMA
847	1305	6154	DCA	REGC	/SAVE FOR TYPING
848	1306	3117	TAD	K177	/GET WHAT IT SHOULD BE
849	1307	1137	CIA		/NEGATE
850	1310	7041	TAD	REGC	/SUBTRACT WHAT IT IS
851	1311	1117	SNA CLA		/EQUAL?
852	1312	7650	JMS I	NERROR	/YES
853	1313	4436	JMS I	ERROR	/NO
854	1314	4437	TMATB		/MESSAGE TAG
855	1315	6752	HLT		/ERROR HALT
856	1316	7402	SKP CLA		/EXIT
857	1317	7610	LIP024		/SCOPE LOOP; ISZ LOOP
858	1320	1220			

```

859
860
861 /
862 /TC12-B-LCX TAPE EXTENDED OPERATIONS (MARK FLOP)
863 /
864 LCX000, JMS      TPEPRE      /0 EVERYTHING
865      1321 4025      TAD      REGA      /GET A TEST NUMBER
866      1322 1115      AND      K0200     /SAVE MARK BIT
867      1323 0056      DCA      REGB      /STORE TEST BIT
868      1324 3116      TAD      REGB      /FETCH BIT
869      1325 1116      LINC      /L MODE
870      1326 6141      AXO      /LOAD MARK BIT
871      1327 0001      CLR      /CLEAR AC,L
872      1330 0011      XOA      /READ EXTENDED OPS REGISTER
873      1331 0021      PDP      /P MODE
874      1332 0002      AND      K0200
875      1333 0056      DCA      REGC      /STORE FOR TESTING
876      1334 3117      TAD      REGC      /FETCH RETURNED DATA
877      1335 1117      CIA      /NEGATE
878      1336 7041      TAD      REGB      /SUBTRACT DATA SOURCE
879      1337 1116      SNA CLA /TEST RESULTS
880      1340 7650      JMS I   NERROR    /TEST OKAY
881      1341 4436      JMS I   ERROR     /TEST FAILED
882      1342 4437      LCM000 /MESSAGE TAG
883      1343 5746      HLT      /ERROR HALT
884      1344 7402      SKP      CLA      /EXIT
885      1345 7610      LCX000 /SCOPE LOOP
886
887 /
888 /DOES TAPE PRESET ZERO THE MARK FLOP
889 /
890 LCX001, TAD      K0200      /GET AC05
891      1347 1056      LINC      /L MODE
892      1350 6141      AXO      /SET MARK FLOP
893      1351 0001      PDP      /P MODE
894      1352 0002      JMS      TPEPRE    /GENERATE TAPE PRESET
895      1353 4025      LINC      /L MODE
896      1354 6141      XOA      /READ EXTENDED OPS REGISTER
897      1355 0021      PDP      /P MODE
898      1356 0002      AND      K0200     /SAVE MARK BIT
899      1357 0056      SNA CLA /TEST
900      1360 7650      JMS I   NERROR    /TEST OKAY
901      1361 4436      JMS I   ERROR     /TEST FAILED
902      1362 4437      LCM001 /MESSAGE TAG
903      1363 5762      HLT      /ERROR HALT
904      1364 7402      SKP CLA /EXIT
905      1365 7610      LCX001 /SCOPE LOOP
906      1366 1347

```

```

904
905
906      /TC12-0=LIN M113,826, PINS P1,R1,S1(TAC=7777=FWD)
907
908
909      /DOES THE GATE RESPOND TO FALSE INPUTS (TAC=7777 AND DIRECTION=REVERSE)
910
911      /
912      LIN001, JMS      TPEPRE      /CLEAR THE WORLD
913              JMS I    MAINT1      /SET NO PAUSE
914              LINC      0700      /L MODE
915              7000      /SET MTB, NOT
916              PDP        0002      /WASTE
917              TAD        K0016     /P MODE
918              JMS I      LOADR      /GET BLOCK MARK
919              TAD        K1000     /SET WINDOW TO BLOCK MARK
920              LMR        6151      /GET AC TO TAC
921              CLA CMA      7240     /LOAD MAINT REG
922              XFR        6154      /SET AC=7777
923              AND        K4440     /SET TAC=0000 7777,NOT
924              LMR        6151      /STATES TO AC AND GENERATE TPK,T 1,TP2
925              CLA CLL      7300     /LOAD MAINT REG TRY TO SET BLOCK
926              XFR        6154      /CLEAR AC,L
927              AND        K3700     /READ MAJOR STATES
928              DCA        REG8      /SAVE MAJOR STATES
929              TAD        REG8      /STORE DATA
930              TAD        M1000     /FETCH DATA
931              SNA CLA      7650     /SUBTRACT SEARCH MODE
932              JMS I      NERROR     /TEST
933              JMS I      ERROR      /TEST OKAY
934              LINMX1      6047      /TEST FAILED
935              HLT        7402      /MESSAGE TAG
936              SKP CLA      7610     /ERROR HALT
937              LIN001      1367     /EXIT
938              /SCOPE LOOP
939
940      /DOES THE GATE RESPOND TO (TAC=0000 AND DIRECTION=FORWARD)
941
942      /
943      LIN002, JMS      TPEPRE      /CLEAR THE WORLD
944              JMS I    MAINT1      /SET NO PAUSE
945              LINC      0700      /L MODE
946              7000      /SET MTB-NOT
947              PDP        0002      /WASTE
948              TAD        K0016     /P MODE
949              JMS I      LOADR      /GET BM
950              TAD        K1000     /SET MARK WINDOW TO BM
951              LMR        6151      /GET AC>TAC
952              CLA CLL      7300     /LOAD MAINT REGISTER
953              /CLEAR AC,L

```

952			XFR		/SET TAC = 7777
953	1435	6154	TAD	K0100	/GET FWD BIT
954	1436	1055	TRC		/SET FORWARD
955	1437	6152	CLA CLL		/CLEAR AC,L
956	1440	7300	TAD	K4440	/TRY TO SET BLOCK MODE
957	1441	1122	LMR		/GENERATE TIMING
958	1442	6151	CLA CLL		/CLEAR AC,L
959	1443	7300	XFR		/READ DATA
960	1444	6154	AND	K3700	/SAVE SIGNIFICANT DATA
961	1445	0123	DCA	REGB	/STORE DATA
962	1446	3116	TAD	REGB	/FETCH DATA
963	1447	1116	TAD	M1000	/SUBTRACT SEARCH MODE
964	1450	1125	SNA CLA		/TEST
965	1451	7650	JMS I	NERROR	/TEST OKAY
966	1452	4436	JMS I	ERROR	/TEST BAD
967	1453	4437	LINMX2		/MESSAGE TAG
968	1454	6066	HLT		/ERROR HALT
969	1455	7402	SKP CLA		/EXIT
970	1456	7010	LIN002		/SCOPE LOOP
971	1457	1422			


```

972
973
974 /DOES M121 B25 V2,R2,S2 GENERATE TP3,TP4,
975 /
976 LTT004, JMS TPEPRE /O>EVERYTHING
977 TAD K0016 /SET BM
978 JMS I LOADR /SET MARK WINDOW TO BLOCK MARK
979 TAD K0250 /SET MARK, NO PAUSE, MAINT
980 LINC /L MODE
981 AXO /SET AOX
982 PDP /P MODE
983 TAD K0020 /SET IP3,TP4
984 LMR /LOAD MAINT REG 1SET LC01,LC00
985 RAL CLL /SET TP0,TP1,TP2
986 CLA CLL /CLEAR AC,L
987 TAD K6000 /GET MISC 1 TO AC
988 LMR /LOAD MAINT MODE
989 CLA CLL /CLEAR AC,L
990 XFR /READ STATUS
991 AND K0400 /SAVE LC01
992 SNA CLA
993 JMP ,+4
994 ISZ REGF /WAIT
995 JMP ,+6
996 SKP CLA
997 JMS I NERROR /TEST OKAY
998 JMS I ERROR /TEST FAILED
999 LTM004 /MESSAGE TAG
1000 HLT /ERROR HALT
1001 SKP CLA /EXIT
1002 LTT004 /SCOPE LOOP

```

1003				
1004			/TAPE 3	
1005			/TC12-0-LCS TAPE CONT STATES + INST	
1006			/	
1007			/CAN WE GO IDLE TO SEARCH	
1008			/	
1009	1513	4025	LCS000, JMS	TPEPRE /0 MAJOR STATE GENERATOR
1010	1514	4432	JMS I	MAINT1 /SET NO PAUSE
1011	1515	6141	LINC	/L MODE
1012	1516	0700	0700	/TAPE COMMAND USED TO SET -
1013	1517	7000	7000	/IN PROGRESS
1014	1520	0002	PDP	/P MODE
1015	1521	1122	TAD	K4440 /GENERATE TP1 AND SET STATES TO AC
1016	1522	6151	LMR	/THIS SHOULD SET SEARCH
1017	1523	7300	CLA CLL	/CLEAR AC,L
1018	1524	6154	XFR	/TRANSFER STATES TO AC
1019	1525	0123	AND	K3700 /SAVE STATES
1020	1526	3116	DCA	REGB /STORE FOR TYPING
1021	1527	1116	TAD	REGB /FETCH IT
1022	1530	1125	TAD	M1000 /SUBTRACT SEARCH MODE
1023	1531	7650	SNA CLA	/WERE WE IN IDLE MODE
1024	1532	4436	JMS I	NERROR /TEST OKAY
1025	1533	4437	JMS I	ERROR /TEST FAILED
1026	1534	6131	LCHX00	/MESSAGE TAG
1027	1535	7402	HLT	/ERROR HALT
1028	1536	7610	SKP CLA	/EXIT
1029	1537	1513	LCS000	/SCOPE LOOP

1030					
1031					
1032			/	DOES SEARCH TO BLOCK WORK	
1033			/		
1034	1540	4025	LCS001,	JMS	TPEPRE
1035	1541	4432		JMS I	MAINT1
1036	1542	6141		LINC	
1037	1543	0700		0700	
1038	1544	7000		7000	
1039	1545	0002		PDP	
1040	1546	1033		TAD	K0016
1041	1547	4434		JMS I	LOADR
1042	1550	1055		TAD	K0100
1043	1551	6152		TRC	
1044	1552	7300		CLA CLL	
1045	1553	1071		TAD	K1000
1046	1554	6151		LMR	
1047	1555	7240		CLA CMA	
1048	1556	6154		XFR	
1049	1557	7300		CLA CLL	
1050	1560	1122		TAD	K4440
1051	1561	6151		LMR	
1052	1562	7300		CLA CLL	
1053	1563	6154		XFR	
1054	1564	3116		DCA	REGB
1055	1565	1116		TAD	REGB
1056	1566	0123		AND	K3700
1057	1567	1124		TAD	M0400
1058	1570	7650		SNA CLA	
1059	1571	4436		JMS I	NERROR
1060	1572	4437		JMS I	ERROR
1061	1573	6147		LCMX01	
1062	1574	7402		HLT	
1063	1575	7610		SKP CLA	
1064	1576	1540		LCS001	

/0 MAJOR STATE GENERATOR

/SET NO PAUSE

/L MODE

/MTB.NOT

/P MODE

/GET FORWARD BIT

/SET FWD

/CLEAR AC,L

/GET AC TO TAC

/SET MAINT IR TO AC TO TAC

/SET AC=7777

/SET TAC=7777

/CLEAR AC,L

/SET STATES TO AC GENERATE TP1,TP2

/LOAD MAINT AND GENERATE TP0,TP1,TP2

/CLEAR AC,L

/READ STATUS

/STORE FOR TYPING

/FETCH IT

/SAVE MAJOR STATES

/SUBTRACT BLOCK MODE

/TEST

/TEST OKAY

/TEST FAILED

/MESSAGE TAG

/ERROR HALT

/EXIT

/SCOPE LOOP

1065			
1066			
1067			/DOES SEARCH TO TURN AROUND FUNCTION
1068			
1069	1577	4025	LCS002, JMS TPEPRE /0 MAJOR STATE GENERATOR
1070	1600	4432	JMS I MAINT1 /SET NO PAUSE
1071	1601	6141	LINC /L MODE
1072	1602	0703	0703 /MTB
1073	1603	7000	7000
1074	1604	0002	PDP /P MODE
1075	1605	1033	TAD K0016 /GET BM
1076	1606	4434	JMS I LOADR /LOAD WINDOW
1077	1607	1071	TAD K1000 /GET AC TO TAC
1078	1610	6155	LMR XFR /SET TAC=7777,NOT
1079	1611	7300	CLA CLL /CLEAR AC,L
1080	1612	1122	TAD K4440 /SET STATES TO AC GENERATE TP1,TP2
1081	1613	6151	LMR /SET COMMAND AND GENERATE TIMING
1082	1614	7300	CLA CLL /CLEAR AC,L
1083	1615	6154	XFR /TRANSFER
1084	1616	0123	AND K3700 /SAVE MAJOR STATES
1085	1617	3116	DCA REG8 /STORE FOR TYPING
1086	1620	1116	TAD REG8 /FETCH FOR TYPING
1087	1621	1150	TAD M0100 /SUBTRACT TURN AROUND
1088	1622	7650	SNA CLA /TEST
1089	1623	4436	JMS I NERROR /TEST OKAY
1090	1624	4437	JMS I ERROR /TEST
1091	1625	6165	LCM002 /MESSAGE TAG
1092	1626	7402	HLT /ERROR HALT
1093	1627	7610	SKP CLA /EXIT
1094	1630	1577	LCS002 /SCOPE LOOP

1095				
1096				
1097			/	/DOES TURN AROUND TO IDLE WORK
1098			/	
1099	1631	4025	LCS003, JMS	TPEPRE /0 MAJOR STATE GENERATOR
1100	1632	4432	JMS I	MAINT1 /SET NO PAUSE
1101	1633	6141	LINK	/L MODE
1102	1634	0703	0703	/SET MTB
1103	1635	7000	7000	/SETS IN PROGRESS
1104	1636	0002	PDP	/P MODE
1105	1637	1033	TAD	K0016 /GET BM
1106	1640	4434	JMS I	LOADR /SET WINDOW TO BLOCK MARK
1107	1641	1122	TAD	K4440 /IDLE TO SEARCH TO TURN AROUND
1108	1642	6151	LMR	/GENERATE TP1,TP2 TO SET TURN AROUND
1109	1643	6151	LMR	/TRY TO GO TO IDLE
1110	1644	7300	CLA CLL	/CLEAR AC, LINK
1111	1645	6154	XFR	/READ STATUS
1112	1646	0123	AND	K3700 /SAVE MAJOR STATES
1113	1647	3116	DCA	REGB /STORE FOR TYPING
1114	1650	1116	TAD	REGB /FETCH
1115	1651	1151	TAD	M2000 /SUBTRACT IDLE MODE
1116	1652	7650	SNA CLA	/TEST
1117	1653	4436	JMS I	NERROR /TEST OKAY
1118	1654	4437	JMS I	ERROR /TEST FAILED
1119	1655	6206	LCH003	/MESSAGE TAG
1120	1656	7402	HLT	/ERROR HALT
1121	1657	7618	SKP CLA	/EXIT
1122	1660	1631	LCS003	/SCOPE LOOP

1123				
1124				
1125			/DOES BLOCK TO CHK WRD WORK	
1126				
1127	1661	4025	LCS004, JMS	TPEPRE
1128	1662	4432	JMS I	MAINT1
1129	1663	6141	LINC	
1130	1664	0700	0700	
1131	1665	7000	7000	
1132	1666	0002	PDP	
1133	1667	1033	TAD	K0016
1134	1670	4434	JMS I	LOADR
1135	1671	1055	TAD	K0100
1136	1672	6152	TRC	
1137	1673	7300	CLA CLL	
1138	1674	1071	TAD	K1000
1139	1675	6151	LMR	
1140	1676	7240	CLA CMA	
1141	1677	6154	XFR	
1142	1700	7300	CLA CLL	
1143	1701	1122	TAD	K4440
1144	1702	6151	LMR	
1145	1703	7300	CLA CLL	
1146	1704	4434	JMS I	LOADR
1147	1705	1035	TAD	K0040
1148	1706	6151	LMR	
1149	1707	7201	CLA IAC	
1150	1710	4434	JMS I	LOADR
1151	1711	1122	TAD	K4440
1152	1712	6151	LMR	
1153	1713	7300	CLA CLL	
1154	1714	6154	XFR	
1155	1715	0123	AND	K3700
1156	1716	3116	DCA	REGB
1157	1717	1116	TAD	REGB
1158	1720	1152	TAD	M0200
1159	1721	7650	SNA CLA	
1160	1722	4436	JMS I	NERROR
1161	1723	4437	JMS I	ERROR
1162	1724	6226	LCS004	
1163	1725	7402	HLT	
1164	1726	7610	SKP CLA	
1165	1727	1661	LCS004	

/0 MAJOR STATE GENERATOR

/SET NO PAUSE

/L MODE

/MTB,NOT

/SET IN PROGRESS

/P MODE

/GET BM

/SET BLOCK MARK

/SET FWD BIT

/SET FORWARD

/CLEAR AC,L

/GET AC TO TAC COMMAND

/LOAD MAINT REG

/SET AC=7777

/SET TAC=7777

/CLEAR AC,L

/GENERATE TP2,TP1,TP0

/AND SET STATES TO AC SETS BLOCK WORD

/CLEAR AC,L

/SET WIND.

/GET TP0

/SET CM

/SET WINDOW TO CHECK MARK

/SET UP FOR TP2

/LOAD MAINT REG

/CLEAR AC,L

/READ STATUS

/SAVE MAJOR STATES

/STORE FOR TYPING

/FETCH IT

/SUBTRACT CHECK WORD

/TEST

/TEST OKAY

/TEST FAILED

/MESSAGE TAG

/ERROR HALT

/EXIT

/SCOPE LOOP

1166				
1167				
1168			/	
1169			/DOES CHK WRD TO IDLE WORK	
1170	1730	4025	LCS005, JMS	TPEPRE
1171	1731	4432	JMS I	MAINT1
1172	1732	6141	LINC	
1173	1733	0700	0700	
1174	1734	7000	7000	
1175	1735	0002	PDP	
1176	1736	1033	TAD	K0016
1177	1737	4434	JMS I	LOADR
1178	1740	1055	TAD	K0100
1179	1741	6152	TRC	
1180	1742	7300	CLA CLL	
1181	1743	1071	TAD	K1000
1182	1744	6151	LMR	
1183	1745	7240	CLA CMA	
1184	1746	6154	XFR	
1185	1747	7300	CLA CLL	
1186	1750	1122	TAD	K4440
1187	1751	6151	LMR	
1188	1752	7300	CLA CLL	
1189	1753	4434	JMS I	LOADR
1190	1754	1035	TAD	K0040
1191	1755	6151	LMR	
1192	1756	7301	CLA CLL	IAC
1193	1757	4434	JMS I	LOADR
1194	1760	1122	TAD	K4440
1195	1761	6151	LMR	
1196	1762	6151	LMR	
1197	1763	7300	CLA CLL	
1198	1764	6154	XFR	
1199	1765	0123	AND	K3700
1200	1766	3116	DCA	REGB
1201	1767	1116	TAD	REGB
1202	1770	1151	TAD	M2000
1203	1771	7650	SNA CLA	
1204	1772	4436	JMS I	NERROR
1205	1773	4437	JMS I	ERROR
1206	1774	6245	LCM005	
1207	1775	7402	HLT	
1208	1776	7618	SKP CLA	
1209	1777	1730	LCS005	

/0 MAJOR STATE GENERATOR

/SET NO PAUSE

/L MODE

/MTB,NOT

/SET IN PROGRESS

/P MODE

/SET BN

/SET MARK WINDOW TO BLOCK MARK

/SET FWD BIT

/SET FORWARD

/CLEAR AC,L

/GET AC TO TAC COMMAND

/LOAD MAINT REG

/SET AC=7777

/SET TAC

/CLEAR AC,L

/GEN TP1,TP2

/SET BLOCK MODE

/CLEAR AC,L

/SET WIND,

/GET TP0

/GET CN

/SET CHECK WORD

/GET TP2 TO SET CHK-WRD

/SET CHECK WORD

/DOES CM*CHK WRD AND PROGRESS (1) SET IDLE

/CLEAR AC,L

/READ STATUS

/STORE FOR TYPING

/FETCH FOR TESTING

/SUBTRACT IDLE MODE

/TEST

/TEST OKAY

/TEST FAILED

/MESSAGE TAG

/ERROR HALT

/EXIT

/SCOPE LOOP

1210				
1211				
1212			/DOES MTB+I SET IDLE FROM SEARCH	
1213			/	
1214	2000	4025	LCS006, JMS	TPEPRE /0 EVERYTHING
1215	2001	4432	JMS I	MAINT1 /SET NO PAUSE
1216	2002	6141	LINC	/L MODE
1217	2003	0723	0723	/MTB I
1218	2004	7000	7000	/SET IN PROGRESS
1219	2005	0002	PDP	/P MODE
1220	2006	1033	TAD	K0016 /GET BM
1221	2007	4434	JMS I	LOADR /SET BLOCK MARK
1222	2010	1122	TAD	K4440 /GENERATE TP1, TP2
1223	2011	6151	LMR	/GO TO SEARCH MODE THEN BACK TO IDLE
1224	2012	7300	CLA CLL	/CLEAR AC, L
1225	2013	6154	XFR	/READ STATUS
1226	2014	0123	AND	K3700 /SAVE STATES
1227	2015	3116	DCA	REG8 /STORE IT FOR TYPING
1228	2016	1116	TAD	REG8 /FETCH IT
1229	2017	1151	TAD	M2000 /SUBTRACT IDLE MODE
1230	2020	7650	SNA CLA	/TEST
1231	2021	4436	JMS I	NERROR /TEST OKAY
1232	2022	4437	JMS I	ERROR /TEST FAILED
1233	2023	6261	LCM006	/MESSAGE TAG
1234	2024	7402	HLT	/ERROR HALT
1235	2025	7610	SKP CLA	/EXIT
1236	2026	2000	LCS006	/SCOPE LOOP


```

1237
1238
1239
1240
1241      2027  4025      LWNORM, JMS      TPEPRE      /0 > EVERYTHING
1242      2030  4432      JMS I      MAINT1      /SET MAINT
1243      2031  6141      LINC              /L MODE
1244      2032  0707      0707
1245      2033  0000      0000
1246      2034  0002      PDP              /P MODE
1247      2035  1115      TAD      REGA      /FETCH TEST NUMBER
1248      2036  6154      XFR              /SET TB TO TEST NUMBER
1249      2037  7300      CLA CL              /CLEAR AC, L
1250      2040  1071      TAD      K1000      /GET AC TO TAC
1251      2041  6151      LMR              /LOAD MAINT REG
1252      2042  7240      CLA CMA      /SET AC=7777
1253      2043  6154      XFR              /SET TAC REGISTER
1254      2044  0033      AND      K0016      /SET AC = TO BLOCK MARK
1255      2045  4434      JMS I      LOADR      /SET REVERSE AND LOAD WINDOW
1256      2046  1055      TAD      K0100      /GET FWD BIT
1257      2047  6152      TRC              /SET DIRECTION FORWARD
1258      2050  7300      CLA CLL              /CLEAR AC, L
1259      2051  1035      TAD      K0040      /SET UP FOR TPO,1,2
1260      2052  6151      LMR              /GO TO BLOCK MODE
1261      2053  7300      CLA CLL              /CLEAR AC, L
1262      2054  1153      TAD      K0011      /GET DM
1263      2055  4434      JMS I      LOADR      /LOAD
1264      2056  1035      TAD      K0040      /GET TP0
1265      2057  6151      LMR
1266      2060  4025      JMS      TPEPRE      /0 PROGRAMS
1267      2061  6141      LINC              /L MODE
1268      2062  0003      TAC              /READ TAC
1269      2063  0002      PDP              /P MODE
1270      2064  1163      TAD      K0003      /ADD THREE (SEE WRITE UP)
1271      2065  3116      DCA      REGB      /STORE FOR TYPING
1272      2066  1116      TAD      REGB      /FETCH
1273      2067  7041      CIA              /NEGATE
1274      2070  1115      TAD      REGA      /SUBTRACT DATA SOURCE
1275      2071  7650      SNA CLA      /TEST
1276      2072  4436      JMS I      NERROR      /TEST OKAY
1277      2073  4437      JMS I      ERROR      /TEST FAILED
1278      2074  6303      LWM101      /MESSAGE TAG
1279      2075  7402      HLT              /ERROR HALT
1280      2076  7610      SKP CLA      /EXIT
1281      2077  2027      LWNORM      /SCOPE LOOP

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1282
1283
1284
1285
1286      2100  4025      /
1287      2101  4432      /DOES MARK WRITE FUNCTION FIRST TEST IS FOR PHASE ON TC12-3-LTS
1288      2102  1067      /
1289      2103  6151      LWN102, JMS      TPREP      /0 EVERYTHING 0 CHKWRD
1290      2104  7300      JMS I      MAINT1
1291      2105  6154      TAD      K6040
1292      2106  7700      LMR      /SET UP FOR TP0
1293      2107  5357      CLA CLL      /SET LC02 (1)
1294      2110  1155      XFR      /CLEAR AC,L
1295      2111  6151      SMA CLA      /READ STATUS
1296      2112  7300      JMP      LWB102      /IS IT SET
1297      2113  6154      TAD      K6020      /NO ERROR
1298      2114  7710      LMR      /SET UP TP ZERO LC02
1299      2115  5357      CLA CLL      /0>LC02
1300      2116  6141      XFR      /CLEAR AC,L
1301      2117  0700      SPA CLA      /READ STATUS
1302      2120  0000      JMP      LWB102      /IS PHASE NOT SET
1303      2121  0002      LINC      /FAILED
1304      2122  1033      TAD      0700
1305      2123  4434      JMS I      LOADR      /GET BM
1306      2124  1071      TAD      K1000      /SET BLOCK MARK
1307      2125  6151      LMR      /GET AC>TAC
1308      2126  7240      CLA CMA      /LOAD MAINT REG
1309      2127  6154      AND      K0100      /SET AC=7777
1310      2130  0055      TRC      /SET TAC 7777
1311      2131  6152      CLA CLL      /SAVE FWD BIT
1312      2132  7300      TAD      K0040      /SET FORWARD
1313      2133  1035      LMR      /CLEAR AC,L
1314      2134  6151      JMS I      LOADR      /SET UP FOR TP0
1315      2135  7300      TAD      K0040      /1 BLOCK MODE
1316      2136  4434      LMR      /CLEAR AC, L
1317      2137  1035      CLA CLL      /CLEAR WINDOW
1318      2140  6151      JMS I      LOADR      /GEN TP0, 1, 2
1319      2141  7201      TAD      K0040      /SET LC01
1320      2142  4434      LMR      /SET CM
1321      2143  1067      CLA IAC      /SET WINDOW TO CHECK MARK
1322      2144  6151      JMS I      LOADR      /SET TO GO TO CHKWRD
1323      2145  7300      TAD      K6040      /GO TO CHKWRD 1 LC02
1324      2146  6154      LMR      /CLEAR AC,L
1325      2147  7710      SPA CLA      /READ STATUS
1326      2150  5357      JMP      LWB102      /DID PHASE COME UP IN ERROR
1327      2151  1155      TAD      K6020      /ERROR
1328      2152  6151      LMR      /SET FOR TP3
1329      2153  7300      CLA CLL      /0 LC02
1330      2154  6154      XFR      /CLEAR AC,L
1331      2155  7710      SPA CLA      /READ STATUS
1332      2156  4436      JMS I      WERROR      /IS IT SET
1333      2157  4437      LWB102, JMS I      ERROR      /TEST OKAY
1334      2160  6333      LWN102      /TEST FAILED
1335      2161  7402      HLT      /MESSAGE TAG
1336      2162  7610      SKP CLA      /ERROR HALT
1336      2162  7610      SKP CLA      /EXIT

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4PQP-12 TAPE CONTROL TEST PART 11, MAINDEC 12-D36A-L

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1337 2163 2100

LWN102

/SCOPE LOOP

1338					
1339					
1340			/	/TEST MARK WRITE	
1341			/		
1342	2164	4025	LWN104,	JMS	TPEPRE
1343	2165	1033		TAD	K0016
1344	2166	4434		JMS I	LOADR
1345	2167	1067		TAD	K6040
1346	2170	6151		LMR	
1347	2171	7300		CLA CLL	
1348	2172	6154		XFR	
1349	2173	0056		AND	K0200
1350	2174	7640		SZA CLA	
1351	2175	5572		JMP I	LWA104
1352	2176	1155		TAD	K6020
1353	2177	6151		LMR	
1354	2200	7300		CLA CLL	
1355	2201	6154		XFR	
1356	2202	0056		AND	K0200
1357	2203	7650		SNA CLA	
1358	2204	5572		JMP I	LWA104
1359	2205	4434		JMS I	LOADR
1360	2206	1067		TAD	K6040
1361	2207	6151		LMR	
1362	2210	7300		CLA CLL	
1363	2211	6154		XFR	
1364	2212	0056		AND	K0200
1365	2213	7650		SNA CLA	
1366	2214	5572		JMP I	LWA104
1367	2215	1155		TAD	K6020
1368	2216	6151		LMR	
1369	2217	7300		CLA CLL	
1370	2220	6154		XFR	
1371	2221	0056		AND	K0200
1372	2222	7650		SNA CLA	
1373	2223	4436		JMS I	NERROR
1374	2224	4437	LWB104,	JMS I	ERROR
1375	2225	6347		LWM104	
1376	2226	7402		HLT	
1377	2227	7610		SKP CLA	
1378	2230	2164		LWN104	

/2 > EVERYTHING 0 TO IDLE MODE
/SET WIND 00 (1)
/SET WINDOW BIT 00
/GET STATUS TO AC
/LOAD MAINT REG
/CLEAR AC,L
/READ MARK WRITE
/SAVE MARK WRITE
/DID IT SET
/NOPE ERROR
/GEN TP3
/LOAD MAINT REG
/CLEAR AC,L
/READ STATUS
/SAVE MARK WRITE
/DID IT STAY ZERO
/NOPE ERROR
/0 WIND
/TRY TO GET OUTPUT FROM WIND00-PHASE
/LOAD MAINT REG
/CLEAR AC,L
/READ STATUS
/SAVE MARK WRITE
/TEST IT
/ERROR
/RESET LC02 (1)
/LOAD MAINT REG
/CLEAR AC,L
/READ STATUS
/SAVE MARK WRITE
/TEST
/TEST OKAY
/TEST BAD
/MESSAGE TAG
/ERROR HALT
/EXIT
/SCOPE LOOP

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1379 /
1380 /LTS IC12-0-LTS
1381 /
1382 /
1383 /DOES DATA CHANNEL RWB 0,4,8 WORK
1384 /
1385 2231 4025 LTR000, JMS TPEPRE /0 EVERYTHING
1386 2232 1042 TAD K4210 /GET RWB 0,4,8
1387 2233 3116 DCA REG8 /STORE FOR TYPING
1388 2234 6151 LMR /SET MAINT REG TO AC > TB
1389 2235 1116 TAD REG8 /FETCH TEST DATA
1390 2236 6154 XFR /SET TB
1391 2237 7300 CLA CLL /CLEAR AC,L
1392 2240 1071 TAD K1000 /GET TB > RWB
1393 2241 6152 TRC /SET RWB
1394 2242 7300 CLA CLL /CLEAR AC,L
1395 2243 1070 TAD K6000 /GET MISC STATUS 1 TO AC
1396 2244 6151 LMR /SET DATA CHANNEL TO AC
1397 2245 7300 CLA CLL /CLEAR AC,L
1398 2246 6154 XFR /READ
1399 2247 0041 AND K0160 /SAVE IT
1400 2250 3117 DCA REGC /STORE IT
1401 2251 1117 TAD REGC /FETCH IT
1402 2252 7640 SZA CLA /TEST
1403 2253 5274 JMP LTB000 /BLUNDER
1404 2254 3116 DCA REG8 /TRY TESTING WITH ZERO DATA
1405 2255 6155 LMR XFR /SET MAINT REG TO AC > TB
1406 2256 1071 TAD K1000 /GET TB > RWB
1407 2257 6152 TRC /SET RWB
1408 2260 7300 CLA CLL /CLEAR AC,L
1409 2261 1070 TAD K6000 /GET MISC STATUS 1 TO AC
1410 2262 6151 LMR /SET DATA CHANNEL TO AC
1411 2263 7300 CLA CLL /CLEAR AC,L
1412 2264 6154 XFR /READ DATA
1413 2265 0041 AND K0160 /SAVE DATA CHANNEL BITS
1414 2266 3117 DCA REGC /STORE FOR TYPING
1415 2267 1117 TAD REGC /FETCH
1416 2270 7041 CIA /NEGATE
1417 2271 1041 TAD K0160 /SUBTRACT DATA
1418 2272 7650 SNA CLA /TEST RESULTS
1419 2273 4436 JMS I NERROR /TEST OKAY
1420 2274 4437 LTB000, JMS I ERROR /TEST FAILED
1421 2275 6366 LMM000 /MESSAGE TAG
1422 2276 7402 HLT /ERROR HALT
1423 2277 7610 SKP CLA /EXIT
1424 2300 2231 LTR000 /SCOPE LOOP

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2301 4025
2302 1056
2303 6141
2304 0001
2305 0011
2306 0001
2307 0002
2310 1070
2311 6151
2312 7300
2313 6154
2314 0112
2315 7640
2316 4436
2317 4437
2320 6414
2321 7402
2322 7610
2323 2301

/DOES THE MARK CLOCK GENERATE TIMING

LXA000, JMS TPEPRE
TAD K0200
LINC
AXO
CLR
AXO
PDP
TAD K6000
LMR
CLA CLL
XFR
AND K0010
SZA CLA
JMS I NERROR
JMS I ERROR
LTM000
HLT
SKP CLA
LXA000

/0 TC01, TC02 AND MARK FLOP 0, GP EQ
/GET MARK BIT
/L MODE
/SET MARK FLOP
/CLEAR AC
/CLEAR MARK FLOP
/P MODE
/GET MISC 1 TO AC
/LOAD MAINT REG
/CLEAR AC,L
/READ DATA
/SAVE EQUAL BIT
/TEST IT
/TEST OKAY
/TEST FAILED
/MESSAGE TAG
/ERROR HALT
/EXIT
/SCOPE LOOP

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1448 /
1449 /DOES LC00,01,02 COUNT NORMALLY
1450 /
1451 2324 4025 LTS101, JMS TPEPRE /0 > EVERYTHING
1452 2325 1033 TAD K0016 /SET BLOCK MARK
1453 2326 4434 JMS I LOADR /SET MARK WINDOW TO REVERSE
1454 2327 1110 TAD K0020 /SET UP FOR TP4
1455 2330 6151 LMR /SET LC01,00 TO ONES
1456 2331 7104 CLL RAL /SET AC FOR TP0
1457 2332 6151 LMR /SET LC02 (1)
1458 2333 7110 CLL RAR /SET AC FOR TP1
1459 2334 6151 LMR /LOAD MAINT REG
1460 2335 7300 CLA CLL /CLEAR AC,L
1461 2336 1070 TAD K6000 /SET UP FOR MISC 1
1462 2337 6151 LMR /LOAD MAINT REG
1463 2340 7300 CLA CLL /CLEAR AC,L
1464 2341 6154 XFR /READ DATA
1465 2342 0145 AND K1400 /SAVE LINE COUNTER
1466 2343 3116 DCA REGB /STORE FOR TYPING
1467 2344 1116 TAD REGB /FETCH IT
1468 2345 7650 SNA CLA /TEST
1469 2346 4436 JMS I NERROR /TEST OKAY
1470 2347 4437 JMS I ERROR /TEST FAILED
1471 2350 6440 LTM101 /MESSAGE TAG
1472 2351 7402 HLT /ERROR HALT
1473 2352 7610 SKP CLA /EXIT
1474 2353 2324 LTS101 /SCOPE LOOP

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1482      2354  4025  MOTST1, JMS      TPEPRE      /0 EVERYTHING
1483      2355  4432      JMS I      MAINT1      /SET NO PAUSE AND MAINT FLOP
1484      2356  6141      LINC              /L MODE
1485      2357  0703      0703              /MOVE TOWARD BLOCK
1486      2360  7000      7000              /
1487      2361  0002      PDP              /P MODE
1488      2362  1033      TAD      K0016      /GET BLOCK MARK
1489      2363  4434      JMS I      LOADR      /SET MARK WINDOW TO BLOCK MARK
1490      2364  1035      TAD      K0040      /SET BIT FOR TP0,TP1,TP2
1491      2365  6151      LMR              /LOAD MAINT REGISTER SET TURN AROUND
1492      2366  1043      TAD      K5000      /ADD UNITS + MTN TO AC
1493      2367  6151      LMR              /TRY TO ZERO MOTION
1494      2370  7300      CLA CLL              /CLEAR AC, LINK
1495      2371  6154      XFR              /READ DATA
1496      2372  0112      AND      K0010      /SAVE MOTION FLOP
1497      2373  7650      SNA CLA              /TEST
1498      2374  4436      JMS I      NERROR      /TEST OKAY
1499      2375  4437      JMS I      ERROR      /TEST FAILED
1500      2376  6464      MOTT1M              /MESSAGE TAG
1501      2377  7402      HLT              /ERROR HALT
1502      2400  7610      SKP CLA              /EXIT
1503      2401  2354      MOTST1              /SCOPE LOOP
1504
1505      /
1506      /DOES TAPE PRESET 0 > THE MOTION FLOP
1507
1507      2402  4025  MOTST2, JMS      TPEPRE      /0 > EVERYTHING
1508      2403  4432      JMS I      MAINT1      /SET MAINT AND NO PAUSE
1509      2404  6141      LINC              /L MODE
1510      2405  0700      0700              /SET MOTION FLOP
1511      2406  7000      7000              /
1512      2407  0002      PDP              /P MODE
1513      2410  4025      JMS      TPEPRE      /ATTEMPT TO ZERO MOTION FLOP
1514      2411  1043      TAD      K5000      /GET MTN TO AC
1515      2412  6151      LMR              /LOAD MAINT REGISTER
1516      2413  7300      CLA CLL              /CLEAR AC, L
1517      2414  6154      XFR              /READ DATA
1518      2415  0112      AND      K0010      /SAVE MOTION FLOP
1519      2416  7650      SNA CLA              /TEST
1520      2417  4436      JMS I      NERROR      /TEST OKAY
1521      2420  4437      JMS I      ERROR      /TEST FAILED
1522      2421  6507      MOTT2M              /MESSAGE TAG
1523      2422  7402      HLT              /ERROR HALT
1524      2423  7610      SKP CLA              /EXIT
1525      2424  2402      MOTST2              /SCOPE LOOP

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2425 4025
2426 7240
2427 3115
2430 3116
2431 1071
2432 6151
2433 7330
2434 6154
2435 4432
2436 6141
2437 0703
2440 0000
2441 0002
2442 1033
2443 4434
2444 1035
2445 6151
2446 7300
2447 1043
2450 6151
2451 7300
2452 6154
2453 0112
2454 7650
2455 5261
2456 2116
2457 5244
2460 7610
2461 4436
2462 4437
2463 6532
2464 7402
2465 7610
2466 2425

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/DOES CLR PROGRESS 0 THE MOTION FLOP
/
MOTST3, JMS      TPEPRE      /0 > EVERYTHING
          CLA CMA      /SET AC=7777
          DCA REGA      /SET MONITOR TO 1 CYCLE
          DCA REGB      /0 TIMING
          TAD K1000      /GET AC>TAC
          LMR          /LOAD MAINT REG
          CLA CML CLL RAR /SET AC00
          XFR          /SET TAC=4000
          JMS I   MAINT1    /SET NO PAUSE MAINT
          LINC      /L MODE
          0703      /MTB
          0000      /
          PDP        /P MODE
          TAD K0016    /GET BM
          JMS I   LOADR  /LOAD MARK WINDOW
          TAD K0040    /GEN TP0,TP1,TP2
          LMR          /LOAD MAINT REG
          CLA CLL      /CLEAR AC,L
          TAD K5000    /GET MTN TO AC
          LMR          /LOAD MAINT REG
          CLA CLL      /CLEAR AC,L
          XFR          /READ DATA
          AND K0010    /SAVE MOTION BIT
          SNA CLA      /TEST
          JMP .+4      /OKAY
          ISZ REGB     /DONE YET
          JMP .-13     /WAIT
          SKP CLA      /ERROR
          JMS I   NERROR /TEST OKAY
          JMS I   ERROR  /TEST FAILED
          MOTT3M      /MESSAGE TAG
          HLT
          SKP CLA
          MOTST3
    
```

1564				
1565				
1566			/DOES M113 B24 PINS D2,E2,F2 SHIFT RWB	
1567				
1568	2467	4025	REG004, JMS	TPEPRE /0>EVERYTHING
1569	2470	4432	JMS I	MAINT1 /SET MAINT MODE
1570	2471	7240	CLA CMA	/FETCH A TEST NUMBER
1571	2472	6154	XFR	/SET TB TO (7777)
1572	2473	7300	CLA CLL	/CLEAR AC, L
1573	2474	1071	TAD	K1000 /SET BIT 2, TB TO RWB
1574	2475	6152	TRC	/SET RWB=TB=7777,
1575	2476	7300	CLA CLL	/CLEAR AC, L
1576	2477	1165	TAD	K3427 /SET FOR TP3 AND READ RWB
1577	2500	6151	LMR	/SHIFT RWB
1578	2501	7300	CLA CLL	/CLEAR AC, L
1579	2502	6154	XFR	/READ RWB
1580	2503	3116	DCA	REGB /STORE
1581	2504	7240	CLA CMA	/FETCH TEST DATA
1582	2505	0171	AND	K7356 /SHIFTED? OR MASKED?
1583	2506	3117	DCA	REGC /STORE FOR TYPING
1584	2507	1117	TAD	REGC /FETCH
1585	2510	7041	CIA	/NEGATE
1586	2511	1116	TAD	REGB /SUBTRACT
1587	2512	7650	SNA CLA	/TEST
1588	2513	4436	JMS I	NERROR
1589	2514	4437	JMS I	ERROR
1590	2515	6556	REGM04	
1591	2516	7402	HLT	
1592	2517	7610	SKP CLA	
1593	2520	2467	REG004	
1594				

1505				
1506				
1507				/DOES WRITE SHIFT RWB FUNCTION
1508				
1509	2521	4025	REG006, JMS	TPEPRE /0> EVERYTHING
1600	2522	4432	JMS I	MAINT1 /SET MAINT AND NO PAUSE
1601	2523	7300	CLA CLL	/CLEAR AC, L
1602	2524	1115	TAD	REGA /FETCH DATA SOURCE
1603	2525	7104	CLL RAL	/SHIFT IT
1604	2526	3116	DCA	REGB* /STORE SIMULATION
1605	2527	6141	LINC	/L MODE
1606	2530	0700	0700	/SET IN PROGRESS
1607	2531	0000	0000	
1608	2532	0002	PDP	/P MODE
1609	2533	1112	TAD	K0010 /GET WRITE SYNC BIT
1610	2534	6152	TRC	/SET WRITE SYNC
1611	2535	7300	CLA CLL	
1612	2536	1033	TAD	K0016 /GET BM
1613	2537	4434	JMS I	LOADR /SET WINDOW TO BLOCK MARK
1614	2540	1071	TAD	K1000 /SET AC> TAC
1615	2541	6151	LMR	/LOAD MAINT IR
1616	2542	7240	CLA CMA	/SET AC=7777
1617	2543	6154	XFR	/SET TAC
1618	2544	0055	AND	K0100 /GET FWD BIT
1619	2545	6152	TRC	/SET FWD BIT
1620	2546	7300	CLA CLL	/CLEAR AC, L
1621	2547	1035	TAD	K0040 /SET UP FOR TP0,1,2
1622	2550	6151	LMR	/1 TO BLOCK MODE
1623	2551	7300	CLA CLL	/CLEAR AC, L
1624	2552	1112	TAD	K0010 /SET AC08
1625	2553	6152	TRC	/SET WRITE SYNC
1626	2554	7300	CLA CLL	/CLEAR AC, L
1627	2555	1110	TAD	K0020 /SET UP FOR TP3
1628	2556	6151	LMR	/SET WRITE
1629	2557	7300	CLA CLL	/CLEAR AC, L
1630	2560	1115	TAD	REGA /GET DATA
1631	2561	6154	XFR	/SET TB
1632	2562	7300	CLA CLL	/CLEAR AC, L
1633	2563	1071	TAD	K1000 /GET TB TO RWB
1634	2564	6152	TRC	/SHIFT RWB
1635	2565	7300	CLA CLL	/CLEAR AC, L
1636	2566	1154	TAD	K3440 /PERFORM SHIFT RWB
1637	2567	6151	LMR	/SET RWB TO AC
1638	2570	7300	CLA CLL	/CLEAR AC, L
1639	2571	6154	XFR	/READ RWB
1640	2572	3117	DCA	REGC /STORE DATA
1641	2573	1115	TAD	REGA /FETCH DATA
1642	2574	7041	CIA	/NEGATE
1643	2575	1117	TAD	REGC /SUBTRACT DATA,
1644	2576	7650	SNA CLA	/TEST
1645	2577	4436	JMS I	NERROR /TEST OKAY
1646	2600	4437	JMS I	ERROR /TEST FAILED
1647	2601	4601	REGM06	/MESSAGE
1648	2602	7402	HLT	/ERROR HALT
1649	2603	7610	SKP CLA	/EXIT

/PDP-12 TAPE CONTROL TEST PART II, MAINDEC 12-03GA-L

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1650 2604 2521

REG006

/SCOPE LOOP

1651		/DOES M115 B27 GENERATE LOAD TAC TAC+TB TO TAC
1652	2605 4025	REG009, JMS TPEPRE
1653	2606 4432	JMS I MAINT1
1654	2607 6141	LINC
1655	2610 0707	0707
1656	2611 0000	0000
1657	2612 0002	PDP
1658	2613 1033	TAD K0016
1659	2614 4434	JMS I LOADR
1660	2615 1071	TAD K1000
1661	2616 6151	LMR
1662	2617 7240	CLA CMA
1663	2620 6154	XFR
1664	2621 0055	AND K0100
1665	2622 6152	TRC
1666	2623 7300	CLA CLL
1667	2624 1035	TAD K0040
1668	2625 6151	LMR
1669	2626 4445	JMS I RAN
1670	2627 3116	DCA REGB
1671	2630 1071	TAD K1000
1672	2631 6151	LMR
1673	2632 7300	CLA CLL
1674	2633 1116	TAD REGB
1675	2634 6154	XFR
1676	2635 7300	CLA CLL
1677	2636 6151	LMR
1678	2637 4445	JMS I RAN
1679	2640 7040	CMA
1680	2641 6154	XFR
1681	2642 3117	DCA REGC
1682	2643 1116	TAD REGB
1683	2644 1117	TAD REGC
1684	2645 3114	DCA REGD
1685	2646 1153	TAD K0011
1686	2647 4434	JMS I LOADR
1687	2650 1035	TAD K0040
1688	2651 6151	LMR
1689	2652 4025	JMS TPEPRE
1690	2653 6141	LINC
1691	2654 0003	TAC
1692	2655 0002	PDP
1693	2656 1040	TAD K0002
1694	2657 3046	DCA REGE
1695	2660 1046	TAD REGE
1696	2661 7041	CIA
1697	2662 1114	TAD REGD
1698	2663 7050	SNA CLA
1699	2664 4436	JMS I NERROR
1700	2665 4437	JMS I ERROR
1701	2666 6630	REGM09
1702	2667 7402	HLT
1703	2670 7610	SKP CLA
1704	2671 2605	REG009

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/0>EVERYTHING
/SET MAINT AND NO PAUSE
/L MODE.
/SET IN PROGRESS
/
/P MODE
/GET BM
/SET WINDOW TO BLOCK MARK
/GET AC>TAC
/LOAD MAINT IR
/SET AC=7777
/SET TAC=7777
/SET FWD BIT
/SET DIRECTION TO FORWARD
/CLEAR AC,L
/SET TP0,TP1,TP2
/LOAD MAINT REG 1>BLOCK
/GENERATE A RANDOM NUMBER
/STORE IT
/GET AC>TAC
/SET MAINT REG TO AC>TAC
/CLEAR AC,L
/FETCH RANDOM DATA
/SET UP TAC REGISTER
/CLEAR AC,L
/SET UP AC>TB
/FETCH A NUMBER
/INVERT IT
/SET TB
/STORE IT
/ADD B
/ADD C SIMULATE THE ADDITION
/STORE SIMULATED ADDITION
/GET DM
/SET MARK WINDOW TO DATA MARK
/GENERATE TP0
/TB+TAC TO TAC
/0 PROGRESS
/L MODE
/READ TAC
/P MODE
/ADD TWO FOR CORRECTION.
/STORE IT
/FETCH IT
/NEGATE
/SUBTRACT DATA SOURCE
/TEST
/TEST OKAY
/TEST FAILED
/MESSAGE TAG
/ERROR HALT
/EXIT
/SCOPE LOOP

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1759

2672 4025

2673 4432

2674 6141

2675 0700

2676 0000

2677 0002

2700 4434

2701 1035

2702 6151

2703 7300

2704 1071

2705 6151

2706 7240

2707 6154

2710 0110

2711 6151

2712 7300

2713 6141

2714 0003

2715 0002

2716 3116

2717 1116

2720 7650

2721 4436

2722 4437

2723 6652

2724 7402

2725 7610

2726 2672

/DOES M121, B25 PINS F1, H1, L1 GENERATE LOAD TAC

REG012, JMS TPEPRE

JMS I MAINT1

LINC

0700

0000

PDP

JMS I LOADR

TAD K0040

LMR

CLA CLL

TAD K1000

LMR

CLA CMA

XFR

AND K0020

LMR

CLA CLL

LINC

TAC

PDP

DCA REGB

TAD REGB

SNA CLA

JMS I NERROR

JMS I ERROR

REGM12

HLT

SKP CLA

REG012

/TEST WRITE CYCLE FLOP

WRCFLP, JMS TPEPRE

JMS I MAINT1

LINC

0700

7000

PDP

TAD K4440

LMR

CLA CLL

XFR

AND K0020

SNA CLA

JMP I PNTB

TAD K1000

LMR

CLA CMA

XFR

AND K0016

JMS I LOADR

/2>EVERYTHING

/SET MAINT AND NO PAUSE

/L MODE

/SET IN PROGRESS

/P MODE

/WIPE OUT WINDOW

/GEN TP0, TP1, TP2

/LOAD MAINT REG 1>SEARCH

/CLEAR AC, L

/SET AC>TAC

/LOAD MAINT REG

/SET AC=7777

/SET TAC=7777

/SET UP FOR TP3, TP4

/CLEAR TAC

/CLEAR AC, L

/L MODE

/READ TAC

/P MODE

/STORE FOR TYPING

/FETCH IT

/TEST

/TEST OKAY

/TEST FAILED

/MESSAGE TAG

/ERROR HALT

/EXIT

/SCOPE LOOP

/2> EVERYTHING

/SET MAINT AND NO PAUSE

/L MODE

/SET WRITE CYCLE

/WASTED MEMORY

/P MODE

/GET ENABLE STATES TO AC SET GP EQ GFC

/LOAD MAINT REGISTER

/CLEAR AC, L

/READ STATUS

/SAVE WRITE CYCLE FLOP

/WAS IT SET

/TROUBLE (GO TO WRCFLB)

/SET AC> TAC

/LOAD MAINT REG

/SET AC=7777

/SET TAC=7777

/SET BM

/SET WINDOW TO BLOCK MARK

ADDP-12 TAPE CONTROL TEST PART III. MAINBEC 12-0354-1 PALLIZ V1341 24-SEP-78 124625 PAGE 4741
17600 2752 1055 TAD K0100 /SET FWD BIT

1761	2753	6152	TRC	/SET FORWARD FLOP
1762	2754	7300	CLA CLL	/CLEAR AC,L
1763	2755	1035	TAD K0040	/GENERATE TP0, TP1, TP2 1> SEARCH
1764	2756	6151	LMR	/1> BLOCK MODE
1765	2757	7300	CLA CLL	/CLEAR AC,L
1766	2760	4434	JMS I LOADR	/0> WINDOW
1767	2761	1035	TAD K0040	/GENERATE TP0
1768	2762	6151	LMR	/TP0, TP1, TP2
1769	2763	7301	CLA CLL IAC	/SET CM
1770	2764	4434	JMS I LOADR	/SET MARK WINDOW TO CM
1771	2765	1122	TAD K4440	/GENERATE TP0, 1, 2
1772	2766	6151	LMR	/SET CHK WRD
1773	2767	6151	LMR	/0> WRITE CYCLE
1774	2770	7300	CLA CLL	/CLEAR AC,L
1775	2771	6154	XFR	/READ STATUS
1776	2772	0110	AND K0020	/SAVE WRITE CYCLE
1777	2773	7640	SEA CLA	/WAS IT ZEROED
1778	2774	5461	JMP I PNTB	/TROUBLE (GO TO WRCFLB)
1779	2775	1033	TAD K0016	/WILL WRITE CYCLE STAY ZEROED
1780	2776	4434	JMS I LOADR	/SET WINDOW TO BM
1781	2777	1055	TAD K0100	/SET FORWARD BIT
1782	3000	6152	TRC	/SET FORWARD FLOP
1783	3001	7300	CLA CLL	/CLEAR AC,L
1784	3002	1035	TAD K0040	/GENERATE TP0, 1, 2 1> SEARCH
1785	3003	6151	LMR	/LOAD MAINT REG
1786	3004	7300	CLA CLL	/CLEAR AC,L
1787	3005	1071	TAD K1000	/GET AC> TAC
1788	3006	6151	LMR	/LOAD MAINT REG
1789	3007	7240	CLA CHA	/SET AC=7777
1790	3010	6154	XFR	/SET TAC
1791	3011	7300	CLA CLL	/CLEAR AC,L
1792	3012	4434	JMS I LOADR	/0> WINDOW
1793	3013	1035	TAD K0040	/GENERATE TP0
1794	3014	6151	LMR	/TP0, 1, 2
1795	3015	7301	CLA CLL IAC	/SET CM
1796	3016	4434	JMS I LOADR	/SET MARK WINDOW TO CM
1797	3017	1122	TAD K4440	/GENERATE TP0, 1, 2
1798	3020	6151	LMR	/SET CHK WRD
1799	3021	6151	LMR	/KEEP WRITE CYCLE 0
1800	3022	7300	CLA CLL	/CLEAR AC,L
1801	3023	6154	XFR	/READ STATUS
1802	3024	0110	AND K0020	/SAVE WRITE CYCLE
1803	3025	7650	SNA CLA	/DID IT SET IN ERROR
1804	3026	4436	JMS I NERROR	/NO TROUBLE
1805	3027	4437	JMS I ERROR	/TROUBLE
1806	3030	6712	WRCM	/MESSAGE
1807	3031	7402	HLT	/ERROR HALT
1808	3032	7610	SKP CLA	/EXIT
1809	3033	2727	WRCFLP	/SCOPE LOOP

WRCFLB,


```

1810 /
1811 /TEST TIMING OKAY GATE
1812 /
1813 3034 1033 TTOK1, TAD K0016 /GET BM
1814 3035 4434 JMS I LOADR /SET WINDOW
1815 3036 4025 JMS TPEPRE /0> MAINT, 0> MARK
1816 3037 1112 TAD K0010 /SET NO PAUSE MODE
1817 3040 6141 LINC /L MODE
1818 3041 0001 AXO /SET NO PAUSE
1819 3042 0700 0700 /SET MOTION
1820 3043 7000 7000
1821 3044 0002 PDP /P MODE
1822 3045 7240 CLA CMA /SET AC=7777
1823 3046 3115 DCA REGA /SET MONITOR TO DO ONE CYCLE.
1824 3047 3116 DCA REGB /0> TIMING REGISTER
1825 3050 1054 TAD K7770
1826 3051 3117 DCA REGC
1827 3052 1053 TAD K4140 /GEN TIMING FOR TTOK
1828 3053 6151 LMR /LOAD MAINT REG
1829 3054 7300 CLA CLL /CLEAR AC,L
1830 3055 6154 XFR /READ
1831 3056 0040 AND K0002 /SAVE TTOK
1832 3057 7640 SZA CLA /TEST
1833 3060 5266 JMP ,+6 /TEST OKAY
1834 3061 2116 ISZ REGB /WAIT
1835 3062 5252 JMP ,+10 /WAIT
1836 3063 2117 ISZ REGC /WAIT SOME MORE
1837 3064 5262 JMP ,+2 /WAIT
1838 3065 7610 SKP CLA /INVENT SKIP
1839 3066 4436 JMS I NERROR /TEST OKAY
1840 3067 4437 JMS I ERROR /TEST FAILED
1841 3070 6734 TTOKM /MESSAGE TAG
1842 3071 7402 HLT /ERROR HALT
1843 3072 7610 SKP CLA /EXIT
1844 3073 3034 TTOK1 /SCOPE LOOP
1845 /
1846 /TAPE TRAP TEST
1847 /
1848 3074 7300 TPTRAP, CLA CLL /0> AC,L
1849 3075 3140 DCA 140 /0 TRAP LOCATION
1850 3076 1145 TAD K1400 /SET INST AND TAPE TRAP
1851 3077 6141 LINC /L MODE
1852 3100 0004 ESF /SET SPECIAL FUNCTION
1853 3101 0700 0700 /TRY AND TRAP THIS
1854 3102 7000 7000
1855 3103 0002 PDP
1856 3104 5314 JMP TPTRBD /P MODE
1857 3105 7300 LOCTRP, CLA CLL /NO TRAP, BLUNDER.
1858 3106 6141 LINC /RETURN HERE FROM TRAP,
1859 3107 0004 ESF /L MODE
1860 3110 0002 PDP /0 SPEC FUN
1861 3111 1140 TAD 140 /P MODE
1862 3112 7640 SZA CLA /FETCH PROGRAM COUNTER,
1863 3113 4436 JMS I NERROR /WAS IT SET
1864 3114 4437 TPTRBD, JMS I ERROR /TEST OKAY
/TEST FAILED

```

1865	3115	7012	TRAPH	/MESSAGE TAG
1866	3116	7402	HLT	/ERROR HALT
1867	3117	7610	SKP CLA	/EXIT
1868	3120	3074	TPTRAP	/SCOPE LOOP
1869				
1870			/GRAND FINAL END	
1871				
1872	3121	4025	JMS TPEPRE	/0 EVERYTHING
1873	3122	2065	ISZ PASS	
1874	3123	7000	NOP	
1875	3124	7604	LAS	
1876	3125	0035	AND K0040	
1877	3126	7640	SZA CLA	
1878	3127	5177	JMP 177	/START OVER
1879	3130	1063	TAD PNTJ	
1880	3131	3437	DCA I ERROR	
1881	3132	5464	JMP I OUTPAS	
1882	3133	6676	LOCJ, PASSH	

1883							
1884	3134	0000	MAINTS,	0000			/RETURN ADDRESS STORAGE
1885	3135	7200		CLA			/CLEAR AC, L
1886	3136	1107		TAD	K0050		/SET MAINT, NO PAUSE
1887	3137	6141		LINC			/L MODE
1888	3140	0001		AXO			/LOAD EXTENDED ORS
1889	3141	0002		PDP			/P MODE
1890	3142	7200		CLA			/CLEAR AC, L
1891	3143	5734		JMP I	MAINTS		/EXIT
1892							
1893	3144	0000	LOADS,	0000			/RETURN ADDRESS STORAGE
1894	3145	7110		RAR	CLL		/WORD TO BE LOADED IS MOVED RIGHT ONE BIT
1895	3146	3113		DCA	TEMPB		/STORE IT
1896	3147	1110		TAD	K0020		/GET REV BIT
1897	3150	6152		TRC			/SET REVERSE
1898	3151	7200		CLA			/CLEAR AC, L
1899	3152	4432		JMS I	MAINT1		/SET MAINTENANCE BIT
1900	3153	1111		TAD	K7773		/SET AC=7773
1901	3154	3334		DCA	MAINTS		/SET TALLY TO MINUS 5
1902	3155	1113	DOMORE,	TAD	TEMPB		/GET STORED DATA
1903	3156	0112		AND	K0010		/SAVE CURRENT DATA BIT
1904	3157	3025		DCA	TPEPRE		/STORE IT
1905	3160	1025		TAD	TPEPRE		/FETCH IT
1906	3161	7040		CMA			/INVERT IT
1907	3162	0110		AND	K0020		/AND IN COMMAND BIT
1908	3163	1025		TAD	TPEPRE		/ADD IN LOADING BIT
1909	3164	6151		LMR			/SEND IT
1910	3165	7200		CLA			/CLEAR AC
1911	3166	1113		TAD	TEMPB		/MOVE NEXT MOST SIGNIFICANT
1912	3167	7004		RAL			/DATA BIT INTO LINK
1913	3170	3113		DCA	TEMPB		/STORE IT BACK
1914	3171	2334		ISZ	MAINTS		/DONE YET
1915	3172	5355		JMP	DOMORE		/NOT DONE YET
1916	3173	5744		JMP I	LOADS		/EXIT

```

1917
1918          5000      *5000
1919          /
1920          /NON ERROR MONITOR DETERMINES IF OPERATOR WANTS TO LOOP ON NON FAILING TEST
1921          NERROS, 0      /RETURN ADDRESS
1922          5001      4432      JMS I      MAINT1      /SET MAINTENANCE FLAG
1923          5002      7307      CLA CLL IAC RTL      /SET AC = 4
1924          5003      1200      TAD          NERROS      /GET RETURN ADDRESS
1925          5004      3200      DCA          NERROS      /UPDATE RETURN ADDRESS
1926          5005      1600      TAD I      NERROS      /GET SCOPE LOOP ADDRESS
1927          5006      3221      DCA          ERRORS      /STORE IT
1928          5007      2115      ISZ          REGA      /UPDATE DATA
1929          5010      5621      JMP I      ERRORS      /EXIT
1930          5011      7604      LAS          /READ SWITCHES
1931          5012      0072      AND          K0400      /SAVE SR3
1932          5013      7640      SZA CLA      /TEST AND CLEAR
1933          5014      5621      JMP I      ERRORS      /LOOPING
1934          5015      7040      CMA          /SET AC=-1
1935          5016      1200      TAD          NERROS      /ADD NERROS
1936          5017      3200      DCA          NERROS      /STORE IN NERROS
1937          5020      5600      JMP I      NERROS      /JUMP INDIRECT LOOP
1938          /
1939          /ERROR PROCESSOR, SCOPE LOOP, HALT, PRINT
1940          ERRORS, 0      /RETURN ADDRESS STORAGE
1941          5021      0000      LAS          /READ SWITCHES
1942          5022      7604      RAL          /MOVE SR1 INTO AC20
1943          5023      7004      SMA CLA      /IS IT SET
1944          5024      7700      JMP          ASCII      /NO TYPE A MESSAGE
1945          5025      5254      JMS I      BELLA      /RING THE BELL
1946          5026      4503      ASCRXT, TAD      ERRORS      /GET CURRENT ERROR ADDRESS
1947          5027      1221      CIA          /INVERT IT
1948          5030      7041      DCA          LSTERR      /STORE IN LAST ERROR
1949          5031      3024      ISZ          ERRORS      /YES INDEX ESCAPE
1950          5032      2221      LAS          /READ SWITCHES
1951          5033      7604      SMA CLA      /IS SR2 SET
1952          5034      7700      JMP I      ERRORS      /NO JUMP TO ERROR HALT
1953          5035      5621      ISZ          ERRORS      /YES INDEX ESCAPE TO JUMP OUT
1954          5036      2221      ISZ          ERRORS      /INDEX ERRORS TO SCOPE MODE
1955          5037      2221      TAD I      ERRORS      /GET SXOPE ADDRESS
1956          5040      1621      DCA          NERROS      /STORE IN TYPE
1957          5041      3200      LAS          /READ SWITCHES
1958          5042      7604      RTL          /MOVE SR02 TO AC0
1959          5043      7006      SPA CLA      /IS SCOPE MODE SELECTED
1960          5044      7710      JMP I      NERROS      /YES CONTINUE IN SCOPE LOOP
1961          5045      5600      ISZ          REGA      /UPDATE DATA
1962          5046      2115      JMP I      NERROS      /TEST WITH NEW DATA
1963          5047      5600      CMA          /NO SET AC=7777
1964          5050      7040      TAD          ERRORS      /SUBTRACT ONE FROM ERRORS
1965          5051      1221      DCA          ERRORS      /STORE SELECTED ADDRESS
1966          5052      3221      JMP I      ERRORS      /EXIT TO NEXT TEST
1967          5053      5621

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1967					
1968	5054	7240	ASCII,	CLA CMA	/SET C(AC)=-1
1969	5055	1621		TAD I ERRORS	/GET MESSAGE ADDRESS STORAGE
1970	5056	3010		DCA PINT	/STORE IT IN AUTO INDEX REGISTER
1971	5057	1221		TAD ERRORS	/GET RETURN ADDRESS
1972	5060	1024		TAD LSTERR	/SUBTRACT LAST ERROR ADDRESS
1973	5061	7650		SNA CLA	/TEST
1974	5062	5366		JMP DATYP	/SAME GO TYPE DATA
1975	5063	1410		TAD I PINT	/GET FIRST CHARACTER
1976	5064	3200		DCA NERROS	/SAVE IT
1977	5065	1200		TAD NERROS	/GET IT
1978	5066	7450		SNA	/TEST IT
1979	5067	5227		JMP ASCRXT	/NUMBER=EXIT
1980	5070	7040		CMA	/INVERT IT
1981	5071	7450		SNA	/NUMBER=EXITA
1982	5072	5320		JMP DATUM	/TYPE OUT DATA ROUTINE
1983	5073	7040		CMA	/CHANGE IT BACK
1984	5074	7112		RTR CLL	/SWAP AC TO THE RIGHT
1985	5075	7012		RTR	/MOVE
1986	5076	7012		RTR	/MOVE
1987	5077	4303		JMS TYPECH	/TYPE IT
1988	5100	1200		TAD NERROS	/GET IT AGAIN
1989	5101	4303		JMS TYPECH	/TYPE IT
1990	5102	5263		JMP ASCII+7	/MUST BE MORE WORDS THAT NEED TYPING
1991	5103	0000	TYPECH,	0	
1992	5104	0073		AND K0077	/SAVE SIGNIFICANT PART
1993	5105	3106		DCA SPACE	/STORE WORD
1994	5106	1106		TAD SPACE	/FETCH IT
1995	5107	7650		SNA CLA	/TEST FOR 00 CRLF CODE
1996	5110	4357		JMS CRLF	/YES IT WAS
1997	5111	1106		TAD SPACE	/NO TYPE IT
1998	5112	1074		TAD M40	/SUBTRACT 40
1999	5113	7510		SPA	/TEST POLARITY
2000	5114	1055		TAD K0100	/ADD 340
2001	5115	1075		TAD K240	/ADD 240
2002	5116	4505		JMS I TYPE	/TYPE
2003	5117	5703		JMP I TYPECH	/EXIT
2004					
2005	5120	1410	DATUM,	TAD I PINT	/GET ADDRESS OF REGISTER
2006	5121	3200		DCA NERROS	/STORE IN TEMP
2007	5122	1200		TAD NERROS	/GET TEMP
2008	5123	7650		SNA CLA	/TEST FOR EXIT
2009	5124	5227		JMP ASCRXT	/EQUALS 0000 EXIT
2010	5125	1200		TAD NERROS	
2011	5126	1052		TAD M4444	
2012	5127	7650		SNA CLA	/S3?
2013	5130	5177		JMP 177	
2014	5131	1600		TAD I NERROS	/GET DATA
2015	5132	4336		JMS OCTYP	/TYPE IT
2016	5133	1075		TAD K240	/SPACE
2017	5134	4505		JMS I TYPE	/TYPE IT
2018	5135	5320		JMP DATUM	/TYPE NUMERIC DATA
2019	5136	0000	OCTYP,	0	/RETURN ADDRESS STORAGE
2020	5137	3303		DCA TYPECH	/STORE DATA TO BE PRINTED
2021	5140	1076		TAD K7774	/SET UP TALLY

/POP-12 TAPE CONTROL TEST PART II, MAINDEC 12-D3GA-L PAL10 V141 24-SEP-74 15:55 PAGE 52-1

2022 5141 3106 DCA SPACE /SET IT

2023						
2024			/TAPE 9			
2025			/			
2026	5142	1077	HERE,	TAD	K1026	/GET FLAG NUMBER
2027	5143	3357	REDO,	DCA	CRLF	/STORE
2028	5144	1303		TAD	TYPECH	
2029	5145	7004		RAL		
2030	5146	3303		DCA	TYPECH	
2031	5147	1357		TAD	CRLF	
2032	5150	7004		RAL		
2033	5151	7420		SNL		
2034	5152	5343		JMP	REDO	
2035	5153	4505		JMS I	TYPE	
2036	5154	2106		ISZ	SPACE	
2037	5155	5342		JMP	HERE	
2038	5156	5736		JMP I	OCTYP	
2039	5157	0000	CRLF,			/EXIT
2040	5160	1100		TAD	K0215	/RETURN ADDRESS STORAGE
2041	5161	4505		JMS I	TYPE	/GET CR
2042	5162	1101		TAD	K0212	/TYPE IT
2043	5163	4505		JMS I	TYPE	/GET LF
2044	5164	1102		TAD	K0177	/TYPE IT
2045	5165	5757		JMP I	CRLF	/SET TO RUBOUT
2046	5166	1410		JMP		/EXIT
2047	5167	7450	DATYP,	TAD I	PINT	/GET A TERM OFF OF TYPE LIST
2048	5170	5227		SNA		/END OF LIST?
2049	5171	7040		JMP	ASCRXT	/YES EXIT
2050	5172	7640		CMA		/INVERT
2051	5173	5366		SZA CLA		/BEGINNING OF DATA
2052	5174	4357		JMP	DATYP	/NO
2053	5175	7300		JMS	CRLF	/YES OK RETURN THE TTY CARRIAGE AND LINE FEED
2054	5176	5320		CLA CLL		/CLEAR AC AND LINK
				JMP	DATUM	/GO TYPE THE DATA

2055				
2056		5200	*5200	
2057	5200	0000	BELL,	0000
2058	5201	7604	LAS	
2059	5202	0055	AND	K0100
2060	5203	7640	SEA CLA	
2061	5204	5600	JMP I	BELL
2062	5205	1104	TAD	K0207
2063	5206	4505	JMS I	TYPE
2064	5207	5600	JMP I	BELL
2065	5210	0000	TYPOUT,	0000
2066	5211	6046		6046
2067	5212	6041		6041
2068	5213	5212	JMP	, -1
2069	5214	7200	CLA	
2070	5215	5610	JMP I	TYPOUT
2071				
2072	5216	0000	RANDOM,	0000
2073	5217	1166	TAD	RNA
2074	5220	1167	TAD	RNB
2075	5221	3166	DCA	RNA
2076	5222	7004	RAL	
2077	5223	1166	TAD	RNA
2078	5224	1167	TAD	RNB
2079	5225	3167	DCA	RNB
2080	5226	7004	RAL	
2081	5227	1166	TAD	RNA
2082	5230	3166	DCA	RNA
2083	5231	1167	TAD	RNB
2084	5232	5616	JMP I	RANDOM
2085	5233	0014	LIM001,	0014
2086	5234	1120		1120
2087	5235	4015		4015
2088	5236	2420		2420
2089	5237	4023		4023
2090	5240	0524		0524
2091	5241	2520		2520
2092	5242	4006		4006
2093	5243	0111		0111
2094	5244	1405		1405
2095	5245	0440		0440
2096	5246	2417		2417
2097	5247	4003		4003
2098	5250	1405		1405
2099	5251	0122		0122
2100	5252	4024		4024
2101	5253	0120		0120
2102	5254	0540		0540
2103	5255	0417		0417
2104	5256	1605		1605
2105	5257	4000		4000
2106	5260	0000	EXIT	

/READ SWITCHES
 /SAVE SR05
 /IS BELL SUPPRESS SET
 /YES EXIT
 /GET BELL
 /TYPE IT
 /EXIT

/LIP MTP SETUP FAILED TO CLEAR TAPE DONE

2107				
2108	5261	0014	LIM002, 0014	/LIP TAPE PRESET FAILED TO CLEAR TAPE DONE
2109	5262	1120		
2110	5263	4024		
2111	5264	0120		
2112	5265	0540		
2113	5266	2022		
2114	5267	0523		
2115	5270	0524		
2116	5271	4006		
2117	5272	0111		
2118	5273	1405		
2119	5274	0440		
2120	5275	2417		
2121	5276	0314		
2122	5277	0501		
2123	5300	2240		
2124	5301	2401		
2125	5302	2005		
2126	5303	4004		
2127	5304	1716		
2128	5305	0500		
2129	5306	0000		
2130	5307	0014	LIM003, 0014	/LIP CLEAR TAPE DONE FAILED
2131	5310	1120		
2132	5311	4003		
2133	5312	1405		
2134	5313	0122		
2135	5314	4024		
2136	5315	0120		
2137	5316	0540		
2138	5317	0417		
2139	5320	1605		
2140	5321	4006		
2141	5322	0111		
2142	5323	1405		
2143	5324	0400		
2144	5325	0000		

2145			
2146	5326	0014	LIM004, 0014
2147	5327	1120	1120
2148	5330	4023	4023
2149	5331	2404	2404
2150	5332	4006	4006
2151	5333	0111	0111
2152	5334	1405	1405
2153	5335	0440	0440
2154	5336	2401	2401
2155	5337	2005	2005
2156	5340	4004	4004
2157	5341	1716	1716
2158	5342	0575	0575
2159	5343	6100	6100
2160	5344	0000	EXIT
2161	5345	0014	LIM005, 0014
2162	5346	1120	1120
2163	5347	4023	4023
2164	5350	2404	2404
2165	5351	4006	4006
2166	5352	0111	0111
2167	5353	1405	1405
2168	5354	0440	0440
2169	5355	2401	2401
2170	5356	2005	2005
2171	5357	4004	4004
2172	5360	1716	1716
2173	5361	0575	0575
2174	5362	6000	6000
2175	5363	0000	EXIT

/LIP STD FAILED TAPE DONE=1

/LIP STD FAILED TAPE DONE=0

2176			
2177	5364	0014	LIM006, 0014
2178	5365	1120	1120
2179	5366	4024	4024
2180	5367	0120	0120
2181	5370	0540	0540
2182	5371	1116	1116
2183	5372	2405	2405
2184	5373	2222	2222
2185	5374	2520	2520
2186	5375	2440	2440
2187	5376	0601	0601
2188	5377	1114	1114
2189	5400	0504	0504
2190	5401	4011	4011
2191	5402	1624	1624
2192	5403	4005	4005
2193	5404	1602	1602
2194	5405	7561	7561
2195	5406	4000	4000
2196	5407	0000	EXIT
2197	5410	0014	LIM007, 0014
2198	5411	1120	1120
2199	5412	4015	4015
2200	5413	2420	2420
2201	5414	4023	4023
2202	5415	0524	0524
2203	5416	2520	2520
2204	5417	4006	4006
2205	5420	0111	0111
2206	5421	1405	1405
2207	5422	0424	0424
2208	5423	1740	1740
2209	5424	2305	2305
2210	5425	2440	2440
2211	5426	1116	1116
2212	5427	5520	5520
2213	5430	2217	2217
2214	5431	0722	0722
2215	5432	0523	0523
2216	5433	2300	2300
2217	5434	0000	EXIT

/LIP TAPE INTERRUPT FAILED INT ENB=1

/LIP MTP SETUP FAILED TO SET IN-PROGRESS

2218			
2219	5435	0014	LIM008, 0014
2220	5436	1120	1120
2221	5437	4024	4024
2222	5440	0120	0120
2223	5441	0540	0540
2224	5442	2022	2022
2225	5443	0523	0523
2226	5444	0524	0524
2227	5445	4006	4006
2228	5446	0111	0111
2229	5447	1405	1405
2230	5450	0440	0440
2231	5451	2417	2417
2232	5452	4032	4032
2233	5453	0522	0522
2234	5454	1740	1740
2235	5455	1116	1116
2236	5456	4020	4020
2237	5457	2217	2217
2238	5460	0722	0722
2239	5461	0523	0523
2240	5462	2300	2300
2241	5463	0000	EXIT
2242	5464	0014	LIM009, 0014
2243	5465	1120	1120
2244	5466	4050	4050
2245	5467	1403	1403
2246	5470	2350	2350
2247	5471	1524	1524
2248	5472	0252	0252
2249	5473	0215	0215
2250	5474	5223	5223
2251	5475	0501	0501
2252	5476	2203	2203
2253	5477	1051	1051
2254	5500	4006	4006
2255	5501	0111	0111
2256	5502	1405	1405
2257	5503	0440	0440
2258	5504	2417	2417
2259	5505	4060	4060
2260	5506	4011	4011
2261	5507	1640	1640
2262	5510	2022	2022
2263	5511	1707	1707
2264	5512	2205	2205
2265	5513	2323	2323
2266	5514	4000	4000
2267	5515	0000	EXIT

/LIP IAPRESET FAILED TO ZERO IN PROGRESS

/LIP (LCS(MTB*BM*SEARCH) FAILED TO ZERO IN PROGRESS

2268			
2269	5516	0014	LIM010, 0014
2270	5517	1120	1120
2271	5520	4015	4015
2272	5521	6161	6161
2273	5522	6540	6540
2274	5523	0362	0362
2275	5524	6540	6540
2276	5525	2011	2011
2277	5526	1640	1640
2278	5527	2362	2362
2279	5530	4006	4006
2280	5531	0111	0111
2281	5532	1405	1405
2282	5533	0440	0440
2283	5534	2417	2417
2284	5535	4060	4060
2285	5536	2022	2022
2286	5537	1707	1707
2287	5540	2205	2205
2288	5541	2323	2323
2289	5542	4000	4000
2290	5543	0000	EXIT

/LIP M115 C25 PIN S2 FAILED TO 0 IN PROGRESS

2291			
2292	5544	0014	LIM013, 0014
2293	5545	1120	1120
2294	5546	4003	4003
2295	5547	1013	1013
2296	5550	4017	4017
2297	5551	1340	1340
2298	5552	0601	0601
2299	5553	1114	1114
2300	5554	0504	0504
2301	5555	4024	4024
2302	5556	1740	1740
2303	5557	6040	6040
2304	5560	1116	1116
2305	5561	4020	4020
2306	5562	2217	2217
2307	5563	0722	0722
2308	5564	0523	0523
2309	5565	2300	2300
2310	5566	0000	EXIT
2311	5567	0014	LIM015, 0014
2312	5570	1120	1120
2313	5571	4003	4003
2314	5572	1013	1013
2315	5573	4017	4017
2316	5574	1340	1340
2317	5575	0601	0601
2318	5576	1114	1114
2319	5577	0504	0504
2320	5600	4024	4024
2321	5601	1740	1740
2322	5602	6040	6040
2323	5603	2022	2022
2324	5604	1707	1707
2325	5605	2205	2205
2326	5606	2323	2323
2327	5607	4000	4000
2328	5610	0000	EXIT

/LIP CHK OK FAILED TO 0 IN PROGRESS

/LIP CHK OK FAILED TO 0 PROGRESS

2329			
2330	5611	0014	LIM017, 0014
2331	5612	1120	1120
2332	5613	4015	4015
2333	5614	6161	6161
2334	5615	6340	6340
2335	5616	0361	0361
2336	5617	6640	6640
2337	5620	1061	1061
2338	5621	4027	4027
2339	5622	2211	2211
2340	5623	2405	2405
2341	5624	4003	4003
2342	5625	3103	3103
2343	5626	1405	1405
2344	5627	4050	4050
2345	5630	6051	6051
2346	5631	4006	4006
2347	5632	0111	0111
2348	5633	1405	1405
2349	5634	0440	0440
2350	5635	2417	2417
2351	5636	4060	4060
2352	5637	4011	4011
2353	5640	1640	1640
2354	5641	2022	2022
2355	5642	1707	1707
2356	5643	2205	2205
2357	5644	2323	2323
2358	5645	4000	4000
2359	5646	0000	EXIT
2360	5647	0014	LIM018, 0014
2361	5650	1120	1120
2362	5651	4023	4023
2363	5652	2427	2427
2364	5653	4006	4006
2365	5654	0111	0111
2366	5655	1405	1405
2367	5656	0440	0440
2368	5657	2401	2401
2369	5660	2005	2005
2370	5661	4027	4027
2371	5662	1722	1722
2372	5663	0475	0475
2373	5664	6100	6100
2374	5665	0000	EXIT
2375	5666	0014	LIM019, 0014
2376	5667	1120	1120
2377	5670	4023	4023
2378	5671	2427	2427
2379	5672	4006	4006
2380	5673	0111	0111
2381	5674	1405	1405
2382	5675	0440	0440
2383	5676	2401	2401

/LIP M113,C16,H1 WRITE CYCLE (0) FAILED TO 0 IN PROGRESS

/LIP STW FAILED TAPE WORD =1

/LIP STW FAILED TAPE WORD =2

2384	5677	2005	2005
2385	5700	4027	4027
2386	5701	1722	1722
2387	5702	0475	0475
2388	5703	6000	6000
2389	5704	0000	EXIT

2390					
2391	5705	0014	LIM022,	0014	/LIP TAPE WORD TOGGLES FAILED
2392	5706	1120		1120	
2393	5707	4024		4024	
2394	5710	0120		0120	
2395	5711	0540		0540	
2396	5712	2717		2717	
2397	5713	2204		2204	
2398	5714	4024		4024	
2399	5715	1707		1707	
2400	5716	0714		0714	
2401	5717	0523		0523	
2402	5720	4006		4006	
2403	5721	0111		0111	
2404	5722	1405		1405	
2405	5723	0400		0400	
2406	5724	0000		EXIT	
2407					
2408	5725	0014	LIM023,	0014	/LIP DATA BREAK FAILED
2409	5726	1120		1120	/0000 0000 0000
2410	5727	4004		4004	
2411	5730	0124		0124	
2412	5731	0140		0140	
2413	5732	0222		0222	
2414	5733	0501		0501	
2415	5734	1340		1340	
2416	5735	0601		0601	
2417	5736	1114		1114	
2418	5737	0504		0504	
2419	5740	4000		4000	
2420	5741	7777		EXITA	
2421	5742	0116		REGB	
2422	5743	0117		REGC	
2423	5744	0114		REGD	
2424	5745	0000		EXIT	
2425					
2426	5746	0014	LCM000,	0014	/LCX MARK FLOP
2427	5747	0330		0330	/0000 0000
2428	5750	4015		4015	
2429	5751	0122		0122	
2430	5752	1340		1340	
2431	5753	0614		0614	
2432	5754	1720		1720	
2433	5755	4000		4000	
2434	5756	7777		EXITA	
2435	5757	0116		REGB	
2436	5760	0117		REGC	
2437	5761	0000		EXIT	
2438	5762	0014	LCM001,	0014	/LCX MARK FLOP TAPE PRESET FAILED
2439	5763	0330		0330	/0000
2440	5764	4015		4015	
2441	5765	0122		0122	
2442	5766	1340		1340	
2443	5767	0614		0614	
2444	5770	1720		1720	

2445	5771	4024	4024
2446	5772	0120	0120
2447	5773	0540	0540
2448	5774	2022	2022
2449	5775	0523	0523
2450	5776	0524	0524
2451	5777	4006	4006
2452	6000	0111	0111
2453	6001	1405	1405
2454	6002	0400	0400
2455	6003	7777	EXITA
2456	6004	0116	REGB
2457	6005	0000	EXIT
2458	6006	0014	LIM000, 0014
2459	6007	1120	1120
2460	6010	4024	4024
2461	6011	0120	0120
2462	6012	0540	0540
2463	6013	0417	0417
2464	6014	1605	1605
2465	6015	4006	4006
2466	6016	0111	0111
2467	6017	1405	1405
2468	6020	0440	0440
2469	6021	2417	2417
2470	6022	4023	4023
2471	6023	0524	0524
2472	6024	0000	EXIT

/LIP TAPE DONE FAILED TO SET

2473			
2474	6025	0014	LIN012, 0014
2475	6026	1120	1120
2476	6027	4005	4005
2477	6030	1604	1604
2478	6031	4011	4011
2479	6032	1623	1623
2480	6033	2440	2440
2481	6034	0601	0601
2482	6035	1114	1114
2483	6036	0504	0504
2484	6037	4024	4024
2485	6040	1740	1740
2486	6041	6040	6040
2487	6042	2022	2022
2488	6043	1707	1707
2489	6044	2205	2205
2490	6045	2323	2323
2491	6046	0000	EXIT
2492	6047	0014	LINMX1, 0014
2493	6050	1116	1116
2494	6051	4024	4024
2495	6052	0103	0103
2496	6053	7567	7567
2497	6054	6767	6767
2498	6055	6740	6740
2499	6056	0411	0411
2500	6057	2275	2275
2501	6060	2205	2205
2502	6061	2640	2640
2503	6062	0601	0601
2504	6063	1114	1114
2505	6064	0504	0504
2506	6065	0000	EXIT
2507	6066	0014	LINMX2, 0014
2508	6067	1116	1116
2509	6070	4024	4024
2510	6071	0103	0103
2511	6072	7560	7560
2512	6073	6060	6060
2513	6074	6040	6040
2514	6075	0411	0411
2515	6076	2275	2275
2516	6077	0627	0627
2517	6100	0440	0440
2518	6101	0601	0601
2519	6102	1114	1114
2520	6103	0504	0504
2521	6104	0000	EXIT
2522	6105	0014	LTM004, 0014
2523	6106	2424	2424
2524	6107	4015	4015
2525	6110	0122	0122
2526	6111	1340	1340
2527	6112	0314	0314

/LIP END INST FAILED TO 0 PROGRESS

/LIN IAC=7777 DIR=REV FAILED

/LIN TAC=0000 DIR=FWD FAILED

/LIT MARK CLOCK FAILED TO GENERATE TFS

2528	6113	1703	1703
2529	6114	1340	1340
2530	6115	0601	0601
2531	6116	1114	1114
2532	6117	0504	0504
2533	6120	4024	4024
2534	6121	1740	1740
2535	6122	0705	0705
2536	6123	1605	1605
2537	6124	2201	2201
2538	6125	2405	2405
2539	6126	4024	4024
2540	6127	2063	2063
2541	6130	0000	EXIT

2542				
2543	6131	0014	LCMX00, 0014	/LCS IDLE > SEARCH FAILED
2544	6132	0323	0323	
2545	6133	4011	4011	
2546	6134	0414	0414	
2547	6135	0540	0540	
2548	6136	7640	7640	
2549	6137	2305	2305	
2550	6140	0122	0122	
2551	6141	0310	0310	
2552	6142	4006	4006	
2553	6143	0111	0111	
2554	6144	1405	1405	
2555	6145	0440	0440	
2556	6146	0000	EXIT	
2557	6147	0014	LCMX01, 0014	/LCS SEARCH > BLOCK FAILED
2558	6150	0323	0323	
2559	6151	4023	4023	
2560	6152	0501	0501	
2561	6153	2203	2203	
2562	6154	1040	1040	
2563	6155	7640	7640	
2564	6156	0214	0214	
2565	6157	1703	1703	
2566	6160	1340	1340	
2567	6161	0601	0601	
2568	6162	1114	1114	
2569	6163	0504	0504	
2570	6164	0000	EXIT	
2571	6165	0014	LCMX02, 0014	/LCS SEARCH > TURN AROUND FAILED
2572	6166	0323	0323	
2573	6167	4023	4023	
2574	6170	0501	0501	
2575	6171	2203	2203	
2576	6172	1040	1040	
2577	6173	7640	7640	
2578	6174	2425	2425	
2579	6175	2216	2216	
2580	6176	4001	4001	
2581	6177	2217	2217	
2582	6200	2516	2516	
2583	6201	0440	0440	
2584	6202	0601	0601	
2585	6203	1114	1114	
2586	6204	0504	0504	
2587	6205	0000	EXIT	

2588

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2599

2600

2601

2602

2603

2604

2605

2606

2607

2608

2609

2610

2611

2612

2613

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2617

2618

2619

2620

2621

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2624

2625

2626

2627

2628

2629

2630

2631

6206 0014

6207 0323

6210 4024

6211 2522

6212 1640

6213 0122

6214 1725

6215 1604

6216 4076

6217 4011

6220 0414

6221 0540

6222 0601

6223 1114

6224 0504

6225 0000

6226 0014

6227 0323

6230 4002

6231 1417

6232 0313

6233 4076

6234 4003

6235 1013

6236 4027

6237 2204

6240 4006

6241 0111

6242 1405

6243 0440

6244 0000

6245 0014

6246 0323

6247 4003

6250 1013

6251 4076

6252 4011

6253 0414

6254 0540

6255 0601

6256 1114

6257 0504

6260 0000

LCM003, 0014

0323

4024

2522

1640

0122

1725

1604

4076

4011

0414

0540

0601

1114

0504

EXIT

LCM004, 0014

0323

4002

1417

0313

4076

4003

1013

4027

2204

4006

0111

1405

0440

EXIT

LCM005, 0014

0323

4003

1013

4076

4011

0414

0540

0601

1114

0504

EXIT

/LCS TURN AROUND > IDLE FAILED

/LCS BLOCK > CHK WRD FAILED

/LCS CHK WRD > IDLE FAILED

2632			
2633	6261	0014	LCM006, 0014
2634	6262	0323	0323
2635	6263	4023	4023
2636	6264	0501	0501
2637	6265	2203	2203
2638	6266	1040	1040
2639	6267	7640	7640
2640	6270	1104	1104
2641	6271	1405	1405
2642	6272	4050	4050
2643	6273	1524	1524
2644	6274	0253	0253
2645	6275	1151	1151
2646	6276	4006	4006
2647	6277	0111	0111
2648	6300	1405	1405
2649	6301	0400	0400
2650	6302	0000	EXIT
2651	6303	0014	LWM101, 0014
2652	6304	2214	2214
2653	6305	7340	7340
2654	6306	1422	1422
2655	6307	0573	0573
2656	6310	4005	4005
2657	6311	1640	1640
2658	6312	2401	2401
2659	6313	0354	0354
2660	6314	4005	4005
2661	6315	1640	1640
2662	6316	2402	2402
2663	6317	5440	5440
2664	6320	1722	1722
2665	6321	4014	4014
2666	6322	1701	1701
2667	6323	0440	0440
2668	6324	2401	2401
2669	6325	0300	0300
2670	6326	7777	EXITA
2671	6327	0051	K7777
2672	6330	0115	REGA
2673	6331	0116	REGB
2674	6332	0000	EXIT

/LCS SEARCH > IDLE (MTB+I) FAILED

/LRL; LRE; EN TAC, EN TB, OR LOAD TAC
/0000 0000 0000

2675			
2676	6333	0014	LWM102, 0014
2677	6334	2423	2423
2678	6335	4020	4020
2679	6336	1001	1001
2680	6337	2305	2305
2681	6340	4007	4007
2682	6341	0124	0124
2683	6342	0540	0540
2684	6343	0601	0601
2685	6344	1114	1114
2686	6345	0504	0504
2687	6346	0000	EXIT
2688	6347	0014	LWM101, 0014
2689	6350	2716	2716
2690	6351	4015	4015
2691	6352	0122	0122
2692	6353	1340	1340
2693	6354	2722	2722
2694	6355	1124	1124
2695	6356	0540	0540
2696	6357	0701	0701
2697	6360	2405	2405
2698	6361	4006	4006
2699	6362	0111	0111
2700	6363	1405	1405
2701	6364	0400	0400
2702	6365	0000	EXIT
2703	6366	0014	LMM000, 0014
2704	6367	2422	2422
2705	6370	4004	4004
2706	6371	0124	0124
2707	6372	0140	0140
2708	6373	0310	0310
2709	6374	0116	0116
2710	6375	1605	1605
2711	6376	1440	1440
2712	6377	2227	2227
2713	6400	0240	0240
2714	6401	6054	6054
2715	6402	6454	6454
2716	6403	7040	7040
2717	6404	0601	0601
2718	6405	1114	1114
2719	6406	0504	0504
2720	6407	4000	4000
2721	6410	7777	EXITA
2722	6411	0116	REGB
2723	6412	0117	REGC
2724	6413	0000	EXIT
2725	6414	0014	LTM000, 0014
2726	6415	2424	2424
2727	6416	4015	4015
2728		0122	0122
2729		1340	1340

/LTS PHASE GATE FAILED

/LWN MARK WRITE GATE FAILED

/LTR DATA CHANNEL RWB 0, 4, 8 FAILED
/4210 0160

/LTT MARK CLOCK FAILED TO GENERATE TEL

2730	6421	0314	0314
2731	6422	1703	1703
2732	6423	1340	1340
2733	6424	0601	0601
2734	6425	1114	1114
2735	6426	0504	0504
2736	6427	4024	4024
2737	6430	1740	1740
2738	6431	0705	0705
2739	6432	1605	1605
2740	6433	2201	2201
2741	6434	2405	2405
2742	6435	4024	4024
2743	6436	2060	2060
2744	6437	0000	EXIT

2745			
2746			
2747	6440	0014	LTM101, 0014
2748	6441	2423	2423
2749	6442	4014	4014
2750	6443	1116	1116
2751	6444	0540	0540
2752	6445	0317	0317
2753	6446	2516	2516
2754	6447	2405	2405
2755	6450	2240	2240
2756	6451	0601	0601
2757	6452	1114	1114
2758	6453	0504	0504
2759	6454	4024	4024
2760	6455	1740	1740
2761	6456	0317	0317
2762	6457	2516	2516
2763	6460	2400	2400
2764	6461	7777	EXITA
2765	6462	0116	REGB
2766	6463	0000	EXIT
2767	6464	0014	MOTT1M, 0014
2768	6465	1525	1525
2769	6466	4024	4024
2770	6467	2522	2522
2771	6470	1640	1640
2772	6471	0122	0122
2773	6472	1604	1604
2774	6473	5440	5440
2775	6474	0215	0215
2776	6475	4006	4006
2777	6476	0111	0111
2778	6477	1405	1405
2779	6500	0440	0440
2780	6501	2417	2417
2781	6502	4060	4060
2782	6503	1517	1517
2783	6504	2411	2411
2784	6505	1716	1716
2785	6506	0000	EXIT

/LTS LINE COUNTER FAILED TO COUNT
/0000

/LMU TURN ARND, BM FAILED TO 2 MOTION

2786	6507	0014	MOTT2M,	0014
2787	6510	1525		1525
2788	6511	4024		4024
2789	6512	0120		0120
2790	6513	0540		0540
2791	6514	2022		2022
2792	6515	0523		0523
2793	6516	0524		0524
2794	6517	4006		4006
2795	6520	0111		0111
2796	6521	1405		1405
2797	6522	0440		0440
2798	6523	2417		2417
2799	6524	4060		4060
2800	6525	4015		4015
2801	6526	1724		1724
2802	6527	1117		1117
2803	6528	1640		1640
2804	6531	0000		EXIT
2805	6532	0014	MOTT3M,	0014
2806	6533	1525		1525
2807	6534	4003		4003
2808	6535	1422		1422
2809	6536	4020		4020
2810	6537	2217		2217
2811	6540	0722		0722
2812	6541	0523		0523
2813	6542	2340		2340
2814	6543	0601		0601
2815	6544	1114		1114
2816	6545	0504		0504
2817	6546	4024		4024
2818	6547	1740		1740
2819	6550	4060		4060
2820	6551	4015		4015
2821	6552	1724		1724
2822	6553	1117		1117
2823	6554	1640		1640
2824	6555	0000		EXIT
2825	6556	0014	REGM04,	0014
2826	6557	2214		2214
2827	6560	4024		4024
2828	6561	2063		2063
2829	6562	4006		4006
2830	6563	0111		0111
2831	6564	1405		1405
2832	6565	0440		0440
2833	6566	2417		2417
2834	6567	4023		4023
2835	6570	1011		1011
2836	6571	0624		0624
2837	6572	4022		4022
2838	6573	2702		2702
2839	6574	4000		4000
2840	6575	7777		EXITA

/LMU TAPE PRESET FAILED TO 0 MOTION

/LMU CLR PROGRESS FAILED TO 0 MOTION

/LRL TP3 FAILED TO SHIFT RWB
/2000 0000

2841	6576	0116	REGB
2842	6577	0117	REGC
2843	6600	0000	EXIT

2844				
2845	6601	0014	REGM09, 0014	/LRL EN WRITE LD RWB FAILED TO SHIFT RWB.
2846	6602	2214	2214	/0000 0000
2847	6603	4005	4005	
2848	6604	1640	1640	
2849	6605	2722	2722	
2850	6606	1124	1124	
2851	6607	0540	0540	
2852	6610	1404	1404	
2853	6611	4022	4022	
2854	6612	2702	2702	
2855	6613	4006	4006	
2856	6614	0111	0111	
2857	6615	1405	1405	
2858	6616	0440	0440	
2859	6617	2417	2417	
2860	6620	4023	4023	
2861	6621	1011	1011	
2862	6622	0624	0624	
2863	6623	4000	4000	
2864	6624	7777	EXITA	
2865	6625	0116	REGB	
2866	6626	0117	REGC	
2867	6627	0000	EXIT	
2868	6630	0014	REGM09, 0014	/LRL TB+TAC=TAC FAILED
2869	6631	2214	2214	/0000 0000 0000 0000
2870	6632	4024	4024	
2871	6633	0253	0253	
2872	6634	2401	2401	
2873	6635	0375	0375	
2874	6636	2401	2401	
2875	6637	0340	0340	
2876	6640	0601	0601	
2877	6641	1114	1114	
2878	6642	0504	0504	
2879	6643	4000	4000	
2880	6644	7777	EXITA	
2881	6645	0116	REGB	
2882	6646	0117	REGC	
2883	6647	0114	REGD	
2884	6650	0046	REGE	
2885	6651	0000	EXIT	
2886	6652	0014	REGM12, 0014	/LRL LOAD TAC FAILED TP3, SEARCH
2887	6653	2214	2214	/0000
2888	6654	4014	4014	
2889	6655	1701	1701	
2890	6656	0440	0440	
2891	6657	2401	2401	
2892	6660	0340	0340	
2893	6661	0601	0601	
2894	6662	1114	1114	
2895	6663	0504	0504	
2896	6664	4024	4024	
2897	6665	2063	2063	
2898	6666	5440	5440	

2899	6667	2305		2305
2900	6670	0122		0122
2901	6671	0310		0310
2902	6672	4000		4000
2903	6673	7777		EXITA
2904	6674	0116		REGB
2905	6675	0000		EXIT
2906	6676	0024	PASSM,	0024
2907	6677	0361		0361
2908	6700	6255		6255
2909	6701	2001		2001
2910	6702	2224		2224
2911	6703	4062		4062
2912	6704	4020		4020
2913	6705	0123		0123
2914	6706	2300		2300
2915	6707	7777		EXITA
2916	6710	0065		PASS
2917	6711	4444		4444
2918				
2919	6712	0014	WRCM,	0014
2920	6713	0323		0323
2921	6714	4027		4027
2922	6715	2211		2211
2923	6716	2405		2405
2924	6717	4003		4003
2925	6720	3103		3103
2926	6721	1405		1405
2927	6722	4006		4006
2928	6723	1417		1417
2929	6724	2040		2040
2930	6725	2405		2405
2931	6726	2324		2324
2932	6727	4006		4006
2933	6730	0111		0111
2934	6731	1405		1405
2935	6732	0400		0400
2936	6733	0000		EXIT
2937	6734	0014	TTOKM,	0014
2938	6735	2423		2423
2939	6736	4024		4024
2940	6737	1115		1115
2941	6740	1116		1116
2942	6741	0740		0740
2943	6742	1713		1713
2944	6743	4007		4007
2945	6744	0124		0124
2946	6745	0540		0540
2947	6746	0601		0601
2948	6747	1114		1114
2949	6750	0504		0504
2950	6751	0000		EXIT
2951	6752	0014	TMATB,	0014
2952	6753	2205		2205
2953	6754	4024		4024

/TC12-PART 2 PASS--(PASS)

/RETURN TO LOC 177

/LCS WRITE CYCLE FLOP TEST FAILED

/LTS TIMING OK GATE FAILED

/LRE TNA FAILED TO INCREMENT DURING TAPE BREAK.

2934	6755	1501	1901
2935	6756	4006	4006
2936	6757	0111	0111
2937	6760	1405	1405
2938	6761	0424	0424
2939	6762	1740	1740
2940	6763	1116	1116
2941	6764	0322	0322
2942	6765	0519	0519
2943	6766	0516	0516
2944	6767	2440	2440
2945	6770	0425	0425
2946	6771	2211	2211
2947	6772	1007	1007
2948	6773	4024	4024
2949	6774	0120	0120
2950	6775	0502	0502
2971	6776	2205	2205
2972	6777	0113	0113
2973	7000	5600	5600
2974	7001	2701	2701
2975	7002	2340	2340
2976	7003	4040	4040
2977	7004	1123	1123
2978	7005	4000	4000
2979	7006	7777	EXITA
2980	7007	0170	CO176
2981	7010	0117	REGC
2982	7011	0000	EXIT
2983	7012	0024	0024
2984	7013	2201	2201
2985	7014	2040	2040
2986	7015	2422	2422
2987	7016	0120	0120
2988	7017	4006	4006
2989	7020	0111	0111
2990	7021	1405	1405
2991	7022	0400	0400
2992	7023	7777	EXITA
2993	7024	0140	0140
2994	7025	0000	EXIT
2995			

/HAS IS

TRAPM:

/TAPE TRAP FAILED
/0000

S

3699
3700

4000

4100

4200

4300

4400

4500

4600

4700

5000 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

5100 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111110

5200 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

5300 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

5400 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

5500 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

5600 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

5700 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

6000 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

6100 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

6200 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

6300 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

6400 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

6500 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

6600 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

6700 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

7000 11111111 11111111 11111100 00000000 00000000 00000000 00000000 00000000

7100 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000

7200

7300

7400

7500

7600

7700

ASCII	5054	K3400	0004	LIM008	5435	LT0004	1400
ASCRXT	5027	K3420	0164	LIM009	5464	LW1004	0172
AXO	5021	K3427	0165	LIM010	5516	LWB102	2157
BELL	5200	K3440	0154	LIM012	6025	LWB104	2224
BELLA	0103	K3700	0123	LIM013	5544	LWM101	6303
C0050	0144	K4000	0003	LIM013	5567	LWM102	6333
C0176	0170	K4140	0053	LIM017	5611	LWM104	6347
CLR	0011	K4210	0042	LIM018	5647	LWN102	2120
COM	0017	K4440	0122	LIM019	5666	LWN104	2164
CRLF	5157	K5000	0043	LIM022	5705	LWNORM	2027
DATUM	5120	K6000	0070	LIM023	5725	LXA000	2301
DATYP	5166	K6020	0155	LIN001	1367	M0100	0150
DELAY	0126	K6040	0067	LIN002	1422	M0220	0152
DOMORE	3155	K7000	0047	LINC	6141	M0400	0124
ERROR	0037	K7030	0050	LINMX1	6047	M1000	0125
ERRORS	5021	K7040	0157	LINMX2	6066	M2000	0151
ESF	0004	K7356	0171	LIP000	0202	M40	0074
EXIT	0000	K7400	0006	LIP001	0231	M4444	0052
EXITA	7777	K7737	0162	LIP002	0264	MAINT1	0032
HERE	5142	K7770	0054	LIP003	0313	MAINTS	3134
K0002	0040	K7773	0111	LIP004	0344	MOTST1	2354
K0003	0103	K7774	0076	LIP005	0403	MOTST2	2402
K0007	0156	K7777	0051	LIP006	0427	MOTST3	2425
K0010	0112	LCM000	5746	LIP007	0460	MOTT1M	6464
K0011	0153	LCM001	5762	LIP008	0502	MOTT2M	6507
K0012	0160	LCM002	6165	LIP009	0524	MOTT3M	6532
K0013	0146	LCM003	6206	LIP010	0550	NERROR	0036
K0016	0033	LCM004	6226	LIP011	0620	NERROS	5000
K0017	0007	LCM005	6245	LIP012	0630	OCTYP	5136
K0020	0110	LCM006	6261	LIP013	0677	OUTPAS	0064
K0040	0035	LCMX00	6131	LIP015	0763	PASS	0065
K0050	0107	LCMX01	6147	LIP017	1041	PASSM	6676
K0077	0073	LCS000	1513	LIP018	1116	PDP	0002
K0100	0055	LCS001	1540	LIP019	1142	PINT	0010
K0150	0057	LCS002	1577	LIP022	1172	PNTA	0060
K0160	0041	LCS003	1631	LIP024	1220	PNTB	0061
K0177	0102	LCS004	1661	LMM000	6366	PNTC	0062
K0200	0056	LCS005	1730	LMR	6151	PNTJ	0063
K0207	0104	LCS006	2000	LOADR	0034	RAN	0045
K0212	0101	LCX000	1321	LOADS	3144	RANDOM	5216
K0215	0100	LCX001	1347	LOC170	0176	REDC	5143
K0250	0005	LIA004	0121	LOCA	0450	REG004	2467
K0400	0072	LIB004	0376	LOCC	1302	REG006	2521
K1000	0071	LIB005	0422	LOCJ	3133	REG009	2605
K1026	0077	LIM000	6006	LOCTRP	3105	REGZ12	2672
K1400	0145	LIM001	5233	LSTERR	0024	REGA	0115
K177	0137	LIM002	5261	LTB000	2274	REGB	0116
K2000	0066	LIM003	5307	LTM000	6414	REGC	0117
K240	0075	LIM004	5326	LTM004	6105	REGD	0114
K3000	0147	LIM005	5345	LTM101	6440	REGE	0046
K3020	0161	LIM006	5364	LTR000	2231	REGF	0120
K3040	0044	LIM007	5410	LTS101	2324	REGM04	6556

RECORD0	6601
RECORD1	6630
RECORD2	6652
RETURN	0000
RVA	0166
RVB	0167
SPACE	0106
STD	0416
STU	0457
TAT	0003
TEMPB	0113
TEMPC	6752
TEMPD	0025
TEMPF	3074
TEMPG	3114
TEMPH	7010
TEMPI	6152
TEMPJ	3034
TEMPK	6734
TEMPL	0105
TEMPM	5103
TEMPN	5210
TEMPO	3027
TEMPQ	2727
TEMPR	6712
TEMPS	6154
TEMPT	0021

ERRORS DETECTED: 0

LINKS GENERATED: 0

RUN-TIME: 29 SECONDS

NO CORE USED

ASCI	186	1944	1968	1998										
ASCRXT	1946#	1979	2009	2048										
AXO	59#	869	890	981	1432	1434	1818	1888						
BELL	122	2057#	2061	2064										
BELLA	122#	185	1945											
C0050	157#	388												
C0176	177#	798	2980											
CLR	63#	870	1433											
COM	98#	320	321	327	328	344	345	351	352	718	719	725	726	746
	747	753	754	780	781									
CRLF	1996	2027	2031	2039#	2045	2052								
DATUM	1982	2005#	2018	2054										
DATYP	1974	2046#	2051											
DELAY	142#	150	180											
DOMORE	1902#	1915												
ERROR	85#	211	242	269	298	332	356	383	407	428	452	496	553	610
	659	707	730	758	785	839	854	880	899	933	967	998	1025	1060
	1090	1116	1161	1205	1232	1277	1333	1374	1420	1443	1470	1499	1521	1559
	1589	1646	1700	1733	1805	1840	1864	1880						
ERRORS	85	1927	1929	1933	1940#	1946	1949	1952	1953	1954	1955	1964	1965	1966
	1969	1971												
ESF	65#	1852	1859											
EXIT	51#	2106	2129	2144	2160	2175	2196	2217	2241	2267	2290	2310	2328	2359
	2374	2389	2406	2424	2437	2457	2472	2491	2506	2521	2541	2556	2570	2587
	2604	2619	2631	2650	2674	2687	2702	2724	2744	2766	2785	2804	2824	2843
	2867	2889	2905	2936	2950	2982	2994							
EXITA	52#	2420	2434	2455	2670	2721	2764	2840	2864	2880	2903	2915	2979	2992
HERE	2026#	2037												
K00002	86#	823	1693	1831										
K00003	172#	1270												
K00007	167#													
K00010	129#	1440	1496	1518	1552	1609	1624	1816	1903					
K00011	164#	827	1262	1685										
K00012	169#													
K00013	159#													
K00016	81#	203	230	261	288	374	443	466	525	577	629	673	769	814
	917	947	977	1040	1075	1105	1139	1176	1220	1254	1324	1343	1452	1498
	1543	1612	1658	1758	1779	1813								
K00017	46#													
K00020	127#	600	652	771	983	1454	1627	1723	1751	1776	1802	1896	1907	
K00040	83#	205	232	263	290</									

K0218	119#	2040														
K0236	44#	979														
K0400	112#	991	1931													
K1500	111#	194	221	252	279	307	471	530	572	595	624	647	675	829		
	919	049	1045	1077	1138	1181	1250	1306	1392	1406	1534	1573	-4-4	7*		
	1800	1671	1719	1754	1787											
K1026	110#	2026														
K1400	150#	700	1465	1850												
K177	151#	849														
K2000	100#	404	425	449	493	607	704									
K240	116#	2001	2016													
K3000	160#															
K3020	170#															
K3040	90#															
K3400	43#															
K3420	173#															
K3427	174#	1576														
K3440	165#	1636														
K3700	130#	927	961	1019	1056	1084	1112	1155	1199	1226						
K4000	42#															
K4140	97#	1827														
K4210	88#	1386														
K4440	137#	923	957	1015	1050	1080	1107	1143	1151	1186	1194	1222	1747	1771		
	1797															
K5000	89#	1492	1514	1548												
K6000	110#	400	421	489	603	706	987	1395	1409	1436	1461					
K6020	166#	1294	1327	1392	1367											
K6040	109#	445	1288	1321	1345	1360										
K7000	93#	844														
K7030	94#															
K7040	168#															
K7356	170#	1502														
K7700	45#															
K7737	143	171#														
K7770	98#	1825														
K7773	128#	1900														
K7774	117#	2021														
K7777	95#	2671														
LCH000	801	2426#														
LCH001	900	2430#														
LCH002	1091	2571#														
LCH003	1119	2589#														
LCH004	1162	2605#														
LCH005	1206	2620#														

[illegible]

[illegible]

MOTS#1	1402#	1503												
MOTS#2	1407#	1504												
MOTS#3	1408#	1505												
MOTS#4	1409#	1506												
MOTS#5	1410#	1507												
MOTS#6	1411#	1508												
MOTS#7	1412#	1509												
MOTS#8	1413#	1510												
MOTS#9	1414#	1511												
MOTS#10	1415#	1512												
MOTS#11	1416#	1513												
MOTS#12	1417#	1514												
MOTS#13	1418#	1515												
MOTS#14	1419#	1516												
MOTS#15	1420#	1517												
MOTS#16	1421#	1518												
MOTS#17	1422#	1519												
MOTS#18	1423#	1520												
MOTS#19	1424#	1521												
MOTS#20	1425#	1522												
MOTS#21	1426#	1523												
MOTS#22	1427#	1524												
MOTS#23	1428#	1525												
MOTS#24	1429#	1526												
MOTS#25	1430#	1527												
MOTS#26	1431#	1528												
MOTS#27	1432#	1529												
MOTS#28	1433#	1530												
MOTS#29	1434#	1531												
MOTS#30	1435#	1532												
MOTS#31	1436#	1533												
MOTS#32	1437#	1534												
MOTS#33	1438#	1535												
MOTS#34	1439#	1536												
MOTS#35	1440#	1537												
MOTS#36	1441#	1538												
MOTS#37	1442#	1539												
MOTS#38	1443#	1540												
MOTS#39	1444#	1541												
MOTS#40	1445#	1542												
MOTS#41	1446#	1543												
MOTS#42	1447#	1544												
MOTS#43	1448#	1545												
MOTS#44	1449#	1546												
MOTS#45	1450#	1547												
MOTS#46	1451#	1548												
MOTS#47	1452#	1549												
MOTS#48	1453#	1550												
MOTS#49	1454#	1551												
MOTS#50	1455#	1552												
MOTS#51	1456#	1553												

[illegible]