digital INTEROFFICE MEMORANDUM

TO: Distribution List

DATE: January 23, 1973

FROM: Larry Goelz

DEPT: Computerpac Support

SUBJ: Option/Maindec Listing

The attached document represents a first pass attempt of providing a list of options, their applicable Maindecs, how to run the Maindecs, and the options IOT codes for the PDP-8 Family, all under one document. There are some minor errors in the listing; a few new options not included and some Maindec number changes that did not get in. In the near future, this document will be released to the Program Library with corrections and in a maintainable form which will be updated on a r- basis.

slm

PDP-8

diagnostic programs index by options

INTRODUCTION

THIS DOCUMENT HAS BEEN COMPILED TO ENABLE A PERSON TO KNOW WHAT DIAGNOSTICS AFFECT ANY OPTION AND THEN BE ABLE TO READ A BRIEF ABSTRACT AND STARTING PROCEDURE ON ANY DIAGNOSTIC. THE FIRST LIST CONTAINS PDP-8 FAMILY OPTIONS AND THE DIAGNOSTICS THAT AFFECT THAT OPTION, THE SECOND IS A LIST OF MAINDECS AND THEIR TITLES, THEN FOLLOWS ABSTRACTS AND STARTING INSTRUCTIONS FOR ALL THE MAINDECS, AT THE END OF THE DOCUMENT IS A TABLE LISTING THE OPTION AND ITS IOT CODES.

OPTIONS	MAINDECS THAT TEST OR EXERCIST THE OPTION
AA05/AA07	08-D6TA
AA50	08-D6WB
AD01-A	08-D6UB
AD08A,B	08-D6JD
AD8E	08-DHADA-A
AF01	08-D6GC
AF04	08-D6HA, D6RB
AF06	8I-D6BB
AFC-8	08-D6VA
AM08/AM03	08-D6QA
AM8E	08-DHADA-A
AX08	8I-D6AC
BM08	8L-D1HA,D1EC
BM8L	8L-D1JA, D0AB; 08-D1EC, D1HA, DHKMA-A,DEBMA,
CM8E	8E-D2DB
CM8F	8E-D2DB
CM8I	8I-D2BA
CM8L	8I-D2BA
CR8-E	8E-D2EB
CR8-F	8E-D2EB
CR8I	08-D20A
CR8L	08-D20A
DB88	08-D8GA
DB08A	08-D81B

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D88EA           8E=D0PC, D0SA
DC02            08=D8WA, D2AA
DC02F           12=D8FB
DC04            08=D9IB
DC08A,B,C,CS    8I=D8AC,D8BB
DC08H,J         8I=D8FA
DC08F,FE,FF     8I=D8FA,D8EA
DC14
DF32            08=D5DB, D5CG, D5BC; 8I=D5DB; X8=DIDFA=A
DF32D           08=D5CG,D5DB; 8I=D5FB; X8=DIDFA
DF32E           08=D5CG, D5DB; 8I=D5FB
DK8-E           8E=D8AC; X8=DIDKA=A
DM01            08=D9KA, D8SC
DM04            08=D9KA; 8I=D8HA
DP8-E           8E=D8BB
DP01A           08=D9MA,D9NA, D9PA, D9QA, D8EB
DR8-E           08=DHDRA=A
DS32            08=D5BB,D5CG, D5DB; 8I=D5BB; X8=DIDFA=A
FPP12           12=D0MC,D0NB,D0OB,D0PC; X8=DIFPA=A
KE8-E           8E=D0LB, D0MB, D0RA; X8=DHKEA=A, DIKEA=A
KE8I            8I=D0AA, D0BA; 08=D0BA; X8=DIKEA=A
KG8E            8E=D8CA
KL8             08=DHKLD=A
KL8F            08=CR8I          08=D20A
KL8-E, A=G      08=DHKLD=A
KM8-E           08=DHKMA=A; 8E=D1FB,D1HB
KP8-E           08=DHKPA=A
KP8I            08=D1KB
KP8L            08=D1KB
KT8I            T8=D8AA,D8BB
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KV8:            8I←D6CE, D6DA
KW08-S          08←D8VB
KW8-I           8I←D8AE; X8←DIDKA←A
KW8L            8I←D8AE; X8←DIDKA←A
LC8L            ?
LC8E            8E←D2FB; X8←DILPA←A
LE8             8I←D2AC; X8←DILPA←A
LP08            8I←D2AC
LS8E            08←DHLSA←A
LT08            MAINDEC-828; 08←D2AA; X8←DILPA←A
LT33            08←D2PE, D2QD, DHKLD←A, DHKLC←A, D2AA; X8←DILPA←A
LT35            08←D2PE, D2QD, DHKLD←A, DHKLC←A, D2AA; X8←DILPA←A
MC8-E           08←DHKMA←A; 8E←D1FB, D1HB
MC8I            08←D4BA, D1EC, D1GD, D1HA, D1L1, D1L2, D1MA←PM1,2
MC8L            8L←D1HA, D1GC; 08←D1EC
MI8E            8E←D1IB
MM8E            8E←D1AB, D1EC
MM8EJ
MM8I            08←D1MA, D1L1,D1L2; D4BA, D1MA←PM(1),(2)
MM8L            08←D1MA, D1L1,D1L2; D4BA, D1MA←PM(1),(2)
MP8I            8I←D4CA; 08←DHA0
MP8L            8L←D5AA; 08←04A0
MP8-E           08←DHMPA←A
MR8-E           8E←D1JB(1), D1JB(2), D1KA
PA60A           08←D2HC
PA60B           08←D2HC
PA60C           08←D2UA
PA61A           08←D2HC
PA63            08←D2HC, D2UA
PA68A           08←D2HC
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PA68F	08=D2HC
PC01	08=D2EA,D2FC, D2GF; X8=DIPLA=A
PC02	08=D2EA, D2FC, D2GF; X8=DIPCA=A
PC03	08=D2GF; X8=DIPCA=A
PC04	08=D2EA, D2FC, D2GF; X8=DIPCA=A
PC8E	8E=D2CA; X8=DIPCA=A
PC8I	08=D2EA, D2FC, D2GF; X8=DIPCA=A
PC8L	08=D2EA,D2FC,D2GF; X8=DIPCA=A
PDP-8	MAINDEC-801; 08-D01A, D02B, D04B, D05B, D07B, D1MA, D1LO, D2EP, D2QD, D1AC
PDP-8E	8E=D0AB, D0BB, D0CC, D0DB, D0EB, D0FC, D0GC; D0HC, D0IB, D0JC, D1AB, D1EC, D1GB,
PDP-8F	8E=D0AB, D0BB, D0CC, D0DB, D0EB, D0FC, D0GC; D0HC, D0IB, D0JC, D1AB, D1EC, D1GB,
PDP-8I	8I=D01C, D02B; 08=D02B, D04B, D05B, D07B, D1LO, D1MA, D2PE, D2QD, D1AC
PDP-8L	8I=D01C, D02B; 08=D02B, D04B, D05B, D07B, D1LO, D1MA, D2PE, D2QD, D1AC; 8L=D0AB
PDP-8M	8E=D0AB, D0BB, D0CC, D0DB, D0EB, D0FC, D0GC; D0HC, D0IB, D0JC, D1AB, D1EC, D1GB,
PP8E	8E=D2CA; X8=DILCA=A
PP8I	08=D2GF; X8=DIPCA=A
PP8L	08=D2GF; X8=DIPCA=A
PP67A,B,C,D	08=D2HC
PR68A,B,D,DA	08=D2HC
PR8E	8E=D2CA; X8=DIPCA=A
PR8I	08=D2EA, D2FC; X8=DIPCA=A
PR8L	08=D2EA,D2FC; X8=DIPCA=A
PT08BC	MAINDEC-828; 08-D2AA
PT08F	08=D8PA
RC8/RS64	
RF08/RS08	08=D5EB, D5FA; X8=DIRFA=A
RK8	08=D5HC, D5KB, D5JB; X8=DIRKA=A
RM08	08=D5AA
RK8E/RK05	08=DHRKA, DHRKB, DHRKC, DHRKD
TC01	08=D3BD, D3RA,D3EB; X8=DITCA=A

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TC08            08-D3BD, D3RA, D3EB; X8-DITCA-A

TC58            08-D9AD, D9BA, D9CC, D9DE, D9EC, D9FC,D9GA; X8-DITCB-A

TD8-E           8E-D3AB(1), D3AB(2)

TM8-E

TR02            08-D4FB, D4DA, D4ER, D3FC,D4CB

TR05/TR06       08-D9AD, D9CC

UDC8            08-D8YC

VC8E            8E-D6CB

VC8I            08-D6KC

VC8L            08-D6KC

VP8I            08-D6CC

VP8L            08-D6CC

VT05            08-DGV5A-A; X8-DILPA-A

VT06            12-D2AA; X8-DILPA-A

VW02            8E-D7AA

XY8E            8E-D6AB
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INDEX OF MAINDECS

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MAINDEC-08-DHKM-A       PDP-8/E EXTENDED MEMORY DATA AND CHECKERBOARD TESTS
        08-DHKPA-A      KP8E POWER FAIL/AUTO RESTART TEST
        08-DGV5A-A      VT05 TERMINAL DIAGNOSTIC
        08-DHKLD-A      PDP-8/E TELETYPE AND KL8 ASYNCHRONOUS DATA CONTROL TESTS
        08-DHDRA-A      DR8EA 12 CHANNEL BUFFERED DIGITAL INTERFACE
        08-DHADA-A      AD8E,AM8E A-D CONVERTER AND MULTIPLEXER DIAG.
        08-DHKLC-A      KL8F DOUBLE BUFFERED ASYNCHRONOUS INTERFACE DIAG.
        08-DHMPA-A      PDP-8/E EXTENDED MEMORY PARITY TEST
        08-DHLSA-A
        08-DHRKA
        08-DHRKB
        08-DHRKC
        08-DHRKD
        08-D01A         PDP-8 INSTRUCTION TEST - PART 2A
        08-D02B         PDP-8 INSTRUCTION TEST - PART 2B
        08-D04B         RANDOM JMP TEST
        08-D05B         RANDOM JMP-JMS TEST
        08-D07B         RANDOM ISZ TEST
        08-D0BA         PDP-8 INSTRUCTION TEST EAE
        08-D0UA         FAMILY OF 8 RANDOM ADD ROTATE TEST
        08-D1AC         PDP-8 MEMORY POWER ON/OFF TEST
        08-D1EC         PDP-8,8I EXTENDED MEMORY CHECKERBOARD
        08-D1GD         PDP-8, 8I, 8S EXTENDED MEMORY CONTROL
        08-D1HA         PDP-8, 8I EXTENDED MEMORY ADDRESS TEST
        08-D1KB         KP8I/KR01 POWER FAIL TEST
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08-D1LO         BASIC PDP-8, 8I MEMORY CHECKERBOARD
08-D1MA         MEMORY ADDRESS TEST

08-D2AA         FAMILY OF 8 TELETYPE TESTS THRU PT08,LT08 OR DC02 INTERFACE
08-D2EA         PDP-8 HIGH SPEED READER TEST
08-D2FC         HIGH SPEED READER TEST
08-D2GF         FAMILY OF 8 HIGH SPEED PUNCH AND READER TESTS
08-D2HC         FAMILY OF 8 TYPESETTING CONFIGURATION TESTS
08-D2OA         CR03 G,D,I, CARD READER TEST
08-D2PE         FAMILY OF 8 ASR 33/35 TELETYPE TESTS PART 1
08-D2QD         FAMILY OF 8 ASR 33/35 TELETYPE TESTS PART 2
08-D2UA         PA60C DIAGNOSTIC
08-D3BD         TC01 BASIC EXERCISER
08-D3EB         TC01 EXTENDED MEMORY EXERCISER
08-D3FC         INCREMENTAL TAPE DELAY TEST
08-D3RA         DECTREX 1 TC01 RANDOM EXERCISER
08-D4A0         PDP-8,8I MEMORY PARITY CHECKERBOARD
08-D4BA         PDP-8, 8I EXTENDED MEMORY PARITY TEST
08-D4CB         PDP-8I,8L INCREMENTAL TAPE COMPATIBILITY TEST
08-D4DA         INCREMENTAL TAPE DATA RELIABILITY TEST
08-D4EB         PDP-8I AND 8L PEC INCREMENTAL TAPE INSTRUCTION TEST
08-D4FB         PDP8I AND 8L PEC INCREMENTAL TAPE RANDOM EXERCISER
08-D5AA         RM08 DRUM TEST AND MAINTENANCE COMPILER
08-D5BC         DF32 DISKLESS LOGIC TEST
08-D5CG         DF32/DF32D DISK DATA MINIDISK, INTERFACE ADDRESS, DATA TEST
08-D5DB         DF32 MULTI DISK
08-D5EB         RF08 DISK DATA(256K)
08-D5FA         RF08 MULTI DISK II (256K)
08-D5HC         RK8 DISK DATA RELIABILITY TEST (RK01 VERSION)
08-D5JB         RK8 DISK AND CONTROL INSTRUCTION TEST
08-D5KB         RK08 DISK FORMATTER
08-D6CC         PDP-8 CALCOMP PLOTTER DIAGNOSTIC
08-D6GC         A/D CALIBRATION CHECK
08-D6HA         AF04A DIAGNOSTIC AND DEMONSTRATION
08-D6JD         AD08 DIAGNOSTIC
08-D6KC         DISPLAY TEST 340/VC8I
08-D6QA         LOW LEVEL MULTIPLEXER DIAGNOSTIC(AM08/AM03)
08-D6RB         AF04 DIAGNOSTIC TEST
08-D6TA         AA05/AA07 CALIBRATION TAPE
08-D6UB         AD01-A DIAGNOSTIC
08-D6VA         AFC-8 DIAGNOSTIC
08-D6WB         AA50 D/A CONVERTER DIAGNOSTIC
08-D7CA         TYPESET-8 SYSTEM EXERCISER (TCSE)
08-D81B         DB08A TEST
08-D8EB         DP01A IOT AND DATA TESTS(DEVICE CODE 30)
08-D8GA         DB88 TEST
08-D8PA         PT08 TEST PROGRAM FOR USE WITH DATAPHONE OPTIONS
08-D8SC         DM01 EXERCISER
08-D8VB         KW08S CLOCK TEST
08-D8WA         DC02
08-D8XA         XOR BUFFER OPTION DIAG, FOR USE WITH DP01A
08-D8YC         UDC8 SYSTEM FUNCTION EXERCISER
08-D9AD         TC58 DATA RELIABILITY TEST (7 TRACK)
08-D9BA         TC58 DRIVE FUNCTION TIMER
08-D9CC         TC58 RANDOM EXERCISER
08-D9DE         TC58 INSTRUCTION TEST - PART 1
08-D9EC         TC58 INSTRUCTION TEST - PART 2
08-D9FC         TC58 DATA RELIABILITY TEST (9 TRACK)
08-D9GA         TC58 DATA RELIABILITY TEST (9 TRACK-TU30 VERSION)
08-D9IB         PDP 8I/L DC04-C WIRE STORAGE INTERFACE DIAG.
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08-D9KA	FAMILY OF 8 MULTI BREAK DEVICE EXERCISER
08-D9MA	DP01A BIT SYNCHRONOUS DATA COMM,SYSTEM IOT TEST 6301
08-D9NA	DP01A BIT SYNCHRONOUS DATA COMM,SYSTEM IOT TEST 6501
08-D9PA	DP01A BIT SYNCHRONOUS DATA COMM,SYSTEM IOT TEST 6601
08-D9QA	DP01A BIT SYNCHRONOUS DATA CONN,SYSTEM IOT TEST 6701
MAINDEC-8L-D0A$_B$	8L MEMORY PROTECT TEST
8L-D1GC	PDP 8L EXTENDED MEMORY CONTROL TEST
8L-D1HA	PDP 8L EXTENDED MEMORY CONTROL TEST (12K)
8L-D1JA	BM8L EXTENDED MEMORY CONTROL TEST
8L-D5AA	PDP 8L MEMORY PARITY IOT TEST
MAINDEC-828	PDP-8 LT08 TELEPRINTER TEST
T8-D8AA	TIME SHARING 8 OPTION TEST
T8-D8BB	TIME SHARE 8 HARDWARE EXERCISER
M$_A$INDEC-12-D8F$_B$	DC02-F OPTION TEST
12-D0MC	FPP12 INSTRUCTION TEST 2A
12-D0NB	FPP12 INSTRUCTION TEST 2B
12-D0OB	FPP12 INSTRUCTION TEST 2C
12-D0PC	FPP12 ADDRESS TEST
12-D2AA	VT06 (DATA POINT 3300)
MAINDEC-8I-D01C	INSTRUCTION TEST 1
8I-D02B	INSTRUCTION TEST 2
8I-D0AA	PDP 8I INSTRUCTION TEST - PART 3A
8I-D0BA	EXTENDED ARITHMETIC PDP 8I INSTRUCTION TEST PART 3B
8I-D2AC	LE8/LP08 LINE PRINTER TEST
8I-D2BA	OPTICAL MARK CARD READER TEST
8I-D4CA	PDP 8I MEMORY PARITY IOT TEST
8I-D5DB	DF32 DISCLESS LOGIC TEST, MINIDICS
8I-D5FB	DF32D DISCLESS LOGIC TEST, MINIDISC
8I-D6AC	AX08 DIAGNOSTIC
8I-D6BB	CDP EXERCISER
8I-D6CE	KV8I DISPLAY DIAGNOSTIC
8I-D6DA	KV8I MULTIPLEX DISPLAY DIAGNOSTIC
8I-D8AC	DC08T1:DC08 OFF-LINE IOT AND DATA TEST
8I-D8AE	KW8I REAL TIME CLOCK
8I-D8BB	DC08T2-DC08 ON-LINE DATA EXERCISER
8I-D8EA	DC08-F AND DC08-H OFF LINE DIAGNOSTIC TEST
8I-D8FA	DC08-F AND DC08-H ON-LINE DIAGNOSTIC EXERCISER
8I-D8HA	DM04 BREAK MULT CONTROL PRIORITY

MAINDEC-8E-D0AB	PDP8E INSTRUCTION TEST 1
8E-D0BB	PDP8E INSTRUCTION TEST 2
8E-D0CC	8E ADDER TEST
8E-D0DB	RANDOM AND TEST

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8E-D0EB          RANDOM TAD TEST
8E-D0FC          RANDOM ISZ TEST
8E-D0GC          RANDOM DCA TEST
8E-D0HC          RANDOM JMP TEST
8E-D0IB          BASIC JMP-JMS TEST
8E-D0JC          RANDOM JMP-JMS TEST
8E-D0LB          KE8-E (EAE) INSTRUCTION TEST 1
8E-D0MB          KE8-E (EAE) INSTRUCTION TEST 2 MULTIPLY AND DIVIDE
8E-D0NA          JMP SELF TEST
8E-D0PC          DB8E INTERPROCESSOR BUFFER TEST(M8326 REV. D OR BELOW)
8E-D0RA          KE8-E EXTENDED MEMORY EXERCISER
8E-D0SA          DB8E INTERPROCESSOR BUFFER TEST (M8326 REV. E OR ABOVE)
8E-D1AB          MM8E 4K MEMORY CHECKERBOARD
8E-D1EC          MEMORY ADDRESS TEST
8E-D1FB          PDP8E EXRENDED MEMORY ADDRESS TEST
8E-D1GB          PDP8E MEMORY POWER ON/OFF TEST
8E-D1HB          PDP8E MEMORY EXTENSION AND TIME SHARE CONTROL TEST
8E-D1IB(1);(2)   MI8-E BOOTSTRAP DIAGNOSTIC(LOW,HIGH)
8E-D1JB(1);(2)   MR8-EA READ ONLY MEMORY TEST(LOW,HIGH)
8E-D1KA          MR8-EC ROM CONTENTS(TD8-E DECTAPE SYSTEM HANDLER)
8E-D2CA          HIGH SPEED READER/PUNCH TESTS
8E-D2DB          CM8E CARD READER TEST
8E-D2EB          CR8E CARD READER TEST
8E-D2FB          DECWRITER(LA30) CONTROL/EXERCISER TEST
8E-D3AB(1);(2)   TD8E DECTAPE DIAGNOSTIC
8E-D6AB          PDP8E XY8-E PLOTTER CONTROL AND DISPLAY DIAGNOSTIC PROGRAM
8E-D6CB          VC-8E DISPLAY DIAGNOSTIC
8E-D7AA          RAD8/3 DIAGNOSTIC EXERCISER
8E-D8AC          DK8E CLOCKS DIAGNOSTIC
8E-D8CA          REDUNDANCY CHECK


MAINDEC-X8-DIQAB-A    DEC/X8 USERS GUIDE MONITOR/BUILDER
        X8-DIPCA-A    DEC/X8 MODULE"HSRHSP", HIGH SPEED READER/PUNCH EXERCISER
        X8-DIDFA-A    DEC/X8 MODULE "DF32DS", DF32/DF32D DECDISK SYSTEM EXERCISER
        X8-DIKAC-A    DEC/X8 MODULE "OPERATE", OPERATE INSTRUCTION TEST
        X8-DIKAB-A    DEC/X8 MODULE "RANMRI", RANDOM MEMORY REFERENCE INTRUCTION EXERCISER
        X8-DILPA-A    DEC/X8 MODULE "PRINTER", PRINTER EXERCISER
        X8-DILKAD-A   DEC/X8 MODULE "NOTFUN", NON FUNCTIONAL IOT TEST
        X8-DIKAA-A    DEC/X8 MODULE "MRI08A", MEMORY REFERENCE INSTRUCTION TEST
        X8-DITCA-A    DEC/X8 MODULE "TC01DT", TC01/TC08 DECTAPE EXERCISER
        X8-DHKEA-A    DEC/X8 MODULE "EAEDP", KE8E DOUBLE PRECISION AND SAM INSTRUCTIONS EXERCISER
        X8-DIKEA-A    DEC/X8 MODULE "EAEALL", EAE EXERCISER OF MUY, DVI,SHL,LSR,ASR AND NMI INSTRUCTIONS
        X8-DIRFA-A    DEC/X8 MODULE "RF08DS", RF08 DISK YSTEM EXERCISER
        X8-DIFPA-A    DEC/X8 MODULE "FPP12"
        X8-DITCB-A    DEC/X8 MODULE "TC58MT", TC58 DECMAGTAPE EXERCISER
        X8-DIDKA-A    DEC/X8 MODULE "TIMERA", REAL TIME CLOCK ELAPSED TIME REPORTER, JOB DEAD CHECKER AND ROTATION
                      RANDOMIZER
        X8-DIRKA-A    DEC/X8 MODULE "RK8DS", RK8 DISK SYSTEM EXERCISER
        X8-DDTCA-A    DEC/X8 MODULE "TC12LT", TC12 LINCTAPE EXERCISER
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MAINDEC-08-DHKMA-A-D

PDP-8/E EXTENDED MEMORY DATA &
CHECKERBOARD TEST

ABSTRACT

THE PDP-8/E EXTENDED MEMORY DATA & CHECKERBOARD TEST IS DESIGNED TO DETECT MEMORY FAILURE DUE TO SENSE-LINE NOISE UNDER WORST CASE CONDITIONS. THE FOUR WORST CASE PATTERNS PROVIDED WILL GENERATE WORST CASE NOISE CONDITIONS IN ALL STANDARD AND SPECIALLY PURCHASED PDP-8/E CORE STACKS, AND WILL TEST SYSTEMS EQUIPPED WITH FROM 8K TO 32K WORDS OF CORE MEMORY. THE ALL 0'S AND ALL 1'S PATTERNS ARE PROVIDED TO IDENTIFY BASIC MEMORY FAILURES. AUTOMATIC PROGRAM RELOCATION IS PROVIDED IN ORDER TO TEST ALL MEMORY FIELDS FROM EACH MEMORY FIELD. TELETYPE PRINTOUTS ARE PROVIDED FOR ERROR IDENTIFICATION, AND THE OPERATOR IS GIVEN A DEGREE OF CONTROL OVER THE PROGRAM BY VARIOUS SWITCH REGISTER SETTINGS.

REQUIREMENTS

A PDP-8/E COMPUTER EQUIPPED WITH AT LEAST 8K OF CORE MEMORY.

STORAGE - THE PROGRAM OCCUPIES CORE LOCATIONS 0000 TO 4777 AND 6000 TO 7177 OF THE PRESENT FIELD.

LOADING - BINARY LOADER

STARTING PROCEDURE

SET THE SR TO THE IF AND DF OF THE FIELD THAT CONTAINS THE PROGRAM.
PRESS KEY EXTD ADDR LOAD.
SET THE SR EQUAL TO 0200.
PRESS KEYS ADDR LOAD, CLEAR, AND CONT. A SETUP SR MESSAGE WILL BE PRINTED.
PRESS KEY CONT.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES

SWITCH	0 (DOWN)	1 (UP)
SR00	CONTINUE AFTER ERROR	HALT AFTER ERROR
SR01	TYPEOUT ERRORS	INHIBIT ERROR TYPEOUTS
SR02	NORMAL	TTY BELL ON ERROR
SR03	RELOCATE PROGRAM	INHIBIT PROGRAM RELOCATION
SR04	NORMAL	CHANGE FIELD LIMITS
SR05	NORMAL	HALT AFTER CURRENT TEST

SR06-08 STARTING FIELD LIMIT (0-7)
SR09-11 ENDING FIELD LIMIT (0-7)

MAINDEC-08-DHKPA-A-D

KP8/E POWER FAIL/AUTO RESTART TEST

ABSTRACT

THIS DIAGNOSTIC IS A COMPLETE TEST OF THE PDP-8/E POWER FAIL OPTION WITH THE INTERVENTION OF THE OPERATOR.

REQUIREMENTS

PDP-8/E
KP8/E POWER FAIL OPTION

STORAGE - THE MAIN PROGRAM OCCUPIES THE FIRST THREE PAGES IN CORE.
2000 TO 3777 LOWER BUFFER
4000 TO 5777 HIGH BUFFER

LOADING - BINARY LOADER

STARTING PROCEDURE
SET SWITCH REGISTER TO 200
DEPRESS LOAD ADDRESS
SET CONTROL SWITCH TO SELECT DESIRED TEST.
DEPRESS CLEAR AND THEN DEPRESS CONTINUE
THE OPERATOR MUST NOW CAUSE POWER TO FAIL, EITHER BY
DIRECTLY TURNING THE POWER KEY OFF AND/OR BY THE USE
OF A POWER INTERRUPTER.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES
BITS 0-3 ARE USED FOR TEST SELECTION

BITS				
0	1	2	3	TEST NUMBER
-	-	-	-	
0	0	0	1	TEST 1
0	0	1	0	TEST 2
0	1	0	0	TEST 3
1	0	0	0	TEST 4

MAINDEC-08-DGV5A-A-D

VT05 TERMINAL DIAGNOSTIC

ABSTRACT
THIS DIAGNOSTIC CONTAINS A SERIES OF ROUTINES WHICH ALLOW VISUAL
INSPECTION OF THE PERFORMANCE OF THE VT05 ALPHANUMERIC DISPLAY TERMINAL.

REQUIREMENTS
PDP-8
VT05 ALPHANUMERIC DISPLAY TERMINAL
PT08 (OPTIONAL)
DC02 (OPTIONAL)

STORAGE - THE PROGRAM OCCUPIES 4K OF CORE.

LOADING - BINARY LOADER

STARTING PROCEDURE
NOTE: THE IOTS ARE SET TO RUN ON THE DC02, HOWEVER, IF THE
OPERATOR WISHES TO RUN THE VT05 IN THE PDP-8 CONSOLE SLOT OR
ON THE PT08, HE MAY DO SO BY CHANGING THE RECEIVER IOT DEVICE
SELECTION CODE CONTAINED IN BITS 6-11 OF LOCATION 100.

LOAD THE STARTING ADDRESS INTO THE ADDRESS SWITCHES
PRESS LOAD ADDRESS
SELECT SR SWITCH OPTIONS (SEE SECTION 6.)
PRESS START

TWO CONTROLS ARE PROVIDED FOR OPERATION OF THE PROGRAM VIA
THE CONSOLE DEVICE.

A. TYPING CTRL C (↑C) WILL RESULT IN THE TTY MESSAGE:

PATT PASSES

B. TYPING CTRL D (↑D) WILL TEMPORARILY INTERRUPT THE ROUTINE
IN PROGRESS, AND OUTPUT A DIRECTORY OF THE PATTERNS ON THE
CONSOLE DEVICE.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES

SR0=1 HALT AT THE END OF EACH PATTERN
SR0=0 RUN CONTINUOUSLY

SR1=1 LOOP THE CURRENT PATTERN
SR1=1 RUN EACH PATTERN ONCE

SR3=1 SWAP HALVES FOR PATTERN N
SR3=0 RUN PATTERN N NORMALLY

SR9-11=0	110 BAUD
" =0	150 BAUD
" =0	300 BAUD
" =1	600 BAUD
" =2	1200 BAUD
" =4	2400 BAUD

NOTE: IT IS EXTREMELY IMPORTANT THAT SR SWITCHES 9-11 BE SET
TO INDICATE THE SPEED AT WHICH THE VT05 IS RUNNING.
THEY DETERMINE THE NUMBER OF FILLER CHARACTERS (ASCII
CODE 0) TO BE INSERTED AFTER THE FOLLOWING:

MAINDEC-08-DHKLD-A-D

POP-8/E TELETYPE AND KL8 ASYNCHRONOUS
DATA CONTROL TESTS

ABSTRACT

THIS PROGRAM CONSISTS OF A PACKAGE OF TEST PROGRAMS FOR
TESTING THE KL8 LOGIC (EIA OR CURRENT) AND A TELETYPE, ONLY
ONE TELETYPE MAY BE TESTED AT A TIME. THE TELETYPE TO BE TEST-
ED CAN BE A KSR33, ASR33, KSR35, ASR35, OR KSR37.

THE TEST PROGRAMS ARE:

PRG0-BASIC TEST OF THE OUTPUT LOGIC (CURRENT AND EIA)
PRG1-BASIC TEST OF THE OUTPUT AND INPUT LOGIC (LOOP AROUND) (EIA)
PRG2-BASIC TEST OF INPUT LOGIC (USES TTY READER) (CURRENT)
PRG3-READER TEST

//

PRG4-PRINTER TEST
PRG5-PUNCH TEST
PRG6-KEYBOARD TEST
PRG7-COMBINED TEST
PRG10-READER EXERCISER, BINARY COUNT PATTERN
PRG11-PRINTER EXERCISER
PRG12-BINARY COUNT TAPE GENERATOR

REQUIREMENTS
PDP-8/E WITH AT LEAST 4K OF MEMORY
FOR EIA A JUMPER TO CONNECT INPUT TO OUTPUT, SEE TEST EQUIPMENT 7,3.
KSR33, ASR33, KSR35, ASR35 TO TEST AN 110 BAUD CURRENT OPTION.

STORAGE - LOCATIONS 0000 THROUGH 7600 ARE USED.

LOADING - BINARY LOADER

STARTING PROCEDURE
SET LOCATION 0020 TO:

0000 FOR KSR OR ASR 33 TELETYPE
0001 FOR KSR OR ASR 35 TELETYPE
0002 FOR KSR 37 TELETYPE

SET LOCATION 0021 AS FOLLOWS:

LOAD ADDRESS 0021.
SET SR 0 THROUGH 5 TO THE DEVICE CODE OF THE KEYBOARD/READER
TO BE TESTED.
(EG: READER CODE OF 03, SR0-5-03.
SET SR 6 THROUGH 11 TO THE DEVICE CODE OF THE PRINTER/PUNCH TO
BE TESTED.
(EG: PRINTER CODE OF 04, SR6-11-04.
PRESS DEPOSIT

SET LOCATION 0022 AS FOLLOWS:

LOAD ADDRESS 0022.
PLACE THE FOLLOWING IN THE SR:
0110 FOR 110 BAUD, OR
0150 FOR 150 BAUD, OR
0300 FOR 300 BAUD, OR
0600 FOR 600 BAUD, OR
1200 FOR 1200 BAUD, OR
2400 FOR 2400 BAUD, OR
PRESS DEPOSIT.

PRG0

INSURE THAT TELETYPE IS ON-LINE IF ON THE KL8 BEING TESTED.
INSURE THAT THERE IS PAPER IN TELEPRINTER.
LOAD ADDRESS 0200.
SET SR TO 0000.
PRESS CLEAR ON CONTINUE.

PROGRAM HALTS AT LOCATION 0236 TO PERMIT SETTING OF SR
OPTIONS. SET ANY DESIRED OPTIONS. NORMAL RUN IS WITH
SR=0000. PRESS CONTINUE.

PRG0 SR SPTIONS:

```
        SR0=1   HALT AT END OF ROUTINE, ROUTINE NUMBER IN AC.
        SR1=1   SELECT ROUTINE WHOSE NUMBER IS SET IN SR6 - SR11.
        SR2=1   LOOP PROGRAM.
        SR6 THROUGH SR11        ROUTINE NUMBER TO BE SELECTED.

        PROGRAM IS EXECUTED AND HALTS AT LOCATION 0300 PROGRAM END
        HALT, IF NO LOOP OPTIONS ARE SET, AND IF NO ERROR OCCURRED.

PRINTOUTS = YES

SWITCH REGISTER OPTIONS - YES


MAINDEC-08-DHDRA-A-D

DR8-EA 12 CHANNEL BUFFERED
DIGITAL INTERFACE

ABSTRACT
        THIS PROGRAM IS A DIAGNOSTIC AND EXERCISER FOR THE DR8-EA 12
        CHANNEL BUFFERED DIGITAL INTERFACE.  ALL FUNCTIONS ARE TESTED
        AND ERRORS ARE REPORTED BY HALTS AND/OR ERROR TYPEOUTS.

REQUIREMENTS
        PDP-8/E STANDARD COMPUTER WITH 4K OF CORE
        ASR-33 TELETYPE (OR EQUIVALENT)
        DR8-EA WITH TEST CABLE

STORAGE - THE PROGRAM USES LOCATION 0000-3377

LOADING - BINARY LOADER

STARTING PROCEDURE
        LOAD PROGRAM INTO MEMORY
        SET SWITCH REGISTER TO DESIRED STARTING ADDRESS
        LOAD ADDRESS
        CLEAR SWITCHES
        PRESS CLEAR AND CONTINUE

        FOR STARTING ADDRESS 200

        THE PROGRAM WILL TYPE "SET SR FOR DEVICE CODE AND CONT" AND
        THEN HALT.

        SET SWITCHES TO 00X WHERE X IS AN OCTAL
        NUMBER CORRESPONDING TO THE 3 LSB OF THE DEVICE SELECTOR CODE.
        PRESS CONTINUE.

        PROGRAM WILL RESPOND BY TYPING
        "SET SR FOR INTERRUPT JUMPERS AND CONT" AND THEN HALT.
        SET SWITCHES FOR ALL INPUT REGISTER BITS JUMPERED TO INTERRUPT.
        PRESS CONTINUE.

        PROGRAM WILL RESPOND BY TYPING
        "SET SR FOR FLIPFLOP JUMPERS AND CONT" AND THEN HALT.
        SET SWITCHES FOR ALL INPUT REGISTER FLIPFLOPS.
        PRESS CONTINUE.
```

PROGRAM WILL RESPOND BY TYPING
"SET SR FOR RUN" AND THEN HALT.
SET SWITCHES AS IN 4,2 OR 5,1
PRESS CONTINUE

PROGRAM WILL BEGIN TEST EXECUTION

PRINTOUTS - YES

SWITCH REGISTER OPTIONS
SR0=1, SUPPRESS ERROR HALT
SR1=1, SUPPRESS ERROR TYPEOUT
SR2=1, LOOP ON CURRENT TEST
SR3=1, LOOP WITH CURRENT DATA
SR4=1, SUPPRESS BELL OR TYPEOUT AT END OF PASS
SR5=1, SUPPRESS ITERATIONS
SR6=1, ESCAPE TO NEXT TEST ON ERROR

MAINDEC-08-DHADA-A-D

AD8E,AM8E A-D CONVERTER AND
MULTIPLEXER DIAGNOSTIC

ABSTRACT
THIS PROGRAM PERFORMS BASIC TESTS ON THE INPUT/OUTPUT CONTROL LOGIC AND MULTIPLEXER. THE ANALOG TESTS ARE DESIGNED TO PROVIDE A MEANS OF CALIBRATING THE CONVERTER AND CHECKING CONVERSION PARAMETERS.

REQUIREMENT
PDP-8/E WITH 4K CORE, ASR33 TELETYPE, AD8E A-D CONVERTER, (AM8E MULTIPLEXER OPTIONAL), ADJUSTABLE HIGH QUALITY VOLTAGE SOURCE, EDC MODEL MV105G OR EQUIVALENT.

NOTE: TO RUN MONOTINICITY TEST, A FUNCTION GENERATOR CAPABLE OF .1 CPS, SINE OR RAMP OUTPUT MUST BE USED.

STORAGE - MAINDEC RESIDES IN LOCATIONS 0000-4500.

LOADING - BINARY LOADER

STARTING PROCEDURE
LOAD 200.
PRESS CLEAR THEN CONTINUE, HALT WILL OCCUR.
SELECT OPTIONS FROM SWITCHES 0, 1, 2, 5.
IF SW5 IS PRESENT (1), SELECT TEST FROM SW8-11.
PRESS CONTINUE.
AFTER EACH PASS (12 SEC) "END OF LOGIC TEST"
WILL BE PRINTED.

NOTE: WITH SW5 DOWN AND SW2 UP, ANY ERROR WILL BE REPORTED ONCE, THEN PROGRAM WILL CONTINUE TO NEXT TEST.

STARTING ADDRESSES-

0201- IOT SCOPE LOOP

```
        0202-   DISPLAY CONVERTED VALVE IN A,C.
        0203-   EXTERNAL ENABLE WITH REAL TIME CLOCK (DK8EP,ES)
        0204-   MONOTINICITY TEST.
        0205-   RESOLUTION ACCURACY
        0206-   SUCCESSIVE READS
        0207-   MUX, NOISE TEST
        0210-   LAB8E SYSTEM TEST.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES
        SW0-    SUPPRESS ERROR MESSAGES AND "END LOGIC TEST"
                MESSAGE
        SW1-    HALT ON ERROR WITH PC DISPLAYED IN AC.
        SW2-    SCOPE LOOP OVERRIDE TO EXIT FROM LOOP ON
                ERROR AND PERMIT CONTINUANCE OF TEST.  ALSO
                HALTS WITH CONVERTED WORD IN AC FOR EXTERNAL
                ENABLE WHEN THERE IS NO ERROR.
        SW3-    ENABLES HALT DURING CALIBRATION ROUTINE.
                CONVERTED WORD IS DISPLAYED IN AC.
        SW4-    MUST BE SET TO RUN EXTERNAL ENABLE TEST.
        SW5-    ALLOWS OPERATOR TO EXPLICITLY SELECT ANY ONE
                OF THE LOGIC ROUTINES.


MAINDEC-08-DHKLC-A-D

MAINDEC-8/E-D2GA-D

ABSTRACT
        THIS DIAGNOSTIC FACILITATES THE CHECK-OUT OF THE KL8F DOUBLE
        BUFFERED ASNYCHRONOUS INTERFACE.  THIS IS A CLOSED LOOP TEST.
        A METHOD TO CONNECT EIA OUTPUT TO EIA INPUT IS REQUIRED,
        REFER TO TEST PROCEDURE M8652-0-3 FOR CONFIGURATION.
        ERROR HALTS AND SCOPE LOOPS ARE PROVIDED.

REQUIREMENTS
        PDP-8/E COMPUTER
        ASR-33 TELETYPE OR EQUIVALENT DEVICE
        M8652 QUAD MODULE
        ONE LOOP BACK PLUG #7008517
        IF LOOP BACK PLUG IS NOT AVAILABLE, CONNECT PINS
        E TO M, AND F TO J ON CONNECTOR J1 OF M8652 MODULE.

STORAGE - THE PROGRAM OCCUPIES MEMORY LOCATIONS 0000 TO 3000.

LOADING - BINARY LOADER

STARTING PROCEDURE
        LOAD STARTING ADDRESS 0200-DEPRESS CONTINUE.  PROGRAM
        WILL HALT AT LOCATION 0202.

        FIRST PROGRAM HALT (0202) IS TO ALLOW OPERATOR TO SELECT
        IOT STRUCTURE, THROUGH THE SWITCHES, FOR WHICH HIS M8652
        HAS BEEN JUMPERED TO OPERATE WITH.
        SWITCHES        SELECTS
        0-5             RECEIVE IOT
        6-11            TRANSMIT IOT
        FOR EXAMPLE; IF THE NUMBER 0304 WAS PLACED IN THE SWITCHES
```

THE IOT STRUCTURE WOULD BE:
RECEIVE = 603X
TRANSMIT = 604X
WHERE X=0-7
DEPRESS CONTINUE
PROGRAM WILL HALT AT LOCATION 0204.

THE SECOND PROGRAM HALT (0204) IS TO ALLOW THE OPERATOR TO PLACE IN THE SWITCH REGISTER (S.R.) THE NUMBER OF DATA BITS PER CHARACTER TO BE TRANSMITTED.
THERE ARE FOUR POSSIBLE COMBINATIONS:

S.R.=0037	(5 DATA BITS)
S.R.=0077	(6 DATA BITS)
S.R.=0177	(7 DATA BITS)
S.R.=0377	(8 DATA BITS)

DEPRESS CONTINUE
PROGRAM WILL HALT AT LOCATION 0207.

THE THIRD PROGRAM HALT (0207) ALLOWS THE OPERATOR TO SELECT THROUGH THE S.R. THE TEST TO BE RUN, BAUD RATE AT WHICH DATA IS TO BE TRANSFERRED, AND THE TOTAL NUMBER OF BITS (INCLUDING START, STOP, PARITY) EACH CHARACTER IS COMPOSED OF. FOR CONTROL SWITCH SETTINGS,
DEPRESS CONTINUE PROGRAM WILL NOW HALT ONLY IF AN ERROR IS ENCOUNTERED.

PRINTOUTS = YES

SWITCH REGISTER OPTIONS = YES

S.R. BIT(S)	SET AS	ACTION ON PROGRAM
0	0	STAY IN SCOPE LOOP
	1	EXIT SCOPE LOOP
1,2,3	0	RUN ALL TESTS
	1	TEST ONE ONLY
	2	TEST TWO ONLY
	3	TEST THREE ONLY
	4	TEST FOUR ONLY
	5	TEST FIVE ONLY
	6	TEST SIX ONLY
	7	TEST SEVEN ONLY
4,5	NOT USED	
6,7,8	0	7 BITS PER CHARACTER
	1	8 BITS PER CHARACTER
	2	9 BITS PER CHARACTER
	3	10 BITS PER CHARACTER
	4	11 BITS PER CHARACTER
	5	12 BITS PER CHARACTER
	6	NOT USED
	7	NOT USED
9,10,11	0	110 BAUD
	1	134.5 BAUD
	2	150 BAUD
	3	300 BAUD
	4	600 BAUD
	5	1200 BAUD

6	1800 BAUD
7	2400 BAUD

MAINDEC-08-DHMPA-A-D

PDP-8/E EXTENDED MEM
PARITY TEST

ABSTRACT

THE PDP-8/E EXTENDED MEMORY PARITY CHECKERBOARD DIAGNOSTIC IS DESIGNED TO DETECT PARITY FAILURES ON HALF-SELECTED LINES UNDER WORST CASE NOISE CONDITIONS. THE WORST CASE PATTERN PROVIDED WILL GENERATE WORST CASE NOISE CONDITIONS IN ALL PDP-8/E PARITY STACKS. ALSO, THE PARITY ERROR INTERRUPT AND THE PARITY DATA DECODING CIRCUITS ARE CHECKED FOR PROPER OPERATION. THIS PROGRAM WILL TEST SYSTEMS EQUIPPED WITH PARITY AND FROM 8K TO 32K WORDS OF CORE MEMORY. AUTOMATIC PROGRAM RELOCATION IS PROVIDED FOR ERROR IDENTIFICATION, AND THE OPERATOR IS GIVEN A DEGREE OF CONTROL OVER THE PROGRAM BY VARIOUS SR SETTINGS.

REQUIREMENTS

A PDP-8/E COMPUTER EQUIPPED WITH MEMORY PARITY AND AT LEAST 8K OF CORE MEMORY.

STORAGE - THIS PROGRAM OCCUPIES CORE LOCATION 0000 - 5177 AND 6400 - 6630 OCTAL.

LOADING - BINARY LOADER

STARTING PROCEDURE

SET THE SR TO THE INSTRUCTION FIELD AND DATA FIELD OF THE STACK WHICH CONTAINS THE PROGRAM.
PRESS KEY EXTD ADDR LOAD.
SET THE SR EQUAL TO 0200.
PRESS KEYS ADDR LOAD, CLEAR, AND CONT. A SETUP SR MESSAGE WILL BE PRINTED.
SET THE SR FOR DESIRED OPERATION.
PRESS KEY CONT.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES

SWITCH	0 (DOWN)	1 (UP)
SR00	CONTINUE AFTER ERROR	HALT AFTER ERROR
SR01	TYPEOUT ERRORS	INHIBIT ERROR TYPEOUTS
SR02	NORMAL	TTY BELL ON ERROR
SR03	RELOCATE PROGRAM	INHIBIT PROGRAM RELOCATION
SR04	NORMAL	CHANGE STACK LIMITS
SR05	NORMAL	HALT AFTER CURRENT TEST
SR06-08	STARTING STACK LIMIT (0-7)	
SR09-11	ENDING STACK LIMIT (0-7)	

MAINDEC-08-DHLSA-A

LS8E LINE PRINTER TEST

ABSTRACT

THE LINE PRINTER DIAGNOSTIC TEST PROGRAM IS DESIGNED TO TEST FOR CORRECT OPERATION OF THE CONTROL INTERFACE AND CORRECT CHARACTER GENERATION OF THE CENTRONICS MODEL 101 LINE PRINTER. THE NORMAL FLOW OF THIS DIAGNOSTIC PROGRAM IS TO SEQUENTIALLY TEST FIVE SECTIONS, WHEN A TEST SECTION IS ENTERED THE TITLE OF THE TEST SECTION WILL BE PRINTED ON THE TELETYPE.

REQUIREMENTS

ANY OF THESE PROCESSORS: PDP-8,8/I,8/L,8E OR PDP 12
CENTRONICS MODEL 101 LINE PRINTER
LS8E CONTROL INTERFACE
TELETYPE-ASCII KEYBOARD PRINTER

LOADING - BINARY LOADER

STARTING PROCEDURE

LOAD LINE PRINTER WITH LINE PRINTER PAPER
TURN ON POWER BY PRESSING ON/OFF SWITCH
SWITCH SHOULD LIGHT UP AFTER HAVING BEEN PRESSED.
AT THIS POINT ALL OTHER LIGHTS SHOULD BE OFF.
PRESS SELECT SWITCH
SELECT SWITCH SHOULD LIGHT UP AFTER HAVING BEEN PRESSED.
SELECT STARTING ADDRESS AND LOAD ADDRESS (START 0200)
PRESS START
(FOR A PDP-8/E:START=CLEAR, THEN CONT.)
PROGRAM WILL HALT AT ADDRESS 422.
AT THIS TIME SELECT A PROCESSOR AND ALL OTHER SWITCHES
(SEE SWITCH SETTINGS)
PRESS CONTINUE

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES

SW0=0 DO ONE PASS OF COMPLETE TEST AND HLT
SW0=1 LOOP ON COMPLETE TEST

SW1=0 PRINT ERROR MESSAGE
SW1=1 INHIBIT ERROR MESSAGE PRINT OUT

SW2=0 DON'T LOOP ON CURRENT TEST
SW2=1 LOOP ON CURRENT TEST

SW3=0 NORMAL TEST FLOW
SW3=1 REPEAT CURRENT TEST SECTION

SW4=0 NORMAL TEST FLOW
SW4=1 HLT AFTER COMPLETION OF SELECTED PRINT TEST

PROCESSOR SELECTION SWITCHES

SW8 05-06-07

001 PDP-8 OR PDP-8/I
010 PDP-8/L
011 PDP-12
100 PDP-8/E

TEST SECTION INHIBIT SWITCHES

SW8=0 DO THE BASIC IOT TEST
SW8=1 INHIBIT BASIC ITO TEST

SW9=0 DO THE FORMAT CONTROL CHARACTER TESTS
SW9=1 INHIBIT FORMAT CONTROL CHARACTER TESTS

SW10=0 DO THE CARACTER PRINT TESTS
SW10=1 INHIBIT CHARACTER PRINT TESTS

SW11=0 DO THE TIMING TESTS
SW11=1 INHIBIT TIMING TESTS

MAINDEC-08-DHRKA-A-D

RK8E DISKLESS CONTROL TEST

ABSTRACT
THE RK8E DISKLESS CONTROL TEST IS DESIGNED FOR THE PURPOSE OF CHECKOUT OF THE RK8E DISK CONTROL LOGIC NOT REQUIRING THE USE OF THE DISK DRIVE. THIS TEST SHOULD BE RUN WITH ALL EXISTING DRIVES SET TO THE LOAD POSITION.

REQUIREMENTS
PDP-8/E COMPUTER
AT LEAST 4K OF READ/WRITE MEMORY
ASR-33 TELETYPE OR EQUIVALENT
RK8E DISK CONTROL
RK05 DISK DRIVE

STORAGE - THE PROGRAM UTILIZES OR OCCUPIES LOCATIONS 0000 TO 7577 OF THE CURRENT FIELD.

STARTING PROCEDURE
REGULAR DISKLESS CONTROL TEST

SET THE SWITCH LABELED "RUN/LOAD" TO THE "LOAD" POSITION ON ALL DRIVES

SET THE SWTICH LABELED "ON/OFF" TO THE "ON" POSITION ON ALL DRIVES.

SET THE SWITCH REGISTER TO 0200 AND PRESS LOAD ADDRESS.

SET THE SWITCH REGISTER TO 0000.

SET SWR9-11 TO THE AMOUNT OF EXTENDED R/W MEMORY BANKS AND START THE COMPUTER RUNNING.

SET SWR1=1 IF THE OPERATOR DESIRES TO INHIBIT THE END OF TEST HALT AT LOCATION "ENDHLT".

SWR4=1 SHOULD ALWAYS BE USED TO STOP THE PROGRAM.

THE PROGRAM SHOULD PRINT THE FOLLOWING MESSAGE AT THE COMPLETION OF EACH SUCCESSFUL PASS APROX. EVERY 3.5 MINUTES.

"RK8E DISKLESS PASS COMPLETE"

PRINTOUTS = YES

SWITCH REGISTER OPTIONS = YES

SWR0=1	ENTER SCOPE LOOP, AFTER AN ERROR HALT AT LOCATION "ERHLT9" RAISING THIS SWITCH AND PRESSING KEY CONTINUE WILL CAUSE A SCOPE LOOP ON THE CURRENT TEST. IF SWR2=0 AND THE TEST IS STILL FAILING, THE ERROR BELL SHOULD RING INDICATING AN ERROR.
SWR1=1	INHIBIT END OF TEST HALT, AT THE COMPLETION OF THE TEST THE PROGRAM SHOULD HALT AT LOCATION "ENDHLT". RAISING THIS SWITCH WILL INHIBIT THE END OF TEST HALT.
SWR2=1	INHIBIT ERROR BELL ON SCOPE LOOP.
SWR3=1	GET ALL REGISTERS AFTER "ERHLT9", AFTER AN ERROR HALT AT LOCATION "ERHLT9". RAISING THIS SWITCH AND PRESSING KEY CONTINUE WILL RESULT IN THE TYPEOUT OF THE ABSOLUTE CONTENTS OF THE STATUS, COMMAND, CRC, LOWER DATA, AND SURFACE AND SECTOR REGISTERS.
SWR4=1	STOP PROGRAM OR TEST HALT, RAISING THIS SWITCH WILL HALT THE PROGRAM AT THE COMPLETION OF THE CURRENT TEST. IF POSSIBLE THIS SWITCH SHOULD ALWAYS BE USED TO STOP THE PROGRAM.
SWR9-11	AMOUNT OF EXTENDED BANKS OF MEMORY. AT INITIAL START OF THE PROGRAM, SWR9-11 INDICATES THE AMOUNT OF EXISTING EXTENDED MEMORY FIELDS AVAILABLE TO TEST.

MAINDEC-08-DHRKB-B-D

RK8E DRIVE CONTROL TEST

ABSTRACT

THE RK8E DRIVE CONTROL TEST IS DESIGNED FOR THE PURPOSE OF CHECKOUT OF THE RK8E DISK CONTROL LOGIC REQUIRING THE USE OF THE DISK DRIVE.

IN GENERAL, THE TEST IS AN INSTRUCTION TEST TO VERIFY BASIC OPERATION OF THE SEEK ONLY, WRITE DATA, READ DATA, WRITE ALL, AND READ ALL FUNCTIONS WITH ALL DRIVES ON THE CONTROL, SIMPLE COMPLEMENT DATA PATTERNS OF 2525 + 5252, 5252 + 2525, AND 0000 + 7777 ARE USED TO VERIFY ADDRESSING AND DATA

TRANSFERS TO AND FROM EACH INDIVIDUAL DRIVE.

REQUIREMENTS
PDP8/E COMPUTER
AT LEAST 4K OF READ/WRITE MEMORY
ASR-33 TELETYPE OR EQUIVALENT
RK8E DISK CONTROL
RK05 DISK DRIVE(S)

STORAGE - THE PROGRAM OCCUPIES OR UTILIZES LOCATION 0000 TO LOCATION 7577 OF THE CURRENT FIELD.

STARTING PROCEDURES
MAKE READY THE DISK DRIVE TO BE TESTED USING THE RK05 DRIVE CARTRIDGE MOUNTING PROCEDURE SECTION 5.2.

SET SWITCH LABELED "RUN/LOAD" TO THE "LOAD" POSITION ON ALL DRIVES NOT BEING TESTED.

SET SWITCH LABELED "ON/OFF" TO THE "ON" POSITION ON ALL DRIVES NOT BEING TESTED.

SET THE SWITCH REGISTER TO 0200 AND PRESS LOAD ADDRESS.

SET THE SWITCH REGISTER TO 0000.

SET SWR3=1 TO INDICATE "SINGLE DRIVE TESTING".

SET SWR10-11 TO THE DISK DRIVE TO BE TESTED AND START THE COMPUTER RUNNING.

THE PROGRAM SHOULD PRINT THE FOLLOWING MESSAGE AT THE COMPLETION OF EACH PASS.

"RK8E DRIVE CONTROL TEST PASS COMPLETE"

ALWAYS USE SWR4=1 FOR STOPPING THE TEST.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES

MAINDEC-08-DHRKC-A-D

RK8E DATA RELIABILITY PROGRAM

ABSTRACT
THE RK8E DATA RELIABILITY PROGRAM IS DESIGNED PRIMARILY AS AN ACCEPTANCE TEST TO VERIFY DISK DATA TRANSFERS WITHIN THE DISK SYSTEM.

THE "ACCEPT MODE" OF OPERATION VERIFIES THE CAPABILITY OF TRANSFERRING A TOTAL 3 X 10(9) BITS OF DATA TO AND FROM EACH INDIVIDUAL DISK DRIVE ON THE DISK SYSTEM.

THE "MANUAL INTERVENTION MODE" IS AVAILABLE AS A HARDWARE DEBUGGING AID TO ALLOW THE OPERATOR TO SELECT DATA PATTERNS, TRANSFER LENGTHS, AND ADDRESSING.

REQUIREMENTS
PDP8/E COMPUTER
AT LEAST 4K OF READ/WRITE MEMORY
ASR-33 TELETYPE OR EQUIVALENT
RK8E DISK CONTROL
RK05 DISK DRIVE(S)

STORAGE - THE PROGRAM OCCUPIES OR UTILIZES LOCATION 0000 TO LOCATION 7577 OF FIELD 0.

EXECUTION TIME - THE PROGRAM EXECUTION TIME (I.E. PASSING 3 X 10(9) BITS OF DATA ON A DISK DRIVE), IS APROX. 6 HOURS PER DISK DRIVE ON A 4K MEMORY SYSTEM OR APROX. 5 HOURS PER DISK DRIVE ON SYSTEMS WITH EXTENDED MEMORY.

STARTING PROCEDURE
RK8E DATA RELIABILITY (ACCEPT MODE)

MAKE READY ALL DRIVES TO BE TESTED.

SET SWITCH LABELED "RUN/LOAD" TO THE "LOAD" POSITION ON ALL DRIVES NOT BEING TESTED.

SET SWITCH LABELED "ON/OFF" TO THE "ON" POSITION ON ALL DRIVES NOT BEING TESTED.

SET THE SWITCH REGISTER TO 0200 AND PRESS LOAD ADDRESS.

SET THE SWITCH REGISTER TO 0000 AND PRESS START.

THE OPERATOR MAY SET SWR5=1 IF IT IS DESIRED TO HAVE THE PROGRAM AUTOMATICALLY DISCONNECT EACH DISK DRIVE AS EACH MAKE THEIR PASS COMPLETION. (NOTE: IF SWR5=0, ALL DISK DRIVES WILL CONTINUE TO RUN AFTER THEIR PASS COMPLETION)

THE TTY WILL PRINT THE FOLLOWING PROGRAM NAME AND QUESTION.

RK8E DATA RELIABILITY
AMOUNT OF EXTENDED R/W MEMORY (0-7)?

THE OPERATOR SHOULD THEN TYPE THE AMOUNT OF EXTENDED READ/WRITE MEMORY BANKS NUMBERED SEQUENCIALLY FROM BANK 0, AS INDICATED BY THE TTY QUESTIONS.

THE TTY WILL PRINT THE FOLLOWING QUESTION(S), ASKING THE DESIRED DISK DRIVE(S) TO BE USED IN TESTING.

EXERCISE DISK0? DISK1? DISK2? DISK3?

FOR THE QUESTION(S) ABOVE, TYPE Y FOR YES, IF IT IS DESIRED TO TEST THE DISK DRIVE IN QUESTION, OTHERWISE, TYPE N FOR NO.

THE TTY WILL PRINT THE FOLLOWING QUESTION.

ACCEPT MODE?

THE OPERATOR SHOULD THEN TYPE Y FOR YES TO RUN THE ACCEPTANCE MODE OF OPERATION.

THE TTY WILL PRINT THE FOLLOWING QUESTION.

ARE YOU SURE?

IF THE OPERATOR IS CERTAIN OF THE AMOUNT OF MEMORY, THE DISK DRIVE(S) SELECTED AND THE MODE OF OPERATION, TYPE Y FOR YES, TYPING N FOR NO WILL RESULT IN A REPEAT OF ALL MESSAGES AND QUESTIONS ENCOUNTERED THUS FAR.

THE PROGRAM SHOULD START TESTING THE DISK DRIVES(S) AND MEMORY SELECTED.

THE "STATUS-COMPLETE" TYPEOUT SHOULD OCCUR UPON PASS COMPLETION OF EACH DISK DRIVE, ALL OTHER TYPEOUTS OR HALTS WILL BE CONSIDERED AS AN ERROR CONDITION.

A SUCCESSFUL PASS COMPLETE ON A DISK DRIVE WILL BE CONSIDERED AS NO "WARD" ERRORS AND NO MORE THAN ONE (1) "SCFT" ERROR PER PASS COMPLETE.

IF ANY ERRORS DO OCCUR, THE OPERATOR SHOULD ACCESS SECTION 5 IN THIS DOCUMENTATION.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES

MAINDEC-08-DHRKD-A-D

RK8E DISK FORMATTER PROGRAM

ABSTRACT

THE RK8E DISK FORMATTER PROGRAM IS DESIGNED TO WRITE AND CHECK THE FORMAT OF THE COMPLETE DISK CARTRIDGE.

ONLY STANDARD DEC SURFACE FORMAT IS AVAILABLE (I.E. SECTORS NUMBERED IN THE NORMAL NUMERICAL SEQUENCE 0, 1, 2, 3, 4, 5, ETC.).

REQUIREMENTS

PDP-8/E COMPUTER
AT LEAST 4K OF READ/WRITE MEMORY
ASR-33 TELETYPE OR EQUIVALENT
RK8E DISK CONTROL
RK05 DISK DRIVE(S)

STORAGE - THE PROGRAM UTILIZES OR OCCUPIES LOCATIONS 0000 TO 3000 OF THE CURRENT FIELD.

STARTING PROCEDURE

FORMAT PROGRAM

MAKE READY ALL DRIVES TO BE FORMATTED.

SET SWITCH LABELED "RUN/LOAD" TO THE "LOAD" POSITION ON ALL DRIVES NOT BEING FORMATTED.

SET SWITCH LABELED "ON/OFF" TO THE "ON" POSITION ON ALL DRIVES NOT BEING FORMATTED.

SET THE SWITCH REGISTER TO 0200 AND PRESS LOAD ADDRESS.

SET THE SWITCH REGISTER TO 0000 AND PRESS KEY START (KEY START IS KEY CLEAR AND THEN KEY CONTINUE ON A PDP8/E, PDP8/F, OR PDP8/M) AND THE TTY SHOULD TYPE THE FOLLOWING PROGRAM NAME, INFORMATION, AND QUESTION.

```
RK8E DISK FORMATTER PROGRAM
FOR ALL QUESTIONS ANSWER Y FOR YES OR N FOR NO.
FORMAT DISK 0?
```

IF THE OPERATOR DESIRES TO FORMAT DISK 0, TYPE Y FOR YES, OTHERWISE, N FOR NO, ON THE TTY KEYBOARD, THE FOLLOWING QUESTION WILL THEN BE TYPED ON THE TTY.

```
FORMAT DISK 1?
```

IF THE OPERATOR DESIRES TO FORMAT DISK 1, TYPE Y FOR YES, OTHERWISE, N FOR NO, ON THE TTY KEYBOARD, THE FOLLOWING QUESTION WILL THEN BE TYPED ON THE TTY.

```
FORMAT DISK 2?
```

IF THE OPERATOR DESIRES TO FORMAT DISK 2, TYPE Y FOR YES, OTHERWISE, N FOR NO, ON THE TTY KEYBOARD, THE FOLLOWING QUESTION WILL THEN BE TYPED ON THE TTY.

```
FORMAT DISK 3?
```

IF THE OPERATOR DESIRES TO FORMAT DISK 3, TYPE Y FOR YES, OTHERWISE, N FOR NO, ON THE TTY KEYBOARD, THE FOLLOWING QUESTION WILL THEN BE TYPED ON THE TTY.

```
ARE YOU SURE?
```

TYPING N FOR NO WILL RESULT IN REPEATING ALL THE PREVIOUS QUESTIONS, TYPING Y FOR YES, WILL RESULT IN EXECUTION OF THE OPERATION SELECTED.

PROGRAM EXECUTION IS APROX. 80 SECONDS PER DISK DRIVE. AFTER ALL DISKS SELECTED HAVE BEEN FORMATTED AND CHECKED THE TTY WILL TYPE THE FOLLOWING PASS COMPLETE MESSAGE AND QUESTION.

```
RK8E DISK FORMATTER PASS COMPLETE
FORMAT SAME DISK(S) AGAIN?
```

IF THE OPERATOR DESIRES TO REPEAT THE OPERATION SELECTED, TYPE Y FOR YES, TYPING N FOR NO WILL RESULT IN A REPEAT OF THE INITIAL START-UP QUESTIONS.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - NO

MAINDEC-08-D01A-D

PDP-8 INSTRUCTION TEST - PART 2A

ABSTRACT
THIS PROGRAM IS A TEST OF THE MEMORY REFERENCE INSTRUCTIONS, OPERATE INSTRUCTIONS, AND INTERRUPT MODE. AN ATTEMPT IS MADE TO DETECT AND ISOLATE ERRORS TO ITS MOST BASIC FAULT.

REQUIREMENTS
PDP-8 PROCESSOR, KEYBOARD READER AND TELEPRINTER.

STORAGE - MEMORY LOCATIONS 20 8-5166 8.

LOADING - BINARY LOADER

EXECUTION TIME - 16 SECONDS

STARTING PROCEDURES
THE STARTING ADDRESS OF THE PDP-8 PART 2A INSTRUCTION TEST IS 1200.
SET 1200 IN THE SWITCH REGISTER AND PRESS THE LOAD ADDRESS KEY.
SET THE SWITCH REGISTER KEYS TO 7777 AND PRESS THE START KEY.

PRINTOUTS - NO

SWITCH REGISTER OPTIONS - NO

MAINDEC 08-D02B-D

PDP-8 INSTRUCTION TEST PART 2B

ABSTRACT
THIS PROGRAM IS A TEST OF THE 2S COMPLEMENT ADD (TAD) AND ROTATE LOGIC (RAL, RTL, RAR, RTR). RANDOM NUMBERS ARE USED IN THE TWOS ADD PORTION OF THE TEST AND SEQUENTIAL NUMBERS ARE USED IN THE ROTATE PORTION. PROGRAM CONTROL DEPENDS ON 1-OPERATOR MANIPULATION OF FOUR SWITCHES IN THE SWITCH REGISTER (BITS 0,

1,2,3). ERROR INFORMATION IS NORMALLY PRINTED OUT ON THE KEYBOARD PRINTER.

REQUIREMENTS
PDP-8 PROCESSOR-KEYBOARD READER

STORAGE - MEMORY LOCATIONS 20 8-4177 8.

LOADING - BINARY LOADER

STARTING PROCEDURE
THE STARTING ADDRESS OF THE TAD PORTION OF THE TEST IS 0200 8. THE STARTING ADDRESS OF THE ROTATE PORTION OF THE TEST IS 200 8. IF BIT 3 OF THE SWITCH REGISTER IS SET, IT AUTOMATICALLY CAUSES AN EXIT FROM THE TWOS ADD PORTION OF THE TEST TO THE ROTATE PORTION OF THE TEST.

SET EITHER 0200 8 IN THE SWITCH REGISTER TO START AT THE TWOS ADD PORTION OF THE TEST, OR SET 2000 8 IN THE SWITCH REGISTER TO

```
        START AT THE ROTATE PORTION OF THE TEST.
        PRESS THE LOAD ADDRESS KEY.
        PRESS THE START KEY.

PRINTOUTS = YES

SWITCH REGISTER OPTIONS = YES
        SWITCH 0        STOP ON ERROR (406 8 FOR TAD OR 2433 8 FOR ROTATE TEST).
        SWITCH 1        SCOPE MODE (REPEAT LOOP CAUSING THE ERROR).
        SWITCH 2        PRINT ERROR.
        SWITCH 3        LEAVE THE TWOS ADD TEST AND START THE ROTATE TEST.


MAINDEC-08-D04B-D

RANDOM JMP TEST

ABSTRACT
        THIS PROGRAM TESTS THE JMP INSTRUCTION OF THE PDP-8.  MOST OF
        MEMORY IS USED AS A JUMP FIELD WITH A RANDOM NUMBER GENERATOR
        SELECTING EACH JUMP FROM AND JUMP TO LOCATION.

REQUIREMENTS
        PDP-8 EQUIPPED WITH TELETYPE.

STORAGE = 0000, TO 0364.

LOADING = BINARY LOADER.

STARTING PROCEDURE
        SET SR TO 0200 AND PRESS LOAD ADDRESS.
        SET SR TO DESIRED MODE.  IF A PARTICULAR MEMORY LOCATION
        IS DESIRED FOR EITHER A "CONSTANT FORM" OR "CONSTANT TO", THIS
        MEMORY ADDRESS IS ENTERED INTO ONE OF THE LOCATIONS SHOWN BELOW:
        FROM 1  ADDRESS = 0116
        FROM    ADDRESS = 0115
        TO      ADDRESS = 0114
        NOTE:  ALWAYS MAKE (FROM1)=(FROM)-1
        PRESS START.

PRINTOUTS = YES

SWITCH REGISTER OPTIONS = YES
        SR0     HALT ON ERROR.

        SR2     HOLD JUMP FROM ADDRESSES CONSTANT.(1)
                SELECT RANDOM JUMP FROM ADDRESSES.(0)
```

```
        SR3     HOLD JUMP TO ADDRESSES CONSTANT.(1)
                SELECT RANDOM JUMP TO ADDRESSES.(0)

MAINDEC-08-D05B

RANDOM JMP-JMS TEST

ABSTRACT
        THIS IS A DIAGNOSTIC PROGRAM TO TEST THE JMS INSTRUCTION OF THE
        PDP-8,  RANDOM FROM AND TO ADDRESSES ARE SELECTED FOR
        EACH TEST,  THE JMP INSTRUCTION IS TESTED IN THAT EACH TEST RE-
        QUIRES A JMP TO REACH THE JMS.

REQUIREMENTS
        PDP-8 EQUIPPED WITH TELETYPE.

STORAGE - LOCATIONS 0000-0574

LOADING - BINARY LOADER

STARTING PROCEDURE
        SET SR TO 0200 AND PRESS LOAD ADDRESS
        IF IT IS DESIRED TO SET EITHER SR2 OR SR3, THE FROM OR TO
        ADDRESS MAY BE SPECIFIED BY ENTERING THE ADDRESS INTO THE LOCA-
        TIONS SHOWN BELOW.

                FROM = LOCATION 130
                TO   = LOCATION 126

        IF SR2 OR SR3 IS SET AFTER THE PROGRAM HAS BEEN STARTED, THE LAST
        ADDRESS TAKEN FROM THE RANDOM NUMBER GENERATOR IS USED REPEATEDLY.
        PUSH START.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES
        SR0     HALT ON ERROR.

        SR2     HOLD THE FROM ADDRESS CONSTANT(1).
                SELECT RANDOM FROM ADDRESSES(0).

        SR3     HOLD THE TO ADDRESS CONSTANT(1).
                SELECT RANDOM TO ADDRESSES(0).


MAINDEC-08-D07B

RANDOM ISZ TEST
```

ABSTRACT

THIS PROGRAM IS WRITTEN TO TEST THE ISZ INSTRUCTION OF THE PDP-8. AN ISZ INSTRUCTION IS PLACED IN A FROM LOCATION, AND A TO LOCATION, CONTAINS THE OPERAND. PART 1 OF THE PROGRAM SELECTS FROM, TO, AND OPERAND FROM A RANDOM NUMBER GERERATOR, WITH THE OPTION OF HOLDING ANY OR ALL CONSTANT. PART 2 USES A FIXED SET OF FROM, TO, AND OPERAND NUMBERS.

REQUIREMENTS

ONE PDP-8 EQUIPPED WITH TELETYPE.

STORAGE - THIS PROGRAM USES LOCATIONS 0000-7600 8.

LOADING - BINARY LOADER

STARTING PROCEDURE

SET SR (SWITCH REGISTER) TO 0037 AND PRESS LOAD ADDRESS.
SET SR TO DESIRED MODE OF OPERATION; FOR MOST RUNS; SR9=1
ALLOWS THE MOST TESTING IN THE LEAST AMOUNT OF TIME.
FOR FIXED FROM, TO, OR OPERAND USAGE, THE FIXED NUMBER MAY BE SELECTED AND ENTERED INTO THE MEMORY LOCATIONS SHOWN BELOW:
FROM = 0002
TO = 0020
OPERAND = 0021
PUSH START.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES

SR0 = HALT ON ERROR

SR1 = ELIMINATE ERROR PRINTOUTS

SR3 = FIXED FROMS (1)
RANDOM FROMS (0)

SR4 = FIXED TOS (1)
RANDOM TOS (0)

SR5 = FIXED OPERAND (1)
RANDOM OPERAND (0)

SR9 = DO ONE ISZ ONLY

SR11 = DO PART 2 (1)->SR3, 4, 5 MUST BE 0S.
DO PART 1 (0)

MAINDEC-08-D0BA

PDP-8 INSTRUCTION TEST EAE

ABSTRACT
THE DIVIDE OVERFLOW DETECTION HARDWARE, AND THE DIVIDE AND MULTIPLY HARDWARE ARE TESTED BY USING A PSEUDO RANDOM-NUMBER GENERATOR TO PRODUCE THE PARAMETERS FOR EACH TEST, A SOFTWARE SIMULATED DIVIDE AND MULTIPLY ARE USED TO TEST THE RESULTS OF THE HARDWARE DIVIDE AND MULTIPLY.

REQUIREMENTS
PDP-8 PROCESSOR, EAE TYPE 182 OPTION, KEYBOARD READER AND TELEPRINTER

STORAGE - MEMORY LOCATIONS 0010 8 -2551 8

LOADING - BINARY LOADER

STARTING PROCEDURE
THE STARTING ADDRESS OF THE PDP-8 PART 3B INSTRUCTION TEST IS 0200 8,
SET 0200 8 IN THE SWITCH REGISTER KEYS AND PRESS THE LOAD ADDRESS KEY,
SET 5000 8 IN THE SWITCH REGISTER KEYS AND PRESS THE START KEY.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - NO.

MAINDEC-08-D0UA

FAMILY OF 8 RANDOM ADD ROTATE TEST

ABSTRACT
THIS PROGRAM IS A TEST OF THE 2'S COMPLEMENT ADD (TAD) ROTATE LOGIC (RAL, RTL, RAR, RTL) AND INDEX THE ACCUMULATOR (IAC); RANDOM NUMBERS ARE USED IN ALL SIX (6) TESTS. PROGRAM CONTROL DEPENDS ON OPERATOR MANIPULATION OF SIX (6) SWITCHES IN THE SWITCH REGISTER (BITS 0,1,2,3,4,5). ERROR INFORMATION IS NORMALLY PRINTED OUT ON THE TELEPRINTER.

REQUIREMENTS
PDP-5, 8, 8/S, 8/I, 8/L LINC-8 OR PDP-12 PROCESSOR
TELETYPE WITH A RENDER.

STORAGE - MEMORY LOCATIONS 0001 - 1676

LOADING - BINARY LOADER

STARTING PROCEDURE
THE STARTING ADDRESS OF THIS TEST IS 0200 8. THE NORMAL SWITCH SETTING IS 0000 8. DURING NORMAL OPERATION A BELL WILL RING AFTER EVERY PASS THRU THE PROGRAM (ABOUT 20 SECONDS ON AN 8, 8/I, 8/L, LINC-8 OR PDP-12).

SET SWITCH REGISTER TO 0200 8

PRESS LOAD ADDRESS

SET SWITCH REGISTER TO 0000

PRESS TO START KEY

PRINTOUTS = YES

SWITCH REGISTER OPTIONS = YES

SR00 = 1	SUPPRESS ERROR HALT
SR01 = 1	SUPPRESS TYPE OUT
SR02 = 1	SCOPE LOOP IN CURRENTLY FAILING TEST
SR03 = 1	STAY IN CURRENT NOT FAILING TEST
SR04 = 1	DO NOT CHANGE TEST DATA.
SR05 = 1	SUPPRESS BELL

MAINDEC-08-D1AC

PDP-8 MEMORY POWER ON/OFF TEST

ABSTRACT
THIS PROGRAM IS A MEMORY DATA VALIDITY TEST TO BE USED AFTER A SIMULATED POWER FAILURE.

REQUIREMENTS
PDP-8 PROCESSOR, KEYBOARD READER, AND TELEPRINTER

STORAGE = MEMORY LOCATIONS 0001 8--7477 8

LOADING = BINARY LOADER

STARTING PROCEDURE
LOAD ADDRESS 0014 AND PRESS START.
THE PROGRAM SHOULD THEN HALT AT 0042 8.
LOAD ADDRESS 0001 AND PRESS START.
THE PROGRAM SHOULD NOW LOOP.

PRINTOUTS = NO

SWITHCH REGISTER OPTIONS - NO

MAINDEC-08-D1EC

PDP-8, 8/I EXTENDED MEMORY
CHECKERBOARD

ABSTRACT
THE PDP-8, 8/I EXTENDED MEMORY CHECKERBOARD DIAGNOSTIC IS DE-
SIGNED TO PROVIDE WORST CASE HALF-SELECT NOISE CONDITIONS IN
ORDER TO DETERMINE THE OPERATIONAL STATUS OF CORE MEMORY.
FOUR DATA PATTERNS, AND THEIR COMPLEMENTS, ARE WRITTEN AND CHECKED
FOR ERROR. THE PATTERNS PROVIDED WILL GENERATE THE WORST CASE
NOISE CONDITIONS FOR A PDP-8 OR 8/I EQUIPPED WITH STANDARD OR
SPECIALLY PURCHASED CORE STACKS, AND WILL TEST SYSTEMS EQUIPPED WITH
FROM 8K TO 32K WORDS OF CORE MEMORY. AUTOMATIC PROGRAM RELOCATION
IS PROVIDED IN ORDER TO TEST ALL MEMORY STACKS FROM EACH STACK.
TELETYPE PRINT-OUTS ARE PROVIDED FOR ERROR IDENTIFICATION.
ALSO, THE OPERATOR IS GIVEN A DEGREE OF CONTROL OVER THE PRO-
BY VARIOUS SR SETTINGS.

REQUIREMENTS
A STANDARD PDP-8 OR 8/I EQUIPPED WITH AT LEAST 8K WORDS OF
CORE MEMORY.

STORAGE - THE PROGRAM OCCUPIES LOCATIONS 0010 TO 3334.

LOADING - BINARY LOADER

STARTING PROCEDURE
IMMEDIATELY AFTER STARTING FROM ADDRESS 200 OR 207, THE PROGRAM
WILL PRINT TEST LIMITS. THE OPERATOR MUST THEN SPECIFY, VIA THE
TELETYPE KEYBOARD, THE AMOUNT OF CORE MEMORY TO TEST,
FOLLOWED BY A CARRIAGE RETURN.
THE FOLLOWING RULES GOVERN THE AMOUNT OF MEMORY TO TEST:
TYPE TWO OCTAL NUMBERS, SEPARATING THE NUMBERS WITH A COMMA.
THE FIRST NUMBER SIGNIFIES THE LOWWEST ORDER 4K STACK TO
TEST; THE SECOND SIGNIFIES THE HIGHEST ORDER.
IF A TYPING ERROR IS MADE, PRESS THE RUB-OUT KEY.
SET THE SR TO 200; PRESS LOAD ADDRESS, AND THEN START.
THE MESSAGE TEST LIMITS WILL BE PRINTED. SPECIFY THE LIMITS VIA KEYBOARD.
THE MESSAGE SETUP SR WILL BE PRINTED. SET THE SR TO 0000 8,
AND PRESS THE CARRIAGE RETURN KEY.
THE PROGRAM WILL PERFORM ALL FOUR TESTS ON ALL OF CORE MEMORY
SPECIFIED, AFTER WHICH, AUTOMATIC PROGRAM RELOCATION TAKES PLACE.

```
PRINTOUTS = YES

SWITCH REGISTER OPTIONS = YES
        SR01 = INHIBIT ERROR PRINTOUT,
        SR02 = BELL ON ERROR
        SR03-06 = TEST SELECTION
        SR07 = INHIBIT PROGRAM RELOCATION
        SR11 = CHANGE TEST LIMITS AND SR,
```

MAINDEC-08-D1GD

PDP-8 8I, 8S EXTENDED MEMORY CONTROL

ABSTRACT

THIS PROGRAM TESTS THE EXTENDED MEMORY CONTROL LOGIC FOR PROPER OPERATION. IT MAY BE USED WITH A PDP-8, 8I, OR 8S EQUIPPED WITH A MINIMUM OF 4K OF EXTENDED MEMORY. THE PROGRAM EXERCISES AND TESTS THE CONTROL IOT'S; THE ABILITY TO REFERENCE ALL FIELDS FROM 0; PROGRAM INTERRUPT AND INTERRUPT INHIBIT; AUTO-INDEXING IN EACH FIELD; AND A SPECIAL TEST FOR THE PDP-8/I WHICH TESTS THE PRESENCE OF A FALSE MEMORY PULSE WHEN A NON-EXISTENT MEMORY FIELD IS REFERENCED.

ERRORS ENCOUNTERED DURING RUNNING WILL RESULT IN A PROGRAM HALT. THE HALT LOCATIONS ARE LABELED, AND THE ERROR MAY BE IDENTIFIED BY REFERENCING THE PROGRAM LISTING OR TABLE OR ERROR HALTS.

REQUIREMENTS

A STANDARD PDP-8, 8/I OR 8/S EQUIPPED WITH AN EXTENDED MEMORY CONTROL, AND AT LEAST 4K OF EXTENDED MEMORY.

STORAGE - THE PROGRAM REQUIRES 2400(8) LOCATIONS OF CORE MEMORY.

LOADING - BINARY LOADER.

STARTING PROCEDURE

WITH THE PROGRAM IN MEMORY; SET THE SWITCH REGISTER TO 0200 OCTAL.
PRESS LOAD ADDRESS.
SET SR 8 TO A 1 IF A PDP-8/I IS BEING USED; OTHERWISE, SET SR 8 TO A 0.
PLACE THE OCTAL NUMBER OF EXTENDED MEMORY FIELDS AVAILABLE IN SR 9, 10 AND 11. THIS VALUE MAY VARY FROM 1 TO 7 ONLY.
PRESS START
THE PROGRAM WILL RUN UNTIL AN ERROR IS DETECTED, OR STOPPED BY THE OPERATOR.
THE TTY BELL IS RUNG ONCE AFTER ONE COMPLETE PASS OF THE PROGRAM.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES

MAINDEC-08-D1HA

PDP-8, 8/I, EXTENDED MEMORY

ADDRESS TEST

ABSTRACT

THE PDP-8, 8/I EXTENDED MEMORY ADDRESS TEST TESTS ALL OF MEMORY NOT OCCUPIED BY THE PROGRAM TO MAKE SURE THAT EACH LOCATION CAN BE UNIQUELY ADDRESSED. THIS IS PERFORMED BY A SERIES OF FOUR TESTS. THE FIRST TWO TESTS WRITE THE ADDRESS AND COMPLEMENT ADDRESS OF EACH MEMORY LOCATION INTO ITSELF, AND THEN CHECKS THE CONTENTS OF EACH LOCATION TO MAKE SURE EACH IS CORRECT. THE THIRD TEST FIRST SETS ALL OF MEMORY NOT OCCUPIED BY THE PROGRAM TO ALL ONES, AND THEN WRITES A WORD OF ALL ZEROES, EXCEPT FOR ONE BIT, INTO EACH LOCATION AND CHECKS FOR ERROR. THE FOURTH TEST IS SIMILAR EXCEPT THAT A WORD OF ALL ONES, EXCEPT FOR ONE BIT, IS WRITTEN INTO EACH LOCATION AND CHECKS FOR ERROR.

REQUIREMENTS

A STANDARD PDP-8 OR 8/I WITH A MINIMUM OF 8K WORDS OF CORE MEMORY.

STORAGE - THE PROGRAM REQUIRES LOCATIONS 0010 TO 2534 OCTAL.

LOADING - BINARY LOADER

STARTING PROCEDURE

IMMEDIATELY AFTER STARTING FROM ADDRESS 200 OR 207, THE PROGRAM WILL PRINT "TEST LIMITS". THE OPERATOR MUST THEN SPECIFY, VIA THE TELETYPE KEYBOARD, THE AMOUNT OF CORE MEMORY TO TEST, FOLLOWED BY A CARRIAGE RETURN.
THE FOLLOWING RULES GOVERN THE AMOUNT OF MEMORY TO TEST:
TYPE TWO OCTAL NUMBERS, SEPARATING THE NUMBERS WITH A COMMA.
THE FIRST NUMBER SIGNIFIES THE LOWEST ORDER 4K STACK TO TEST;
THE SECOND SIGNIFIES THE HIGHEST ORDER.
IF A TYPEING ERROR IS MADE, PRESS THE RUB-OUT KEY.
SET THE SR TO 200; PRESS LOAD ADDRESS, AND THEN START.
THE MESSAGE "TEST LIMITS" WILL BE PRINTED. SPECIFY THE LIMITS, VIA KEYBOARD.
THE MESSAGE "SETUP SR" WILL BE PRINTED. SET THE SR TO 0000(8), AND PRESS THE CARRIAGE RETURN KEY.
THE PROGRAM WILL PERFORM ALL FOUR TESTS ON ALL OF CORE MEMORY SPECIFIED, AFTER WHICH, AUTOMATIC PROGRAM RELOCATION TAKES PLACE.

PRINTOUTS - YES

SWITCH REGISTER OPTION - YES

SR00 - HALT AFTER TEST OR ERROR.
SR01 - INHIBIT ERROR PRINTOUT.
SR02 - BELL ON ERROR
SR03-06 - TEST SELECTION.
SR09 - INHIBIT PROGRAM RELOCATION
SR11 - CHANGE TEST LIMITS AND SR.

MAINDEC-08-D1KB-D

KP8I/KR01 POWER FAIL TEST

ABSTRACT
THIS DIAGNOSTIC IS A COMPLETE TEST OF THE PDP-8 AND PDP-8/I
POWER FAIL OPTION WITH THE INTERVENTION OF THE OPERATOR.

REQUIREMENTS
PDP-8 OR PDP-8/I
KP8/I POWER FAIL OPTION (EIGHT I)
KR01 POWER FAIL OPTION (EIGHT)

STORAGE - THE MAIN PROGRAM OCCUPIES THE FIRST THREE PAGES IN CORE.

LOADING - BINARY LOADER

STARTING PROCEDURE
SET SWITCH REGISTER TO 200
DEPRESS LOAD ADDRESS
SET SWITCH REGISTER TO DESIRED TEST.
DEPRESS START
THE OPERATOR MUST NOW CAUSE POWER TO FAIL, EITHER BY DIRECTLY
TURNING THE POWER KEY OFF AND/OR BY THE USE OF A POWER INTERRUPTER.

PRINTOUTS - NO

SWITCH REGISTER OPTIONS - YES

0	1	2	3	
0	0	0	1	TEST 1
0	0	1	0	TEST 2
0	1	0	0	TEST 3
0	0	0	0	TEST 4
1	0	0	0	COMPUTER WITH EAE

MAINDEC-08-D1L0

BASIC PDP-8, 8/I MEMORY CHECKERBOARD

ABSTRACT
THE PDP-8, 8/I MEMORY CHECKERBOARD DIAGNOSTIC TESTS MEMORY FOR
CORE FAILURE ON HALF-SELECTED LINES UNDER WORST CASE CONDITIONS.
ITS USE IS INTENDED FOR BASIC 4K MEMORY SYSTEMS.

REQUIREMENTS
A STANDARD PDP-8 OR 8/I

STORAGE - THERE ARE TWO VERSIONS OF THIS MAINDEC. THE LOW END PROGRAM
OCCUPIES LOCATIONS 0005 THROUGH 0150 OCTAL, AND TESTS MEMORY
FROM 151 THROUGH 7700 OCTAL.
THE HIGH END PROGRAM OCCUPIES LOCATIONS 7430 TO 7573 OCTAL, AND
TESTS MEMORY FROM 0000 TO 7400 OCTAL.

```
LOADING - RIM LOADER.

STARTING PROCEDURE
        STARTING ADDRESSES
        0005 LOW END CHECKERBOARD
        7430 HIGH END CHECKERBOARD
        WITH THE PROGRAM IN MEMORY; SET THE SWITCH REGISTER TO THE STARTING
        ADDRESS, 0005 FOR LOW END OR 7430 FOR HIGH END;
        PRESS LOAD ADDRESS.
        SET THE SWITCH REGISTER TO ONE OF THE FOUR SETTINGS TO OBTAIN THE
        CORRECT PATTERN.  FOR MOST PDP-8'S THIS WILL BE 0100.  FOR MOST
        PDP-8/I'S, THE SETTING WILL BE 0101.
        PRESS START.
        THE PROGRAM WILL RUN UNTIL AN ERROR IS DETECTED, OR STOPPED
        BY THE OPERATOR.

PRINTOUTS - NO

SWITCH REGISTER OPTIONS - YES
        0100    THIS SETTING IS USED FOR THE STANDARD PDP-8 CORE UNIT.

        0101    THIS SETTING IS USED FOR THE STANDARD PDP-8/I CORE UNIT.

        0000
                THESE ARE FOR SPECIAL CORE UNITS FROM OTHER SUPPLIERS.
        0001



MAINDEC-08-D1MA-D

MEMORY ADDRESS TEST

ABSTRACT
        THE MEMORY ADDRESS TEST CHECKS FOR PROPER MEMORY ADDRESS SELECTION
        ON THE PDP-8.

REQUIREMENTS
        STANDARD PDP-8 COMPUTER.

STORAGE - THE LOW VERSION OCCUPIES LOCATIONS 0000-0222;  THE HIGH VERSION
        OCCUPIES LOCATIONS 7400-7575, 0-3.

LOADING - RIM LOADER.

STARTING PROCEDURE
        STARTING ADDRESSES
        0004 LOW STORAGE RESTART 0000
        7400 HIGH STORAGE
        LOAD THE STARTING ADDRESS INTO THE PROGRAM COUNTER;
        SET THE SWITCH REGISTER TO 4000, IF HALT ON ERROR IS DESIRED;
        PUSH START;

PRINTOUTS - NO

SWITCH REGISTER OPTIONS - NO
```

MAINDEC-08-D2AA-D(D)

FAMILY-OF-8 TELETYPE TESTS
THROUGH PT08, LT08, OR DC02
INTERFACE

ABSTRACT

THIS PROGRAM CONSISTS OF A PACKAGE OF TEST PROGRAMS FOR TESTING A TELETYPE CONNECTED TO A PT08, LT08, OR DC02 INTERFACE. ONLY ONE TELETYPE MAY BE TESTED AT A TIME, THE PROGRAM RUNS IN A FAMILY-OF-8 SYSTEM, OR IN A PDP-12.

THE TELETYPE TO BE TESTED CAN BE A KSR33, ASR33, KSR35, ASR35, OR KSR37.

THE TEST PROGRAMS ARE:

PRG0 - BASIC INPUT TESTS (USES TTY READER)
PRG1 - BASIC OUTPUT TESTS (USES TTY PRINTER)
PRG2 - READER TEST
PRG3 - PRINTER TEST
PRG4 - PUNCH TEST
PRG5 - KEYBOARD TEST
PRG6 - COMBINED TEST
PRG7 - READER EXERCISER, BINARY COUNT PATTERN
PRG10 - PRINTER EXERCISER
PRG11 - BINARY COUNT TAPE GENERATOR.

REQUIREMENTS

FAMILY-OF-8 SYSTEM OR PDP-12, WITH PT08, LT08, OR DC02 INTERFACE.

<SR33, ASR33, KSR35, ASR35, OR KSR37 TELETYPE.

SOTRAGE - LOCATIONS 0000 THROUGH 6777 ARE USED.

LOADING - BINARY LOADER

STARTING PROCEDURE

BEFORE ANY PROGRAM CAN BE RUN, THE PROGRAM MUST HAVE THE FOLLOWING INFORMATION:

TYPE OF TELETYPE (33, 35, OR 37),
DEVICE CODES ASSIGNED.

TO PROVIDE THIS INFORMATION, PROCEED AS FOLLOWS:

SET LOCATION 0020 TO:
1) 0000 FOR KSR OR ASR 33 TELETYPE
2) 0001 FOR KSR OR ASR 35 TELETYPE
3) 0002 FOR KSR37 TELETYPE

SET LOCATION 0021 AS FOLLOWS:

LOAD ADDRESS 0021.
SET SR0 THROUGH 5 TO THE DEVICE CODE OF THE KEYBOARD/READER TO BE TESTED.
SET SR6 THROUGH 11 TO THE DEVICE CODE OF THE PRINTER/PUNCH TO BE TESTED.
PRESS DEPOSIT.
INSURE THAT TELETYPE IS ON-LINE.

LOAD BINARY COUNT PATTERN TEST TAPE IN READER.

TURN ON READER.

LOAD ADDRESS 0200.

SET SR TO 0000.

IF TESTING THROUGH A DC02, SET SR0 TO 7 TO THE UNIT
TO BE TESTED. SET SR0 FOR UNIT 0, OR SR1 FOR UNIT 1,
ETC. ONLY ONE UNIT MAY BE SELECTED.

PRESS START.

PROGRAM HALTS AT LOC 0240 TO PERMIT SETTING OF SR OPTIONS.
SET ANY DESIRED OPTIONS. NORMAL RUN IS WITH SR=0000.
PRESS CONTINUE.

PRG0 SR OPTIONS:

SR0 = HALT AT END OF ROUTINE, ROUTINE NUMBER IN AC.
SR1 = SELECT ROUTINE WHOSE NUMBER IS SET IN SR6-SR11.
SR2 = LOOP PROGRAM
SR6 THROUGH SR11 - ROUTINE NUMBER TO BE SELECTED.

PROGRAM IS EXECUTED AND HALTS AT LOC 0302, PROGRAM
END HALT, IF NO "LOOP" OPTIONS ARE SET, AND IF NO
ERRORS OCCUR.

PRINTOUTS = YES

SWITCH REGISTER OPTIONS = YES

MAINDEC-08-D2EA-D

PDP-8 HIGH SPEED READER TEST

ABSTRACT

THIS PROGRAM TESTS THE PERFORMANCE OF THE SPEED PERFORATED
TAPE READER AND CONTROL BY SCANNING A CLOSED-LOOP TEST TAPE FOR
ACCURACY OF TRANSMISSION. THE READER CONTROL IS TESTED FOR
CORRECT OPERATION WITH THE PDP-8 INTERRUPT SYSTEM.

AN AUXILIARY PROGRAM INCLUDED WITH THE TEST PUNCHES A TAPE FROM
WHICH THE TEST LOOP CAN BE MADE.

REQUIREMENTS

STANDARD PDP-8
PC01 READER CONTROL

STORAGE - THE TEST PROGRAM OCCUPIES STORAGE LOCATION 0001-0110.

LOADING - RIM LOADER

STARTING PROCEDURE

STARTING ADDRESSES:
0020---START OF READER TEST PROGRAM

0100---START OF AUXILIARY PUNCH PROGRAM

TO START THE AUXILIARY PUNCH PROGRAM, SET THE SR TO 0100, PRESS LOAD ADDRESS, THEN START. WHEN ENOUGH TAPE HAS BEEN PRODUCED (ABOUT 20-24 INCHES), PRESS STOP AND REMOVE THE TAPE FROM THE PUNCH BIN

MAKE A CLOSED LOOP OF THIS TAPE BY OVERLAPPING THE ENDS.

PLACE THE TEST LOOP IN THE HIGH SPEED READER, AND TURN ON THE READER POWER SWITCH.

SET THE SR TO 0020, AND PRESS LOAD ADDRESS.

SET THE SR ACCORDING TO THE READING SPEED DESIRED. IF YOU WANT MAXIMUM SPEED, SET THE SR TO 0000.

PRESS START

PRINTOUTS = NO

SWITCH REGISTER OPTIONS = NO

MAINDEC-08-D2FC-DN

HIGH SPEED READER TEST

ABSTRACT

THIS A DIAGNOSTIC PROGRAM FOR THE DIGITRONICS 2500 AND THE PC01 HIGH SPEED PAPER TAPE READERS USING CONTROL LOGIC TYPE 750C. THE PROGRAM IS DIVIDED INTO THREE PARTS, THE FIRST OF WHICH IS A TEST TAPE GENERATOR THAT PUNCHES TEST TAPES FOR PARTS TWO AND THREE ON THE HIGH SPEED PUNCH. PART TWO IS A SERIES OF SPECIFIC TESTS WITH MODULE ISOLATION PROVIDED FOR ERROR SITUATIONS. PART THREE READS A PRESELECTED TAPE PATTERN WITH THE CHOICE OF RANDOM OR FIXED BLOCK LENGTHS AND STALLS BETWEEN BLOCKS.

REQUIREMENTS

STANDARD PDP-8
TYPE DT2500 OR TYPE PC01 HIGH SPEED PAPER TAPE READER AND 750C CONTROL LOGIC.

STORAGE = THE PROGRAM USES LOCATION 0000 - 3315.

LOADING = BINARY LOADER

STARTING PROCEDURE

STARTING ADDRESSES

0200 TEST TAPE GENERATOR
0300 LOGIC TESTS
1625 READ BINARY-COUNT PATTERN OR ALTERNATE 1S AND 0S PATTERN
2000 READ ALL-SAME-CHARACTER PATTERN

TEST TAPE GENERATOR (PART1)

A. TO PUNCH TAPE ON THE TELETYPE PUNCH INSTEAD OF THE HIGH SPEED PUNCH ENTER 6041 INTO 0221 AND 6046 INTO 0223.

B. SET SR TO 0200, PRESS LOAD ADDRESS. SET SR TO DESIRED CONFIGURATION, THEN PRESS START. TAPE IS PUNCHED UNTIL STOPPED.

C. TO MAKE A CLOSED LOOP FROM THE TEST TAPE, THE PUNCHED PATTERN MUST BE MAINTAINED AT THE SPLICE.

LOGIC TEST (PART2)

A. PLACE AN ALL 0S TEST TAPE IN THE HIGH SPEED READER.

B. SET SR TO 0300, PRESS LOAD ADDRESS. SET SR TO DESIRED CONFIGURATION, THEN PRESS START.

NOTE: HALT ON ERROR SWITCH SR0 ONLY TO TESTS 5, 6 AND 11 WHICH PROVIDE ERROR PRINTOUTS INSTEAD OF ERROR HALTS.

C. THE PROGRAM HALTS AT THE COMPLETION OF TEST 1, PC=0317. THIS IS AN ILLEGAL INSTRUCTION TEST AND ANY TAPE MOVEMENT DURING TEST 1 IS AN ERROR CONDITION. PRESS CONTINUE TO GO ON. PRESS START TO REDO TEST 1.

D. THE PROGRAM HALTS AT TEST 10. PC=1125. PRESS START.

E. WHEN TEST 11 IS REACHED, THE PROGRAM LOOPS IN THIS TEST. THIS IS A SYNC CHARACTER RECOGNITION TEST WHICH IS A PREREQUISITE TO PART 3.

TAPE READ TEST (PART3)

A. LOAD TEST TAPE IN HIGH SPEED READER.

B. FOR TAPE PATTERNS OF ALL THE SAME CHARACTER ENTER THE DESIRED CHARACTER INTO MEMORY LOCATION 0035. SET SR TO 2000 AND PRESS LOAD ADDRESS. SET SR TO DESIRED CONFIGURATION, THEN PRESS START. SKIP TO PARAGRAPH E. FOR OTHER TAPE PATTERNS OMIT THIS PARAGRAPH AND GO TO C.

C. SET SR TO 1625, PRESS LOAD ADDRESS. SET SR TO DESIRED CONFIGURATION. IF SR6 IS A 1 (SELECT BLOCK SIZE), ENTER THE DESIRED BLOCK SIZE INTO LOCATION 0064 BEFORE PRESSING START. THE PROGRAM READS THIS BLOCK OF CHARACTERS AT FULL SPEED, THEN STALLS.

IF SR7 IS A 1 (SELECT STALL), ENTER THE DESIRED STALL INTO LOCATION 2151 BEFORE PASSING START. THIS WILL BE THE STALL BETWEEN BLOCKS. TO CALCULATE THE STALL LENGTH CONVERT THE STALL NUMBER TO DECIMAL AND MULTIPLY BY 0,1 MS.

IN EITHER CASE, IF NO ENTRY IS MADE, THE LAST BLOCK SIZE OR STALL GENERATED THE RANDOM NUMBER GENERATOR IS USED.

PUSH START.

D. THE PROGRAM READS THE TEST TAPE UNTIL IT FINDS AN ALL-ZERO CHARACTER, THEN IT PRINTS AN IN SYNC MESSAGE AND HALTS.

PRESS START TO RESYNC.
PRESS CONTINUE TO GO ON.

PRINOUTS - YES

SWITCH REGISTER OPTIONS - YES

SR0	PUNCH ALTERNATE 1S AND 0S	
SR1	PUNCH BINARY COUNT	
SR2	PUNCH ALL SAME CHARACTER AS SPECIFIED BY SR4-SR11	
SR0	STOP ON ERROR(1) PRINT ON ERROR(0)	
SR1	SCOPE MODE	
SR4	LOOP ON TESTS 2-9	
SR6	PRINT READING SPEED DURING TEST 11	
SR7	PRINT TAPE ACCELERATION TIME DURING TEST 11	
SR10 AND SR11	00 01 11	DT2500 PC01 MODEL 1 PC01 MODEL 2
SR0	STOP ON ERROR(1) PRINT ON ERROR(0)	
SR1	SCOPE MODE, IGNORE ERRORS	
SR2	PRINT ON ERROR(1) PRINT ERRORS AT END OF BLOCK(0)	
SR3	RESYNC TAPE IF 10 ERRORS IN ONE BLOCK	
SR6	SELECT BLOCK SIZE(1) RANDOM BLOCK SIZE(0)	
SR7	SELECT STALL(1) RANDOM STALL(0)	
SR8	RESYNC TAPE AT THE END OF EACH BLOCK	
SR9	READ ALTERNATE 1S AND 0S TAPE	
SR10	READ BINARY-COUNT TAPE	
SR11	READ A TAPE OF ALL THE SAME CHARACTER	

MAINDEC-08-D2HC-D

FAMILY OF 8 TYPESETTING
CONFIGURATION TESTS

ABSTRACT

THE FAMILY-OF-8 TYPESETTING CONFIGURATION TESTS CONSIST OF A PACKAGE OF PROGRAMS USED TO TEST AND ADJUST THE PP67A HIGH-SPEED PUNCH, THE PR68A HIGH-SPEED READER, AND THEIR CONTROL LOGIC. ANY ONE OF UP TO 16 READERS OR UP TO 16 PUNCHES MAY BE TESTED AT ONE TIME. THERE ARE 14 INDIVIDUAL PROGRAMS IN THE PACKAGE, NUMBERED

FROM 00 TO 15 (OCTAL). PROGRAM SELECTION IS ACCOMPLISHED THROUGH THE TELETYPE KEYBOARD.

THE AVAILABLE PROGRAMS ARE:

PRG0 BASIC READER AND READER CONTROL LOGIC TEST; USES ALL 0S TEST TAPE.

PRG1 BASIC PUNCH AND PUNCH CONTROL LOGIC TEST.

PRG2 READER TEST. BINARY COUNT PATTERN

PRG3 PUNCH TEST. BINARY COUNT PATTERN

PRG4 PUNCH VERIFY. BINARY COUNT PATTERN

PRG5 PUNCH TEST. RANDOM CHARACTERS

PRG6 PUNCH VERIFY. RANDOM CHARACTERS

PRG7 COMBINED READER AND PUNCH TEST. BINARY COUNT PATTERN

PRG10 READ AMPLIFIER ADJUSTMENT LOOP. 1S AND 0S TAPE USED.

PRG11 READ 6, STALL 40 MS, READER ADJUSTMENT LOOP.

PRG12 "CHANGE READER UNIT" DELAY ADJUSTMENT LOOP.

PGR13 CONTINUOUS PUNCH LOOP. SR4-SR11 ARE PUNCHED CONTINUOUSLY.

PRG14 1S AND 0S TEST TAPE GENERATER.

PRG15 "PUNCH OUT OF TAPE" SWITCH ADJUSTMENT LOOP.

REQUIREMENTS

STANDARD PDP-8, PDP-8/S.

ASR 33/35 TELETYPE

ONE OR MORE PP67A PUNCHES

ONE OR MORE PR68A READERS

DEPENDING ON NUMBER OF PUNCHES AND READERS, ONE OF THE FOLLOWING CONTROLS:

PA68A (1 PUNCH, 1 READER)

PA60A (1 - 8)

PA60B (1 - 16)

STORAGE - LOCATIONS 0000 THROUGH 4164 ARE USED.

LOADING - BINARY LOADER

STARTING PROCEDURE

SR0 HALT AT ROUTINE END. ROUTINE NUMBER IN AC.

SR1 SELECT ROUTINE WHOSE NUMBER IS SET IN SR8 - SR11.

SR2 LOOP PROGRAM.

SR3 0 = HALT ON ERROR, 1 = DO NOT HALT ON ERROR.

SR4 SKIP TEST AFTER ERROR.

SR5 ENTER SCOPE LOOP AFTER ERROR.

SR8
THROUGH
SR11 ROUTINE NUMBER TO BE SELECTED.

STARTING ADDRESSES (PRG0)

THIS PROGRAM STARTS AT LOCATION 0200.

INSURE THAT THE TELETYPE IS ON-LINE.

LOAD DESIRED READER WITH ALL 0S TEST TAPE, PREFERABLY THE TAPE SHOULD BE SPLICED INTO A LOOP.

LOAD ADDRESS 0200, PRESS START.

REPLY TO TELEPRINTER REQUESTS.

PROGRAM HALTS AT LOC 0275 TO PERMIT SETTING OF SR OPTIONS. SET DESIRED OPTIONS AND PRESS CONTINUE.

THE PROGRAM RUNS AND HALTS AT PROGRAM END HALT; AT LOC 0341, UNLESS PREVENTED FROM ENDING BY ERRORS, OR SR OPTIONS.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES

MAINDEC-08-D20A

CR03 G.D.I. CARD READER TEST

ABSTRACT
THE PROGRAM TESTS THE CR03 CARD READER FOR CORRECT ALPHA-NUMERIC AND BINARY OPERATIONS. IT ALSO TESTS CONTROL INTERRUPT AND TIMING.

REQUIREMENTS
PDP-8 OR 8/S OR 8/I WITH CR03 G.D.I. CARD READER
CR03 ALPHA-NUMERIC CARD DECK
CR03 BINARY CARD DECK

LOADING - BINARY LOADER

STARTING PROCEDURE
STARTING ADDRESSES

0200 8 = DATA TESTS (PDP-8 OR 8/I)
0201 8 = DATA TESTS (PDP-8/S)
0202 8 = STATIC IOT TESTS

```
        0700 8 = SCOPE LOOP

        STATIC IOT TEST

        PLACE A CARD DECK IN INPUT HOPPER
        TURN ON CARD READER POWER
        DEPRESS MOTOR START
        AT THIS POINT THE ONLY RED LIGHT TO BE ON SHOULD BE READ STOP.
        REFERENCE G,D,I. MANUAL TO REMEDY OTHER RED LIGHT ERROR CONDITIONS.
        LOAD ADDRESS 202 8
        DEPRESS START
        PROGRAM WILL PRINT "IOTS OK" IF TEST RUNS.  PROGRAM WILL HALT IF TEST
        FAILS.  REFERENCE SYMBOLIC LISTING AND COMMENTS FOR APPROPRIATE
        ERROR DESCRIPTION.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES
        AC SW   0 = 0   TEST ALPHA-NUMERIC DECK
                0 = 1   TEST BINARY DECK
                1 = 0   SUPPRESS DATA ERROR TYPEOUT
                1 = 1   PRINT DATA ERROR
                2 = 0   SUPPRESS HALT AFTER DATA ERROR
                2 = 1   HALT AFTER DATA ERROR
                3 = 0   HALT AT END OF TEST DECK
                3 = 1   CONTINUE TO NEXT TEST DECK WITHOUT HALT.


MAINDEC-08-D2PE-D

FAMILY-OF-8 ASR 33/35
TELETYPE TESTS PART 1

ABSTRACT
        THE FAMILY-OF-8 ASR33/35 TELETYPE TESTS PART 1 IS THE FIRST
        PART OF A TWO PART PACKAGE USED TO TEST THE ASR33, ASR33TY,
        OR ASR35 TELETYPE WHEN ATTACHED TO A FAMILY-OF-8 SYSTEM.

        PART 1 CONTAINS NINE SELECTABLE PROGRAMS NUMBERED FROM 0 TO 10
        (OCTAL). THE PROGRAMS ARE SELECTED BY MEANS OF THE SWITCH REGISTER (SR).

        THE PROGRAMS AVAILABLE ARE:

        PRG0    BASIC INPUT LOGIC TESTS

        PRG1    BASIC OUTPUT LOGIC TESTS

        PRG2    READER TEST

        PRG3    TEST TAPE GENERATOR,  PUNCHES TAPE WITH CHARACTERS STORED
                IN LOCATIONS 0021 AND 0022.

        PRG4    TEST TAPE GENERATOR,  PUNCHES BINARY COUNT PATTERN
                TEST TAPE.

        PRG5    READER EXERCISER,  READS BINARY COUNT PATTERN TAPE
                IN RANDOM LENGTH BLOCKS, AND WITH FIXED STALLS BETWEEN
                CHARACTERS.  THE STALL IS DETERMINED AT RANDOM.
```

PRG6 READER EXERCISER. READS BINARY COUNT PATTERN TAPE. FIXED STALL BETWEEN CHARACTERS. STALL COUNT IS TAKEN FROM LOC 0023.

PRG7 READER EXERCISER. READS TAPE PUNCHED WITH ANY 2 TEST* CHARACTERS. RANDOM LENGTH BLOCKS AND FIXED STALL BETWEEN CHARACTERS. THE STALL IS DETERMINED AT RANDOM.

PRG10 READER EXERCISER. READS TAPE PUNCHED WITH ANY 2 TEST CHARACTERS. FIXED STALL BETWEEN CHARACTERS. STALL COUNT TAKEN FROM LOC 0023.

PRG11 ASR33TY AUTOMATIC READER OPTION TEST. CHECKS FOR CORRECT RESPONSE TO READER ON. AND READER OFF COMMANDS.

PRG12 ASR33TY AUTOMATIC PUNCH OPTION TEST. CHECKS FOR CORRECT RESPONSE TO PUNCH ON AND PUNCH OFF COMMANDS.

REQUIREMENTS
STANDARD PDP-8/S, PDP-8 OR PDP8/I WITH ASR33, ASR33TY, OR ASR35 TELETYPE.

STORAGE - LOCATIONS 0000 THROUGH 2341 ARE USED.

LOADING - BINARY LOADER

STARTING PROCEDURE (PRG0)
INSURE TELETYPE IS ON-LINE.

LOAD BINARY COUTN PATTERN TEST TAPE IN READER.

TURN ON READER.

LOAD ADDRESS 0200.

SET SR TO 0000.

PRESS START

PROGRAM HALTS AT LOC 0232 TO PERMIT SETTING OF OPTIONS.

SELECT DESIRED OPTIONS, IF ANY, IN SR. FOR NORMAL RUN SR SHOULD BE 0000. PRESS CONTINUE.

PROGRAM IS EXECUTED AND HALTS AT LOC 0274, PROGRAM END HALT, IF NO LOOP OPTIONS ARE SELECTED AND IF NO ERRORS OCCUR.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES
SR0 HALT AT END OF ROUTINE NUMBERS IN AC.

SR1 SELECT ROUTINE WHOSE NUMBER IS SET IN SR6 THROUGH SR11.

SR2 LOOP PROGRAM.

SR6 THROUGH SR11 ROUTINE NUMBER TO BE SELECTED.

MAINDEC-08-D2QD-D

FAMILY OF 8 ASR33/35
TELETYPE TESTS, PART 2

ABSTRACT

THE FAMILY-OF-8 ASR33/35 TELETYPE TESTS, PART 2 IS THE SECOND PART OF A 2 PART PACKAGE USED TO TEST THE ASR33 OR ASR35 TELETYPE WHEN ATTACHED TO A FAMILY-OF-8 SYSTEM.

PART 2 CONTAINS NINE SELECTABLE PROGRAMS NUMBERED FROM 0 TO 10 (OCTAL). THE PROGRAMS ARE SELECTED BY MEANS OF SWITCH REGISTER (SR).

THE AVAILABLE PROGRAMS ARE:

PRG0 PRINTER TEST

PRG1 PUNCH TEST

PRG2 KEYBOARD TEST

PRG3 COMBINED READER, PRINTER, PUNCH TEST

PRG4 PRINTER EXERCISER. PRINTS LINES OF CHARACTERS STORED IN LOC 0021 AND 0022. NO STALLS.

PRG5 SAME AS PRG4, BUT STALLS BETWEEN CHARACTERS.

PRG6 PUNCH EXERCISER. PUNCHES AND READ CHECKS DATA BLOCKS OF DATA STORED IN LOC 0021 AND 0022. NO STALLS.

PRG7 SAME AS PRG6, BUT RANDOM STALLS BETWEEN CHARACTERS PUNCHED.

PRG10 PUNCH EXERCISER. PUNCHES AND READ CHECKS BLOCKS OF BINARY COUNT PATTERN. RANDOM STALLS BETWEEN CHARACTERS PUNCHED.

REQUIREMENTS

STANDARD PDP-8/S, PDP-8, OR PDP-8/I WITH ASR33 OR ASR35 TELETYPE.

STORAGE - LOCATIONS 0000 THROUGH 5173 ARE USED.

LOADING - BINARY LOADER

STARTING PROCEDURE

INSURE TELETYPE IS ON-LINE.

TURN OFF TELETYPE READER AND PUNCH.

LOAD ADDRESS 0200.

SET SR TO 0000.

PRESS START.

PROGRAM HALTS AT LOC 0232 TO PERMIT SETTING OF OPTIONS.

SELECT DESIRED OPTIONS, IF ANY, IN SR. FOR NORMAL RUN SR SHOULD

BE 0000. PRESS CONTINUE.

PROGRAM IS EXECUTED AND HALTS AT PROGRAM END HALT AT LOC 0274, UNLESS PREVENTED FROM ENDING, BY SR OPTIONS.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES

SR0 HALT AT END OF ROUTINE, ROUTINE NUMBER IN AC.

SR1 SELECT ROUTINE WHOSE NUMBER IS SET IN SR6 THROUGH SR11.

SR2 LOOP PROGRAM.

SR6 THROUGH SR11 ROUTINE NUMBER TO BE SELECTED.

MAINDEC-08-D2UA-D

PA 60C DIAGNOSTIC

PA60C DIAGNOSTIC

THE PA60C DIAGNOSTIC IS DESIGNED TO EMULATE THE TYPE-SETTING PROGRAM IN ITS USE OF THE NON-TORN TAPE ALLOTTING LOGIC PA60C.

STARTING THE PROGRAM AT "300" CAUSES A BINARY COUNT TAPE TO BE PUNCHED OUT ON ONE OF THE 6-LEVEL BRPE PUNCHES NORMALLY ON THE SYSTEM. THE BINARY COUNT TAPE IS SUBSEQUENTLY USED TO TEST THE READERS.

EACH READER TO BE TESTED SHOULD BE LOADED WITH A BINARY COUNT TAPE. STARTING THE PROGRAM AT LOCATION "200" STARTS THE TEST. THE PROGRAM WILL SCAN THE READERS LOOKING FOR ONE WHICH IS UNAVAILABLE AND HAS A TAPE IN IT. WHEN A READER IS FOUND WITH TAPE 1 BINARY COUNT SEQUENCE (I.E. 1-77 PUNCHES) IS READ AND CHECKED. IF A BAD CHARACTER IS READ THE PROGRAM WILL HALT DISPLAYING THE CHARACTER IN THE "AC". AFTER ONE BINARY COUNT SEQUENCE HAS BEEN CHECKED, THE PROGRAM WILL AUTOMATICALLY PROCEED TO LOOK FOR ANOTHER READER.

MAINDEC-08-D3BD-D

TC01* BASIC EXERCISER

ABSTRACT

THE TC01 BASIC EXERCISER IS A SERIES OF TEST PROGRAMS THAT MAY BE USED TO GAIN A HIGH DEGREE OF CONFIDENCE IN THE DATA HANDLING ABILITY OF A TC01 DECTAPE CONTROL AND ONE TO EIGHT TU55 DECTAPE TRANSPORTS. THE BASIC EXERCISER CONSISTS OF SEVERAL BASIC ROUTINES THAT MAY BE INDIVIDUALLY SELECTED; EACH ROUTINE WILL OPERATE ON ANY CONFIGURATION OF ONE TO EIGHT DRIVES. THESE ROUTINES INCLUDE A BASIC MOTION ROUTINE, SEARCH FIND ALL BLOCKS TEST, BASIC SEARCH ROUTINE, START/STOP/TURNAROUND TEST, BASIC WRITE/READ DATA TEST WITH EIGHT SELECTABLE PATTERNS, AND A PARITY GENERATION AND CHECKING TEST. THE OPERATION OF THE BASIC MOTION ROUTINE AND THE BASIC SEARCH ROUTINE ARE CONTROLLED BY KEYBOARD

INPUT, ALSO, A WRITE DATA SCOPE LOOP, READ DATA SCOPE LOOP, AND A SEARCH SCOPE LOOP ARE PROVIDED TO KEEP THE TAPE MOVING FROM END ZONE TO END ZONE.

REQUIREMENTS
PDP-8 (STANDARD)
TC21 *DECTAPE CONTROL
ONE TO EIGHT TU55 DECTAPE TRANSPORTS

STORAGE - THE PROGRAM OCCUPIES MOST OF MEMORY ADDRESS FROM 0000 TO 6377 AND UTILIZES THREE BUFFER AREAS.

LOADING - BINARY LOADER

STARTING PROCEDURE
STARTING ADDRESSES OF ROUTINES

ADDRESS	ROUTINE
0200	BASIC MOTION ROUTINE
0201	SEARCH FIND ALL BLOCKS
0202	BASIC SEARCH ROUTINE
0203	START/STOP/TURNAROUND
0204	WRITE/READ DATA TEST
0205	PARITY GENERATION TEST
0206	WRITE DATA SCOPE LOOP
0207	READ DATA SCOPE LOOP
0210	SEARCH SCOPE LOOP

PLACE THE SELECT ADDRESS FOR THE ROUTINE DESIRED IN THE SWITCH REGISTER AND PRESS LOAD ADDRESS.

SET SWITCH REGISTER BITS 0 TO 7 TO SELECT DRIVES. (ANY CONFIRURATION EXCEPT ALL 0S IS VALID.)

PRESS START. THE STATIC REGISTER TEST WILL BE RUN ON STATUS REGISTER A, AND B. THE PROCESSOR SHOULD HALT AT ADDRESS 0223 WITH BITS 0 TO 7 OF THE SWITCH REGISTER DISPLAYED IN THE AC.

A HALT AT ADDRESS 0311 INDICATES BITS 0 TO 7 WERE ALL 0S. SELECT DRIVES AND PRESS CONTINUE TO RECOVER.

SET ALL SWITCH REGISTER BITS TO 0, OR AS DESIRED AND PRESS CONTINUE.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES

SWITCH	DRIVE
0	8
1	1
2	2
3	3
4	4
5	5
6	6
7	7

MAINDEC-08-D3EB-D

TC01 EXTENDED MEMORY EXERCISER

ABSTRACT
TC01 EXTENDED MEMORY EXERCISER IS A TEST PROGRAM FOR THE PDP-8 COMPUTER WHICH TESTS THE TRANSFER TO DATA BETWEEN THE TC01 DECTAPE CONTROL AND EXTENDED MEMORY FIELDS (MORE THAN 4K). IT DOES THIS BY STORING A DATA PATTERN IN AN EXTENDED MEMORY FIELD, TRANSFERRING THE DATA ONTO DECTAPE AND THEN READING THE DATA BACK INTO THE FIELD AND CHECKING IT FOR CORRECT TRANSFER.

REQUIREMENTS
STANDARD PDP-8 COMPUTER
TC01 DECTAPE CONTROL WITH AT LEAST 1 TRANSPORT (TU55)
183 MEMORY EXTENSION CONTROL WITH AT LEAST 1 MEMORY MODULE (184)

STORAGE - THE PROGRAM OCCUPIES THE FIRST 6 PAGES OF BANK 0 AND USES 2000 TO 5777 OF EACH MEMORY BANK FOR DATA STORAGE.

LOADING - BINARY LOADER

STARTING PROCEDURE
SET SR TO 00200, DEPRESS "LOAD ADDRESS".
SET SR 9 TO 11
DEPRESS "START".

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES

SR	SET AS	ACTION
0		UNIT SELECT BITS FOR
1		DECTAPE TRANSPORT
2		
6		NUMBER OF ADDITIONAL
7		MEMORY FIELDS (MUST BE
8		NON-ZERO)
9	1	HALT ON ERROR
	0	DON'T HALT ON ERROR
10	1	DON'T PRINT ERRORS
	0	PRINT ERRORS
11	1	DON'T RING BELL ON ERROR
	0	RING BELL ON ERROR

MAINDEC-08-D3FC-D

INCREMENTAL TAPE DELAY TEST

ABSTRACT
THIS TEST PROGRAM IS DESIGNED TO GIVE THE TECHNICIAN THE TIME OF THE FOUR DELAYS IN THE INCREMENTAL TAPE LOGIC. THE PROGRAM CONSISTS

OF FOUR PARTS, PART ONE TESTS THE 250 MS DELAY WHICH OCCURS WHEN A SETUP TO WRITE COMMAND IS GIVEN FOLLOWING A BACKSPACE.

PART 2 TESTS THE 10 MS DELAY WHICH OCCURS WHEN A SETUP TO WRITE COMMAND IS GIVEN FOLLOWING A LOAD FWD, READY TO READ.

PART 3 TESTS THE 1 MS DELAY WHICH OCCURS WHEN A SKIP ON GAP DETECT COMMAND IS GIVEN FOLLOWING A READ FORWARD COMMAND.

PART 4 TESTS A 10 MS DELAY ALONG WITH A 1 MS DELAY. FOR THIS TEST POWER ON THE TRANSPORT HAS TO BE TURNED OFF (OFF LINE), ITS EXECUTION IS A READ FORWARD COMMAND AND WAIT FOR READ DONE. THE 10 MS DELAY IS FIRED WHEN A READ FORWARD COMMAND IS GIVEN AND WAITING FOR READ DONE FLAG.

REQUIREMENTS
AN 8/I OR 8/L WITH 4K STORAGE
ASR-33 TELETYPE
TR-02 INCREMENTAL TAPE AND CONTROL LOGIC

STORAGE - 4K CORE IS SUFFICIENT FOR TEST

LOADING - BINARY LOADER

STARTING PROCEDURE
STARTING ADDRESS

200 8	PART 1	250 MS	DELAY TEST
210 8	PART 2	10 MS	DELAY TEST
220 8	PART 3	1 MS	DELAY TEST
230 8	PART 4	COMBINATION OF 10 MS AND 1 MS	DELAY TEST

LOAD 0200
SET SR OPTIONS
PRESS START

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES
SR0 = 1 INHIBIT PRINTOUT
SR1 = 1 HLT ON COMPLETION
SR10 = 1 9 TRACK DRIVE
SR11 = 1 TEST DRIVE ONE

MAINDEC-08-D3RA-D

DECTREX 1

TC01 RANDOM EXERCISER

ABSTRACT
DECTREX 1 IS A DECTAPE RANDOM EXERCISER FOR THE TC01 DECTAPE CONTROL AND ANY CONFIGURATION OF ONE TO EIGHT TU55 DECTAPE TRANSPORTS, DRIVE SELECTION, TAPE DIRECTION, NUMBER OF BLOCKS, SEQUENCE OF OPERATION AND PATTERNS GENERATED ARE BY RANDOM SELECTION. THE DECTAPE FUNCTIONS EXERCISED ARE SEARCH, READ DATA AND WRITE DATA IN NORMAL AND CONTINUOUS MODES, READ ALL IN CONTINUOUS MODE, AND MOVE.

ALSO INCLUDED ARE A SHORT SERIES OF PROCESSOR TESTS THAT ARE EXECUTED WHILE WAITING FOR INTERRUPTS AND DURING DATA BREAKS WHILE SEARCHING, READING, AND WRITING FROM DECTAPE.

REQUIREMENTS
PDP-8 (STANDARD)
TC01 DECTAPE CONTROL
ONE TO EIGHT TU55 DECTAPE TRANSPORTS
ONE STANDARD PDP-8 DECTAPE FOR EACH DRIVE (2702 8 129-WORD BLOCKS)

STORAGE - THE PROGRAM OCCUPIES MOST OF MEMORY FROM ADDRESS 0000 TO 5000.
IN ADDITION THE JMS TEST USES ADDRESSES 6000 TO 6200 FOR JMS STORAGE.

LOADING - BINARY LOADER

STARTING PROCEDURE
SWITCH REGISTER BITS 0 TO 7 ARE USED FOR DRIVE SELECTION.
LOAD DECTREX 1 INTO MEMORY.
DIAL THE DESIRED DRIVE NUMBER(S) ON EACH TU55 TO BE TESTED.
PUT EACH TU55 ON LINE, WRITE ENABLED WITH A STANDARD PDP-8 DECTAPE INSTALLED.
SET THE SWITCH REGISTER TO 0200.
PRESS LOAD ADDRESS.
SET THE SWITCH REGISTER TO SELECT DRIVES
PRESS START.
THE PROCESSOR HALTS AT ADDRESS 0207.
SET ALL SWITCH REGISTER BITS TO 0 OR AS DESIRED
PRESS CONTINUE.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES

SW0	UP	DELETE ERROR TYPEOUTS AND HALTS.
SW1	UP	DELETE ERROR HALTS.
SW2	UP	TYPE FIRST FOUR DATA COMPARE ERRORS IN EACH BLOCK.

SW2	DOWN	TYPE ALL DATA COMPARE ERRORS.
SW11	DOWN	ONLY HIT END ZONE ONCE FOR TURNAROUND FOR BLOCKS 0000 AND 2701
SW11	UP	HIT END ZONE TWICE BEFORE TURNAROUND FOR BLOCKS 0000 AND 2701

MAINDEC-08-D4BA-D

PDP-8, 8/I EXTENDED MEMORY PARITY TEST

ABSTRACT

THE PDP-8, 8/I EXTENDED MEMORY PARITY TEST IS DESIGNED TO PROVIDE WORST CASE HALF-SELECT NOISE CONDITIONS WITHIN THE PARITY BIT PLANE. FOUR DATA PATTERNS, AND THEIR COMPLEMENTS ARE WRITTEN, AND CHECKS FOR PARITY ERRORS AFTER WRITING EACH PATTERN ARE MADE. THE PROGRAM WILL TEST SYSTEMS EQUIPPED WITH FROM 8K TO 32K WORDS OF CORE MEMORY.

OPERATION OF THE PROGRAM IS SIMILAR TO THE PDP-8, 8/I, 8/S EXTENDED MEMORY CHECKERBOARD TEST EXCEPT THAT PROGRAM RELOCATION IS NOT INCLUDED, AND ERROR HALTS ARE PROVIDED FOR ERROR IDENTIFICATION.

REQUIREMENTS

A STANDARD PDP-8 OR 8/I EQUIPPED WITH AT LEAST 8K WORDS OF CORE MEMORY WITH PARITY.

STORAGE - THE PROGRAM OCCUPIES LOCATIONS 0020 TO 1565 OCTAL.

LOADING - BINARY LOADER

STARTING PROCEDURE

IMMEDIATELY AFTER STARTING FROM ADDRESS 200, THE PROGRAM WILL PRINT "TEST LIMITS". THE OPERATOR MUST THEN SPECIFY, VIA THE TELE-TYPE KEYBOARD, THE AMOUNT OF CORE MEMORY TO TEST, FOLLOWED BY A CARRIAGE RETURN.

TYPE TWO OCTAL NUMBERS, SEPARATING THE NUMBERS WITH A COMMA. THE FIRST NUMBER SIGNIFIES THE LOWEST ORDER 4K STACK TO TEST; THE SECOND SIGNIFIES THE HIGHEST ORDER.

IF A TYPING ERROR IS MADE PRESS THE RUB-OUT KEY.

SET THE SR TO 200; PRESS LOAD ADDRESS, AND THEN START.

THE MESSAGE "TEST LIMITS" WILL BE PRINTED. SPECIFY THE LIMITS VIA KEYBOARD

THE PROGRAM WILL RUN ALL TESTS ON ALL OF CORE MEMORY SPECIFIED UNTIL STOPPED BY THE OPERATOR.

PRINTOUTS - NO

SWITCH REGISTER OPTIONS - NO

MAINDEC-Ø8-D4CB-D

PDP-8/I, 8/L INCREMENTAL
TAPE COMPATIBILITY TEST

ABSTRACT

THE PDP-8/I, 8/L PEC INCREMENTAL TAPE COMPATIBILITY TEST HAS BEEN PROVIDED TO VERIFY THAT THE PEC INCREMENTAL WRITE ONLY AND INCREMENTAL WRITE-SYNCHRONOUS READ TRANSPORTS GENERATE IBM COMPATIBLE FORMAT. THIS IS ACCOMPLISHED BY GENERATING A TEST TAPE USING PATTERS #1 OF THE TC59 DATA RELIABILITY TEST. THE TC59 IS THE CONTROL UNIT FOR THE TU20 TRANSPORT WHICH IS IBM COMPATIBLE. THE TEST TAPE IS THEN READ BACK ON THE TU20 TRANSPORT USING THE APPROPRIATE TC59 DATA RELIABILITY TEST PROGRAM. FOR OPERATING PROCEDURES OF TC59 DATA RELIABILITY TEST (7 OR 9 TRACK) REFER TO MAINDEC-9A-D4DC-D OR MAINDEC-9A-D4EB-D.

REQUIREMENTS

FOR GENERATING TEST TAPE
- PDP-8/I OR 8/L
- TRØ2 MAGNETIC TAPE CONTROL
- PEC INCREMENTAL WRITE ONLY OR INCREMENTAL WRITE-SYNCHRONOUS READ MAGNETIC TAPE TRANSPORT.

FOR CHECKING TEST TAPE
- PDP-9
- TC59 MAGNETIC TAPE CONTROL
- TU20 MAGNETIC TAPE TRANSPORT

STORAGE - THE PROGRAM OCCUPIES CORE FROM 0000 TO 1300

LOADING - BINARY LOADER

STARTING PROCEDURE
- MOUNT TAPE ON TRANSPORT
- TENSION TAPE
- SET SR TO 200
- DEPRESS LOAD ADDRESS
- SELECT OPTIONS
- DEPRESS START TO WRITE, OR TO READ TEST TAPE
- A HALT AT EITHER 0411 OR 0617, THE TEST TAPE IS COMPLETE AND READY TO BE CHECKED ON THE TU20

PRINTOUTS - NO

SWITCH REGISTER OPTIONS - YES

BIT Ø
- CLEAR FOR ODD PARITY
- SET FOR EVEN PARITY

BIT 1
- CLEAR FOR TRANSPORT Ø
- SET FOR TRANSPORT 1

BIT 2
- CLEAR FOR SEVEN TRACK
- SET FOR NINE TRACK

BIT 11
- CLEAR FOR NORMAL OPERATION
- SET FOR READ ONLY

MAINDEC-08-D4DA-D

INCREMENTAL TAPE DATA
RELIABILITY TEST

ABSTRACT

THIS PROGRAM IS PRIMARILY DESIGNED FOR CHECKOUT OF THE PEC WRITE/READ INCREMENTAL TAPE UNITS INTERFACED WITH EITHER A PDP-8/I OR PDP-8/L. THE PROGRAM EXERCISES UP TO TWO TAPE UNITS WITH THREE SEPARATE PROGRAM ROUTINES WHICH ARE INDEPENDENT OF EACH OTHER. THE OPERATOR MUST SPECIFY THE TYPE OF TAPE UNIT AND THE DESIRED TEST ROUTINES VIA KEYBOARD INPUT. DATA ERRORS READ FROM TAPE ARE INDICATED BY PRINT-OUTS ON THE TTY.

THIS PROGRAM MAY ALSO BE USED AS AN EXTENDED DATA RELIABILITY ACCEPTANCE TEST.

REQUIREMENTS

A PDP-8/I OR 8/L; TR02 CONTROL AND A 7 AND/OR 9 TRACK, WRITE/READ, PEC INCREMENTAL TAPE TRANSPORT.

STORAGE - THE PROGRAM OCCUPIES APPROXIMATELY 4100 (OCTAL) LOCATIONS

LOADING - BINARY LOADER

STARTING PROCEDURE

TAPE MUST BE TENSIONED AND AT LOAD POINT.
SET THE SR TO 0200
PRESS LOAD ADDRESS AND THEN START.

THE OPERATOR MUST THEN SPECIFY THE DRIVE NUMBER, NUMBER OF TRACKS AND WHETHER EVEN OR ODD PARITY IS USED. THIS IS DONE VIA THE KEYBOARD AFTER THE HEADER SHOWN BELOW IS PRINTED.

```
DRIVE           TRACKS          PARITY
 0
```

THE PROGRAM PRINTS THE TAPE DRIVE NUMBER (0 OR 1), AFTER WHICH THE OPERATOR MUST DO THE FOLLOWING:

A. PRESS CARRIAGE RETURN IF THE TAPE DRIVE IS NOT TO BE TESTED.
B. TYPE A 7 OR 9 TO INDICATE THE NUMBER OF TRACKS.
C. INDICATE PARITY BY TYPING A 0 FOR EVEN, OR A 1 FOR ODD.

AFTER STEP C, A 1 WILL BE PRINTED UNDER DRIVE. REPEAT STEPS A THROUGH C FOR DRIVE UNIT 1.

AFTER SPECIFYING DRIVE 1 OPERATIONS, THE PROGRAM WILL PRINT:

```
TEST SELECTION
1
2
3
```

TYPE A 0 OR A 1 AFTER EACH TEST NUMBER IS PRINTED. A 0 INHIBITS A TEST, AND A 1 INDICATES THE TEST IS TO BE RUN.

ANY ONE OR ANY COMBINATION OF THE THREE TESTS MAY BE SELECTED.

AFTER SPECIFYING THE TESTS, THE PROGRAM WILL PRINT:

PATTERN SELECTION
0
1
2
3
4
5
6
7

TYPE A 0 OR A 1 AFTER EACH PATTERN NUMBER IS PRINTED. A 0 INHIBITS A PATTERN, AND A 1 INDICATES THE PATTERN IS TO BE RUN. ANY ONE, ANY COMBINATION, OR ALL OF THE PATTERNS MAY BE SELECTED.

IF ONLY TEST 1 IS TO BE RUN, THERE MUST STILL BE A PATTERN SELECTED EVEN THOUGH IT WILL NOT BE USED.

ANY EXTRANEOUS CHARACTER TYPED WILL RESULT IN THE CURRENT LINE BEING RESTARTED.

THERE MUST BE AT LEAST ONE SELECTION MADE IN EACH OF THE ABOVE; DRIVE, TEST, PATTERN. IF NOT THE SELECTION WILL BE REPEATED.

TESTING BEGINS IMMEDIATELY AFTER PATTERN SELECTION IS SPECIFIED.

PRINTOUTS = YES

SWITCH REGISTER OPTIONS = YES

SR0 ON A 1	= PRINT ACCUMULATED ERRORS ONLY, PRINTED AT COMPLETION OF TEST CYCLE.
SR0 ON A 0	= PRINT ERRORS AS THEY OCCUR.
SR1 ON A 1	= INHIBIT ALL PRINTOUT.
SR1 ON A 0	= RESUME PRINTOUT
SR11 ON A 1	= AT COMPLETION OF CURRENT OPERATION RETURN TO TEST SELECTION ROUTINE.
SR11 ON A 0	= RUN NORMAL TEST SEQUENCE, CYCLE TESTS AS SELECTED.

MAINDEC-08-D4EB-D (D)

PDP-8/I AND 8/L PEC INCREMENTAL
TAPE INSTRUCTION TEST

ABSTRACT

THE PEC INCREMENTAL TAPE INSTRUCTION TEST IS DESIGNED TO TEST ALL IOT INSTRUCTIONS ASSOCIATED WITH THE TR02A CONTROL. THE PROGRAM MAY BE USED ON W/O OR R/W TRANSPORTS, AND 7 AND 9 TRACK

TRANSPORTS AT ANY OF THE THREE STANDARD BIT DENSITIES. THE PROGRAM EXERCISES EACH IOT, BUT DOES NOT TEST VALIDITY OF THE LRCC OR CRC. THESE CHARACTERS ARE CHECKED IN THE DATA RELIABILITY DIAGNOSTIC.

THE PROGRAM INITIALLY TESTS AS MANY FUNCTIONS AS POSSIBLE WITHOUT A SUPPLY REEL MOUNTED. A SUPPLY REEL IS THEN MOUNTED, AND ALL REMAINING TAPE MOVEMENT IOT'S ARE CHECKED. INSTRUCTIONS WHICH THE OPERATOR MUST FOLLOW ARE PRINTED ON THE TTY.

ERRORS ENCOUNTERED ARE INDICATED BY PROGRAM HALTS.

REQUIREMENTS
A PDP-8/I OR 8/L EQUIPPED WITH A TR02A AND A W/O OR R/W PEC INCREMENTAL TAPE TRANSPORT.

STORAGE - THE PROGRAM REQUIRES THE FIRST 4000 OCTAL LOCATIONS OF MEMORY FIELD 0.

LOADING - BINARY LOADER

STARTING PROCEDURE
REMOVE THE TAPE SUPPLY REEL FROM THE TRANSPORT
SET THE SR TO 200
PRESS LOAD ADDRESS AND THEN START
ANSWER THE PRINTED QUESTIONS VIA KEYBOARD, TERMINATE EACH ANSWER BY PRESSING CARRIAGE RETURN, PRESS THE SPACE BAR TO REPEAT THE CURRENT QUESTION IF A TYPING ERROR IS MADE.

IF ALL PRELIMINARY TESTS RUN SUCCESSFULLY, THE PROGRAM WILL ISSUE A PRINT-OUT REQUESTING THAT A TAPE SUPPLY REEL BE MOUNTED. THE TAPE SHOULD HAVE AN EOT INDICATOR 10 OR 12 FEET PAST THE BOT INDICATOR. THIS IS FOR THE EOT TEST. THE EOT TEST MAY BE BYPASSED BY PLACING SR 1 ON A 1 BEFORE STARTING THE PROGRAM FROM 537, AFTER MOUNTING THE REEL.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES
SR 0 ON A 1 WILL INHIBIT THE 'END' TYPEOUT.
SR 1 ON A 1 WILL INHIBIT THE EOT TEST.

MAINDEC-08-D4FB-D(D)

PDP-8/I AND 8/L PEC INCREMENTAL
TAPE RANDOM EXERCISER.

ABSTRACT
THIS PROGRAM WAS WRITTEN FOR PEC WRITE/READ INCREMENTAL TAPE UNITS INTERFACED WITH EITHER A PDP-8/I OR PDP-8/L, AND EXERCISES UP TO TWO TAPE UNITS WITH THREE SEPARATE PROGRAM ROUTINES WHICH ARE DEPENDENT OF EACH OTHER. THE OPERATOR MUST SPECIFY THE TYPE OF TAPE UNIT AND THE DESIRED TEST ROUTINE VIA KEYBOARD INPUT. DATA ERRORS READ FROM TAPE ARE INDICATED BY PRINT-OUTS ON THE TTY.

REQUIREMENTS
A PDP-8/I OR 8/L; TR02 CONTROL AND A 7 OR 9 TRACK, WRITE/READ, PEC INCREMENTAL TAPE TRANSPORT.

STORAGE - THE PROGRAM OCCUPIES APPROXIMATELY 2600 (OCTAL) LOACTIONS OF MEMORY
FIELD 0.

LOADING - BINARY LOADER

STARTING PROCEDURE
SET THE SR TO THE DESIRED STARTING ADDRESS (0200 OR 0203)
TAPE MUST BE TENSIONED AND AT LOAD POINT,
PRESS LOAD ADDRESS AND THEN START.

THE OPERATOR MUST THEN SPECIFY THE DRIVE NUMBER, NUMBER OF TRACKS
AND WHETHER EVEN OR ODD PARITY IS USED. THIS IS DONE VIA THE
KEYBOARD AFTER THE HEADER SHOWN BELOW IS PRINTED.

DRIVE TRACKS PARITY
0

THE PROGRAM PRINTS THE TAPE DRIVE NUMBER (0 OR 1), AFTER WHICH
THE OPERATOR MUST DO THE FOLLOWING:

A. PRESS CARRIAGE RETURN IF THE TAPE UNIT IS NOT TO BE TESTED.
B. TYPE A 7 OR A 9 TO INDICATE THE NUMBER OF TRACKS.
C. INDICATE PARITY BY TYPING A 0 FOR EVEN, OR A 1 FOR ODD.
D. PRESS CARRIAGE RETURN. THE PROGRAM WILL INCLUDE THE DRIVE IN
ALL TESTS.

AFTER STEP D, A 1 WILL BE PRINTED UNDER DRIVE. REPEAT STEPS A
THROUGH D FOR DRIVE UNIT 1.

PRESS THE SPACE BAR IF A TYPING ERROR IS MADE. THE CURRENT LINE
WILL BE RESTARTED.

AFTER SPECIFYING DRIVE 1 OPERATIONS, THE PROGRAM WILL PRINT:

TEST SELECTION
1
2
3

TYPE A 0 OR A 1 AFTER EACH TEST NUMBER IS PRINTED. A 0 INHIBITS A TEST,
AND A 1 INDICATES THE TEST IS TO BE RUN. ANY ONE OR ANY COMBINATION
OF THE THREE TESTS MAY BE SELECTED. THE SELECTIONS WILL BE LOOPED
UNTIL RESTARTING THE PROGRAM FROM 200 OR 203. TESTING BEGINS
IMMEDIATELY AFTER TEST 3 IS SPECIFIED.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES
SR0 ON A 1 = INHIBIT ALL DATA ERROR PRINT OUTS DURING TESTS 2 OR 3.
SR0 ON A 0 = RESUMES ERROR REPORTING.
SR2 ON A 1 = SUPPRESS "END" TYPEOUT.

MAINDEC-08-D5AA-D

RM08 DRUM TEST AND MAINTENANCE COMPILER

ABSTRACT
THIS IS A TEST AND MAINTENANCE PROGRAM DESIGNED TO EXERCISE THE

TYPE RM08 DRUM. THE TEST ROUTINES GENERATED AND EXECUTED BY THE COMPILER ARE SPECIFIED BY A PSEUDO PROGRAM. THIS MAY BE KEPT AS AN INTEGRAL PART OF THE COMPILER BINARY PROGRAM TAPE, STORED ON A SEPARATE PAPER TAPE, OR TYPED ON-LINE FOR INVESTIGATION OF AN OBSERVED MALFUNCTION. THE SWITCH REGISTER ALLOWS TESTING OF VARIOUS SIZE DRUMS. ERRORS ARE INDICATED BY PRINTED MESSAGES, WHICH MAY BE SUPPRESSED IF DESIRED.

REQUIREMENTS
PDP-8, TYPE 33/35 TELETYPE, RM08 DRUM.

STORAGE - THE COMPILER OCCUPIES LOCATIONS 20 TO 1777

LOADING - BINARY LOADER

STARTING PROCEDURE
SET SWITCH REGISTER BITS 3 TO 11 TO INDICATE DRUM SIZE, IN TRACKS.

STARTING ADDRESSES

100 OR 200	THE CURRENT PSEUDO PROGRAM IF ANY, IS DESTROYED, AND THE COMPILER IS READY TO ACCEPT A NEW ONE VIA THE TELETYPE READER OR KEYBOARD.
600	EXECUTION OF THE CURRENT PSEUDO PROGRAM WILL BEGIN AT THE FIRST INSTRUCTION.

SET THE SWITCH REGISTER TO THE REQUIRED STARTING ADDRESS
PRESS THE LOAD ADDRESS SWITCH
PRESS THE START SWITCH
A PSEUDO PROGRAM MAY BE READ IN BY LOADING AND ACTIVATING THE TELETYPE READER.
IF THE OPERATOR CHOOSES, HE MAY INSTEAD TYPE IN HIS PSEUDO PROGRAM
THE NEWLY ENTERED PSEUDO PROGRAM WILL BE EXECUTED WHEN AN EXCLAMATION "!" IS INPUT FROM THE READER OR KEYBOARD.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES

BIT 0	1	THE COMPUTER HALTS ON COMPLETION OF EACH PSEUDO INSTRUCTION.
BIT 1	0	ERRORS ARE PRINTED AS SPECIFIED BY SR BIT 2.
	1	ERROR PRINTOUTS ARE SUPPRESSED.
BIT 2	0	DATA-CHECKING ERROR PRINTOUTS ARE LIMITED TO THE FIRST FOUR FOUND BY EACH CHECKING PSEUDO INSTRUCTION. IN THE CASE OF PSEUDO INSTRUCTIONS THAT EXERCISE THE WHOLE DRUM, THEY ARE LIMITED TO THE FIRST FOUR FOUND FOR EACH DRUM TRACK.
	1	NO LIMIT IS SET TO ERROR PRINTOUTS.
BITS 3 TO 11		BITS 3 TO 11 SPECIFY THE DRUM SIZE, IN TRACKS, WHEN EXERCISING THE WHOLE DRUM. FOR EXAMPLE, IF THE DRUM SIZE IS 65K WORDS (64 TRACKS), 100(8) SHOULD BE SET IN BITS 3 TO 11. THE PROGRAM ASSUMES A MINIMUM OF EITHER ONE OR TWO TRACKS.

MAINDEC-08-D5BC-D

DF32 DISCLESS
LOGIC TEST, MINIDISC

ABSTRACT
DISCLESS IS A TEST OF THE DF32 DISC LOGIC AND ITS COMPUTER INTERFACE. THIS PROGRAM DOES NOT TEST THE DISC, NOR ASSOCIATED ANALOG INTERFACE CIRCUITS.
(THE DISC IS NOT NEEDED FOR THESE ROUTINES; IF IT IS CONNECTED, THE DISC MOTOR SHOULD BE TURNED OFF. FOR A COMPLETE TEST OF THE DISC SYSTEM USE DF32 DISC DATA TEST.)

REQUIREMENTS
PDP-8 STANDARD
DF32 DISC LOGIC
LIGHT CARD (FOR TESTING TRACK SELECTOR)

STORAGE - THE PROGRAM USES MOST OF MEMORY FROM ADDRESS 100 TO 3400 AND LOCATIONS 0, 1 AND 2.

LOADING - BINARY LOADER

STARTING PROCEDURE
TURN DISC MOTOR OFF.
LOAD DISCLESS INTO MEMORY.
SELECT EM0 (DISC ZERO), (ALL OTHER UNITS TO OFF).
WRITE INHIBIT SWITCHES OFF.
CONNECT LIGHT CARD IF TRACKS ARE TO BE TESTED (NOT NECESSARY FOR TEST).
SET THE SWITCH REGISTER TO 100.
LOAD ADDRESS.
SET THE SWITCH REGISTER TO ALL ZERO (DOWN), UNLESS PDP-8E OR PDP-12
PRESS START.
PROGRAM WILL RUN; IF THE LIGHT CARD IS USED, LIGHTS WILL LIGHT FROM 0 TO 17(8) IN SEQUENCE AND THE PROGRAM WILL LOOP UPON COMPLETION.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES

SW0	UP	DELETE PRINT OUT
SW1	UP	HALT AFTER ERROR
SW2	UP	SUB TEST SCOPE LOOP
SW3	UP	DO NOT EXIT SECTION
SW4	UP	DELETE LIGHT BOX
SW11	UP	PDP-8/E OR PDP-12

MAINDEC-08-D5CG-D

DF32/DF32D DISK DATA
MINI DISK, INTERFACE
ADDRESS, DATA TEST

ABSTRACT
THE DF32/DF32D DISK DATA IS COMPLETE TEST OF THE DISK SYSTEM. ALSO INCLUDED IS A SHORT PROCESSOR TEST THAT

IS EXECUTED WHILE WAITING FOR INTERRUPTS, AND DURING
DATA BREAKS.

REQUIREMENTS
PDP-8, PDP-8/S, PDP-8/I, PDP-8/L OR PDP-8/E
IF PDP-8/S; DATA BREAK INTERFACE
DF32 OR DF32D DISK LOGIC
1 TO 4 DISKS

STORAGE - THE PROGRAM USES MOST OF MEMORY - 0000 THROUGH 7400

LOADING - BINARY LOADER

STARTING PROCEDURES
SELECT EMO (ALL OTHER UNITS TO OFF)
WRITE INHIBIT SWITCHES OFF
SET THE SWITCH REGISTER TO 100; (77 FOR THE PDP-8/S)
LOAD ADDRESS
SET THE SWITCH REGISTER TO ALL 0S (DOWN)
PRESS START
PROGRAM WILL RUN AND LOOOP UPON COMPLETION. THE ONLY
PRINTOUT THAT SHOULD OCCUR ARE "RPMXXXX SYNC TIME =
XXXX MICRO SECS" AND "PCXX"

SPECIAL ENTRANCE ADDRESS
101 ADDRESS TEST (SLOW)
102 TRACK DECODE TEST
103 TRACK ERROR RATIO TEST
104 DATA BREAK TEST
105 DATA TEST.
106 READ RECOVERY TIME TEST. (NOT USED ON PDP-8/S)
107 DISK WRTIE CURRENT SATURATION TEST.
110 RANDOM; DISK, TRACK, ADDRESS AND DATA TEST;

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES
SW0 UP DELETE PRINTOUTS
SW1 UP HALT AFTER ERROR.
SW2 UP SUBTEST SCOPE LOOP.
SW3 UP DO NOT EXIT SECTION.
SW11 UP TRACE (TYPE STARTING ADDRESS OF EACH TEST
AS THE PROGRAM ENTERS IT)

MAINDEC-08-D5DB
DF32 MULTI DISK

ABSTRACT
MULTI DISK IS A HIGH SPEED CONFIDENCE TEST THAT EXERCISES THE DISK SYSTEM WITH RANDOM
DATA AND RESTORES THE DISK SURFACE TO ITS ORIGIONAL STATE AT COMPLETION.

REQUIREMENTS
PDP8 OR PDP8/I
DF32 DISK LOGIC
PLUS ADDITIONAL SLAVE DISKS UP TO THREE

STORAGE - PROGRAM OCCUPIES AND USES MEMORY FROM 0 TO 7500;

LOADING - BINARY LOADER

EXECUTION TIME - 15 SECONDS PER DISK.

STARTING PROCEDURES
        ENSURE WRITE INHIBIT SWITCHES ARE OFF
        LOAD ADDRESS 0200
        CLEAR SWITCH REGISTER
        PRESS START

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES

MAINDEC-08-D5EB-D

RF08 DISK DATA (256K)

ABSTRACT
        RF08 DISK DATA WHEN USED IN ITS ENTIRETY IS A COMPLETE CHECK OF THE DISK SURFACE AND CONTROL LOGIC. DISK DATA CONSISTS OF THREE BASIC SECTIONS. THE FIRST IS THE STATIC TEST WHICH IS A CONTINUATION OF DISKLESS, WHICH TESTS THE INTERFACE LOGIC. THE SECOND SECTION IS A COMBINATION OF SEVERAL ADDRESS TESTS. THESE TESTS VERIFY THAT ALL ADDRESSES CAN BE ACCESSED AND THAT ALL TRACKS CAN BE SELECTED. THE THIRD SECTION OF THE TEST, EXERCISES THE DISK'S ABILITY TO TRANSFER DATA CORRECTLY. IN THE DATA TESTS ALL READS ARE ACCOMPLISHED FOUR TIMES FOR EACH DISK BUFFER. BY DOING THIS THE OPERATOR CAN DEFINE THE ERROR AS EITHER A WRITE OR READ ERROR.

REQUIREMENTS
        PDP-8 OR PDP-8/I
        RF08 AND RS08

STORAGE - ALL OF BANK ZERO

LOADING - BINARY LOADER

EXECUTION TIME - 40 MINUTES

STARTING PROCEDURE
        SET SWITCH REGISTER EQUAL TO 0200
        DEPRESS LOAD ADDRESS
        RESET SWITCH REGISTER TO MODE OF OPERATION
        (WORSE CASE SR EQUALS 0)
        DEPRESS START

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES

MAINDEC-08-D5FA

RF08 MULTI DISK 11 (256K)

ABSTRACT
"MULTI DISK 11" IS A HIGH SPEED CONFIDENCE TEST THAT EXERCISES THE DISK SYSTEM WITH RANDOM DATA AND RESTORES THE DISK SURFACE TO ITS ORIGINAL STATE AT COMPLETION.

REQUIREMENTS
PDP-8 OR PDP-8/I
RF08 AND RS08
PLUS ADDITIONAL SLAVE DISKS UP TO THREE

STORAGE - THE MAIN BODY OF THE PROGRAM IS LOCATED BETWEEN LOC.0 AND 1250 IN MEMORY.
THREE BUFFERS OF 2000 WORDS EACH TAKE UP THE REST OF MEMORY UP TO 7500

LOADING - BINARY LOADER

STARTING PROCEDURE
TURN WRITE INHIBIT SWITCHES TO OFF
LOAD ADDRESS 150
SWT SWITCH REGISTER TO MODE OF OPERATION DESIRED
PRESS START
THE PROGRAM WILL CONTINUE TO LOOP UPON COMPLETION OF THE SYSTEM BEING EXERCISED.
END OF TEST COMMAND. WHEN THE END OF TEST COMMAND (CONTROL C) IS GIVEN IN THE NORMAL MODE OF OPERATION THE TEST COMES TO A HALT AT THE COMPLETION OF THE 2000 WORK BUFFER BEING EXERCISED AT THAT TIME.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES

MAINDEC-08-D5HC-D

RK8 DISK DATA RELIABILITY TEST

ABSTRACT
THE RK8 DISK DATA RELIABILITY TEST (RK8DD) IS PRIMARILY DESIGNED FOR THE COLLECTION OF STATISTICAL INFORMATION PERTAINING TO THE DATA RELIABILITY OF THE DISK DRIVES THAT MAY BE ASSOCIATED WITH THE RK8 DISK CONTROL.

TO DO THIS MOST EFFICIENTLY, THIS PROGRAM HAS BEEN DESIGNED AS AN EXTENDED DATA RELIABILITY ACCEPTANCE TEST. FOR THIS REASON RK8DD CONSISTS OF AN "ACCEPT" (ACCEPTANCE) MODE (REFER TO PARAGRAPH 4,2,1,1,).

THIS PROGRAM IS ALSO DESIGNED TO BE USED AS AN AID TO HARDWARE DEBUGGING AND MAINTENANCE OF THE RK8 DISK CONTROL AND ITS ASSOCIATED DISK DRIVES. FOR THIS REASON RK8DD CONSISTS OF A "TEST" (MANUAL INTERVENTION) MODE (REFER TO PARAGRAPH 4,2,1,2).

TO FURTHER INCREASE MANUAL INTERVENTION AND TO FULLY OPTOMIZE ALL ASPECTS OF THIS PROGRAM, SEVERAL SUBMODES HAVE BEEN DEVELOPED.

REQUIREMENTS
PDP-8,8/E,8/I,8/L, OR LINC-8 (STANDARD)
RK8 DISK CONTROL
RK01 DISK DRIVE(S), MAXIMUM OF 4
RK01-K DISK CARTRIDGES (1 OR EACH RK01)

STORAGE - THIS PROGRAM OCCUPIES ALL OF 4K.

LOADING - BINARY LOADER

STARTING PROCEDURE
SET AC SWITCHES TO 200 OR
SET AC SWITCHES TO 201 (FOR IOT "DCLA")
PRESS LOAD ADDRESS
PRESS START

THE PROGRAM WILL PRINT ($) AFTER BEING INITIALIZED AND WAIT
FOR THE OPERATOR TO TYPE ANY ONE OF THE LEGAL INPUT WORDS.
(ANY KEY TYPED BY THE OPERATOR WHICH DOES NOT SPELL ANY OF THE
LEGAL INPUT WORDS PRIOR TO THE CARRIAGE RETURN WILL CAUSE THE
PROGRAM TO PRINT (?) AND WAIT FOR ANOTHER SELECTION.

THE LEGAL INPUT WORDS ARE:
ACCEPT
TEST
SELPAT
SELWC
SELTSS
SELDRV
RETEST
DUMP
CONT
DELPAT
DELWC
DELTSS

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES

MAINDEC-08-D5JB-D

RK8 DISK AND CONTROL INSTRUCTION TEST

ABSTRACT
THE RK8 DISK AND CONTROL INSTRUCTION TEST IS A SERIES OF
INCREMENTAL AS WELL AS NON INCREMENTAL MANUAL INTERVENTION ROUTINES
AND TESTS DESIGNED TO AID IN THE CHECKOUT AND MAINTENANCE
OF THE RK8 DISK SYSTEM.

REQUIREMENTS
PDP-8,8/E,8/I,8/L, OR LINC-8
RK8 DISK CONTROL
RK01 DISK DRIVE
2315 IBM CARTRIDGE OR EQUIVALENT

LOADING - BINARY LOADER

```
STARTING PROCEEDURE
        LOAD ADDRESS 200
        SET AC SWITCHES 6-7-8 FOR EMA SELECTION
        PRESS START

        THE PROGRAM WILL HALT AT ADDRESS 205.

        4.  SET AC SWITCHES 6-7-8-9-10-11 FOR TEST (10-36)
        5.  PRESS CONTINUE

        THE PROGRAM WILL BEGIN EXECUTION OF THE TEST AVAILABLE BEGINNING WITH
        THE TEST SELECTED IN STEP #4.

PRINTOUTS = YES

SWITCH REGISTER OPTIONS = YES
        AC 0 = 0          HALT ON ERROR
        AC 1 = 0          PRINT ERROR MESSAGE HEADER
        AC 2 = 0          PRINT ERROR MESSAGE DATA
        AC 3 = 1          ABORT SCOPE LOOP
        AC 4 = 0          POWER CLEAR IN SCOPE LOOP (SUBROUTINE "PDCLA")
        AC 5 = 0          RING BELL ON ERROR
        AC 6 = 1          SUBTEST SELECTION IS MANUAL INTERVENTION
                          (SENSED AT START ONLY)
        AC 6 = 1          LOOP ON TEST SELECTED IN AC 7-8-9-10-11
                          (SENSED AT RUNTIME)
        AC 7-8-9-10-11    TEST SELECTIONS
        AC 8-9            DRIVE SELECTION (SENSED ONLY IN TEST # 41)
```

MAINDEC-08-D5KB

RK08 DISK FORMATTER

ABSTRACT
THE RK08 DISK FORMATTER WAS GENERATED FOR THE PURPOSE OF WRITING THE SECTOR ADDRESSES ON THE DISK, AND A SET DATA PATTERN IN THE DATA AREA. THE PROGRAM NORMALLY WRITES THE STANDARD DEC SURFACE FORMAT (REF. SEC. 5.2), BUT THE OPERATOR AT INITIALIZATION TIME MAY SET UP A NON-STANDARD SURFACE FORMAT. (REF. SEC. 5.2).

EQUIPMENT
PDP-8, 8/L, 8/I/12
RK08 DISK CONTROL AND DRIVE
RK01 DISK CARTRIDGE

STORAGE - 0 TO 4000 OF BANK ZERO

LOADING - BINARY LOADER.

PDP-8 8L/8I STARTING PROCEDURE
SET SWITCH REGISTER EQUAL TO 200.
DEPRESS LOAD ADDRESS.
SET SWITCH REGISTER 0 TO DELETE DISK CARTRIDGE MOUNTING PROCEDURE.
SET SWITCH REGISTER TO 10-11 EQUAL TO DRIVE NUMBER.
DEPRESS START.

PDP-12 STARTING PROCEDURE
DEPRESS I/O PRESET
SET TO 8 MODE
SET LEFT SWITCH REGISTER EQUAL TO 200.
SET RIGHT SWITCH REGISTER 0 TO DELETE DISK CARTRIDGE MOUNTING PROCEDURE.
SET RIGHT SWITCH REGISTER 10-11 EQUAL TO DRIVE NUMBER
DEPRESS L/S (LOAD START)

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - NO

MAINDEC 08-D6CC-D (D)

PDP-8 CALCOMP PLOTTER
DIAGNOSTIC

ABSTRACT
THE PDP-8 CALCOMP PLOTTER DIAGNOSTIC MAY BE RUN USING THE PDP-8, 8/I OR 8/L COMPUTERS. IT MAY BE USED TO TEST THE 12 INCH 10 MIL, THE 12 INCH 5 MIL, THE 31 INCH 10 MIL, OR THE 31 INCH 5 MIL PLOTTER. SEE PARA. 9 FOR PROGRAM DESCRIPTION.
NOTE: THE PROGRAM MUST BE RELOADED EACH TIME THE SIZE OR STEPPING RATE OF THE PLOTTER BEING TESTED IS CHANGED.

REQUIREMENTS
EQUIPMENT
PDP-8 OR PDP-8/I OR PDP-8/L
CALCOMP PLOTTER TYPE 350

LOADING - BINARY LOADER

STARTING PROCEDURE
SET SWITCH REGISTER TO 200
DEPRESS LOAD ADDRESS
SET SWITCH REGISTER
DEPRESS START
MONITOR COMPUTER FOR ERROR HALTS

PRINTOUTS - NO

SWITCH REGISTER OPTIONS - YES
BIT 0
SET TO HALT PROGRAM AFTER NEXT STEP WHEN DRAWING PATTERNS, (MA=3033)
PRESS CONTINUE TO GO ON.
BIT 1
SET TO RETRACE OCTAGONS OR CONCENTRIC SQUARES
BIT 2
SET TO LOOP TIMING TESTS
BIT 3
SET IF 31 INCH PLOTTER
BIT 5
SET IF 5 MIL PLOTTER
BIT 11
SET FOR PDP-8/L

MAINDEC-08-D6GC-D

A/D CALIBRATION CHECK

ABSTRACT
THE A/D CALIBRATION CHECK FOR THE CONVERTERS IS TO BE USED TO ASCERTAIN
THE ACCURACY OF CONVERTER ADJUSTMENTS. THIS TAPE IS TO BE USED
WITH AN ADJUSTABLE VOLTAGE SOURCE. THE CONVERTED VALUE
WILL BE DISPLAYED IN THE AC, AND THE SWITCH REGISTER WILL BE USED
TO SELECT MULTIPLEXER CHANNELS. (PASSING OF THESE CHECKS DO NOT
GUARANTEE 100% MONOTONICITY, STEADY STATE ACCURACY, SINCE ALL OF
THE 4096 POSSIBLE CONTITIONS ARE NOT CHECKED.)

REQUIREMENTS
PDP-8, PDP-8/I OR 8/S STANDARD COMPUTER
A/D CONVERTER
ADJUSTABLE VOLTAGE SOURCE (0.01% OR BETTER, Z OUT <1.0)

STORAGE - THE ROUTINE USES MEMORY FROM ADDRESS 100 TO 650 AND LOCATION 0 AND 1,

LOADING - BINARY LOADER

STARTING PROCEDURE
FOR NORMAL OPERATION ALL SWITCHES SHOULD BE DOWN.
STARTING ADDRESS IS:
100 FOR AF01A
102 FOR ADC1
CONNECT VOLTAGE SOURCE TO INPUT CONNECTOR.
LOAD THE PROGRAM INTO MEMORY.
SET SWITCH REGISTER TO STARTING ADDRESS.
LOAD ADDRESS.
SELECT MULTIPLEXER CHANNEL USING SWITCH REGISTER 6 TO 11=1 (AF01 ONLY)
PRESS START.
SET THE VOLTAGE SOURCE TO THE VOLTAGE DESIRED, INSPECT THE AC
FOR THE CORRECT CONVERTED VALUE.
FOR STARTING ADDRESS 102 SR=CONVERSION DISPLAY TIME
SA 103 ROUTINE FOR SETTING MULTIPLEXER SR=CHANNEL
SA 104 ROUTINE FOR INCREMENTING MULTIPLEXER SR=CHANNEL EXCEPT FOR OVERFLOW
WHICH SHOULD=ZERO

PRINTOUTS - NO

SWITCH REGISTER OPTIONS - NO

MAINDEC-08-D6HA-D

AF04A DIAGNOSTIC & DEMONSTRATION

ABSTRACT
THE DIAGNOSTIC & DEMONSTRATION PROGRAM FOR THE AF04A ALLOWS
THE OPERATOR TO TYPE IN UP TO 1000 8 PSEUDO INSTRUCTIONS AND CAUSE
ANALOG TO DIGITAL CONVERSIONS VIA THE AF04A. THE PSEUDO - INSTURC-
TIONS WHICH MAKE UP THE INDIVIDUAL PSEUDO - PROGRAM WILL BE
EXECUTED WHEN A "$" (DOLLAR SIGN) IS INPUTED FROM THE KEYBOARD.
THE OPERATOR MAY SPECIFY ALL PARAMETERS OF THE CONVERSION INSTRUCTION
AND SPECIFY ANY ORDER OF INSTRUCTIONS.

REQUIREMENTS
TO RUN THIS PROGRAM THE OPERATOR NEEDS A PDP-8, AN AF04A, AND
A MODEL 33 TELETYPE.

STORAGE - THE PROGRAM OCCUPIES LOCATION 0000 8 TO 2177 8.

LOADING - BINARY LOADER.

STARTING PROCEDURE
AFTER THE PROGRAM HAS BEEN READ IN VIA THE BINARY LOADER THE OPERATOR
SHOULD PLACE 0200 8 IN THE SWITCHES AND PRESS LOAD ADDRESS
AND START.
THE PROGRAM WILL ANSWER WITH A CARRIAGE RETURN, LINE FEED
SIGNALING IT IS READY FOR INSTRUCTIONS VIA THE TELETYPE.

5. OPERATING PROCEDURE

THE OPERATOR SHOULD TYPE HIS COMMANDS IN THE FORM OF A PSEUDO - PORGRAM. THERE ARE 4 POSSIBLE FORMS OF INSTRUCTIONS IN THE PSEUDO - PORGRAM INSTRUCTION SET. THE FIRST INSTRUCTION IS A REQULAR 2 BYTE CONVERSION; THE SECOND IS AN INDEX INSTRUCTION; AND THE THIRD IS A REREAD OR SELECT SAME CHANNEL INSTRUCTION AND THE FOURTH IS AN ON-LINE MONITOR INSTRUCTION.

INSTRUCTION TYPE 1

THE FIRST TYPE OF INSTRUCTION IS DESIGNED TO ALLOW THE OPERATOR TO PERFORM A SINGLE CONVERSION ON A SINGLE CHANNEL.
TO ENTER THE FIRST TYPE OF INSTRUCTION THE OPERATOR MUST TYPE 4 VARIABLES. THE FIRST VARIABLE HE TYPES IS A THREE CHARACTER WORD WHICH MAKES UP THE SEVEN OPTION BITS IN CONVERSION BYTE 1. THIS FIRST VARIABLE SHOULD BE TYPED IN OCTAL. THE SECOND VARIABLE IS ON OCTAL CHARACTER INDICATION THE RANGE OF THE CONVERSION. THE THIRD OCTAL VARIABLE IS THE INTEGRATION PERIOD TO BE USED.
A TABLE OF ALLOWABLE RANGE AND INTEGRATION PREIOD CHARACTERS IS GIVEN BELOW.
THE PROGRAM SEPARATES EACH VARIABLE WITHA A SPACE AND AFTER THE THIRD VARIABLE A CARRIAGE RETURN, LINE FEED IS OUTPUTED AND THE PROGRAM IS WAITING FOR THE FOURTH AND LAST VARIABLE OF INSTRUCTION 1. THE FOURTH VARIABLE IS IN BCD FORMAT (8,4,2,1) AND SPECIFIES THE CHANNEL NUMBER TO BE SAMPLED.
FOR EXAMPLE, TO DO A DC CONVERSION WITH A RANGE OF 4 (WHICH IS 10 VOLTS) AND A RESOLUTION OF 3 ON CHANNEL 9 THE OPERATOR SHOULD TYPE:

```
200     4       3
009
```

FOR A FURTHER EXPLANATION OF RANGE, INTEGRATION TIME, AND OPTION BITS, SEE SECTION 5.2.
AFTER THE LAST VARIABLE IS ENTERED THE PROGRAM WILL OUTPUT A CARRIAGE RETURN AND TO LINE FEEDS AND AWAIT THE NEXT COMMAND

ALLOWABLE RANGE AND INTEGRATION PERIODS

CHARACTER TYPED	RANGE SELECTED	INTEGRATION PERIOD SELECTED
1	10 MVOLTS	.1% (1.67 MSEC)
2	100 MVOLTS	.01% (16.7 MSEC)
3	1000 MVOLTS	.001% (166.7 MSEC)
4	10V/10K	NOT ALLOWABLE
5	100V/100K	NOT ALLOWABLE
6	1000V	NOT ALLOWABLE
7	AUTO RANGE	NOT ALLOWABLE

PRINTOUTS = NO

SWITCH REGISTER OPTIONS = NO

MAINDEC-08-D6JD-D

AD08 DIAGNOSTIC

ABSTRACT
FOR THE AD08A THIS IS AN I/O INSTRUCTION AND CALIBRATION CHECK, FOR THE AD08B IT IS ALSO A LIMITED TEST OF MULTIPLEXER SELECTION AND A/D REPEATABILITY.

REQUIREMENTS
PDP-8 OR 8/I STANDARD COMPUTER
AD08A OR AD08B
ADJUSTABLE VOLTAGE G714 SOURCE (.01% OR BETTER, Z OUT <1.0 OHM),
VOLTAGE MATRIX (OPTIONAL = G714 MATRIX ALLOWS ONE TO APPLY A UNIQUE VOLTAGE TO EACH CHANNEL OF THE AD08B WHEN USED WITH AN EXTERNAL SOURCE).

STORAGE = THE ROUTINE USES MEMORY FROM 0000 TO 2000.

LOADING = BINARY LOADER

STARTING PROCEDURE
IF THE A/D IS AN AD08B, A UNIQUE VOLTAGE SHOULD BE APPLIED TO CHANNEL ZERO BY USING THE OPTIONAL VOLTAGE MATRIX, G714, WITH THE EXTERNAL SOURCE, OR BY APPLYING THE EXTERNAL SOURCE TO CHANNEL ZERO AND GROUNDING ALL OTHER INPUTS.
LOADING THE PROGRAM INTO MEMORY.

SET SWITCH REGISTER TO STARTING ADDRESS.
LOAD ADDRESS.
PRESS START.
THE PROGRAM WILL STAY IN TEST AND LOOP.

STARTING ADDRESS OR ADDRESSES

200=NORMAL STARTING FOR AD08A
201=NORMAL STARTING FOR AD08B
202=DISPLAYS CONVERTED VALUE IN AC (FOR CHECKING CALIBRATION)
203=IOT SCOPE LOOP 65XX, XX EQUAL SR 6-11
204=SWITCH REGISTER CONTROLS CONVERSION RATE
205=SWITCH REGISTER BIT 8-11 EQUAL MULTIPLEXER CHANNEL

PRINTOUTS = NO

SWITCH REGISTER OPTIONS = YES

SW0=1 OR UP	HALT ON ERROR
SW1=1 OR UP	SCOPE LOOP
SW2=1 OR UP	INHIBIT PRINTOUT
SW3=1 OR UP	FOR MULTIPLEXER TEST ALLOW + 1 LSB

MAINDEC-08-D6KC-D

DISPLAY TEST 34D / VC8/I

ABSTRACT

THIS DIAGNOSTIC IS DESIGNED TO CHECK OUT ALL CONFIGURATIONS OF THE 34D-VC8/I DISPLAY, INCLUDING ALL IOT'S, DEFLECTION CIRCUITRY, INTENSITY LOGIC AND LIGHT PEN IF INCLUDED. UNDER NORMAL CONDITIONS WITHOUT A LIGHT PEN THE PICTURE WHICH IS DISPLAYED IS CONTROLLED BY SR00, SR01 AND SR02, WHICH ALLOW ONE OF EIGHT PICTURES TO BE DISPLAYED. THE INTENSITY OF THE DISPLAY IS CONTROLLED BY SR10, SR11. IF A LIGHT PEN IS CONNECTED AND SR03 IS SET, THE PICTURE WILL NOT CHANGE UNLESS A LIGHT PEN HIT IS MADE (I.E., THE LIGHT PEN IRIS IS OPEN, THE GAIN IS PROPERLY SET AND THE LIGHT PEN IS POINTED TOWARD ANY SORUCE OF LIGHT, TO WHICH LIGHT PENS ARE NORMALLY SENSITIVE.)

REQUIREMENTS

BASIC CONFIGURATION PDP-5, 8, 8/S, 8/I, 8/L, 8/E, 12 OR LINC-8.
A 34D OR VC8/I DISPLAY
A 370 LIGHT PEN (IF AVAILABLE)

LOADING - BINARY LOADER

STARTING PROCEDURE

HORIZONTAL

A. SET HORIZONTAL DISPLAY TO HORIZ AMP. ONLY.
B. SET HORIZONTAL TO 1 VOLTS/CM.
C. SET THE RED "VARIABLE" KNOB TO THE "CALIBRATED" MAXIMUM CLOCKWISE POSITION UNTIL IT CLICKS.
D. SET THE +INPUT SLIDE SWITCH TO DC.
E. SET THE -INPUT SLIDE SWITCH TO GND (AMP).

VERTICAL

F. SET VERTICAL TO 1 VOLTS/CM.
G. SET THE RED "VARIABLE" KNOB TO THE "CALIBRATED" MAXIMUM CLOCKWISE POSITION UNTIL IT CLICKS.
H. SET THE +INPUT SLIDE SWITCH TO DC.
I. SET THE -INPUT SLIDE SWITCH TO DC.

INTENSITY

J. ON THE REAR OF THE OSCILLOSCOPE THERE IS A BANANA PLUG, LABELED EXTERNAL INPUT ASCERTAIN THAT THE SHIELDED TERMINAL OF THE INPUT IS CONNECTED TO THE GROUND INPUT OF THE TERMINAL AND THE SIGNAL INPUT IS CONNECTED TO THE C.R.T. GRID INPUT.
K. TURN ON THE RM503 OSCILLISCOPE AND ALLOW IT TO WARM UP FOR SEVERAL MINUTES.

LIGHT PEN (IF AVAILABLE)

L. EXAMINE LIGHT PEN IRIS-TEST IRIS BUTTON TO ASCERTAIN THAT IT OPENS AND CLOSES THE IRIS.
M. SET LIGHT PEN GAIN CONTROL KNOB TO MID POSITION.
N. IF NO LIGHT PEN IS INSTALLED BE SURE THAT A JUMPER WIRE IS INSTALLED TO KEEP THE LIGHT PEN FLAG IN THE 0 CONDITION.

```
        SET THE COMPUTER SWITCH REGISTER TO 0200(8)
        DEPRESS LOAD ADDRESS
        SET SWITCH REGISTER TO 0000.
        DEPRESS START.
        THE DISPLAY TEST IS RUNNING AND A DIAGONAL LINE SHOULD BE
        VISIBLE DRAWN FROM THE UPPER LEFT CORNER TO THE LOWER
        RIGHT CORNER.

PRINTOUTS = NO

SWITCH REGISTER OPTIONS = YES
        SR=000          RUN TESTS 0 TO
           111          TEST 7.



MAINDEC-08-D6QA-D-D

LOW LEVEL MULTIPLEXER DIAGNOSTIC
        (AM03/AM08)

ABSTRACT
        THIS UNIT IS TESTED IN TWO SECTIONS,
        A.  AN IOT INSTRUCTION AND LOGIC TEST
        B.  A TEST OF THE MULTIPLEXER SELECTION, IN GROUPS OF 64 CHANNELS AT A TIME.

REQUIREMENTS
        PDP-8 OR 8/I STANDARD COMPUTER
        AM03 MULTIPLEXER
        AM08 MULTIPLEXER CONTROL
        A/D CONVERTER
        VOLTAGE MATRIX (OPTIONAL)

STORAGE = THE ROUTINE USES MEMORY FROM 0000 TO 3000.

LOADING = BINARY LOADER

STARTING PROCEDURE
        STARTING ADDRESS OR ADDRESSES
        177=INSTRUCTION AND SYSTEM TEST (10 BIT CONVERTER)
        200=INSTRUCTION AND SYSTEM TEST (12 BIT CONVERTER)
        201=AUTOMATIC MULTIPLEXER SELECTION
        202=CA REGISTER SCOPE LOOP SR=DATA
        203=INDEX CA REGISTER SCOPE LOOP SR=DATA
        204=FA REGISTER SCOPE LOOP SR=DATA
        205=MULTIPLEXER SELECTION SCOPE LOOP, SR=CHANNEL, AC=CONVERTED VALUE
        206=IOTS SCOPE LOOP 65XX,XX EQUALS SR 6 TO 11

        CONNECT VOLTAGES TO CHANNEL UNDER TEST,
        SET SWITCH REGISTER TO STARTING ADDRESS,
        LOAD ADDRESS,
        PRESS START,
        THE PROGRAM WILL STAY IN SECTION 1 AND LOOP.  (IF SR 6-11 = ZERO)
        TTY BELL WILL RING ONCE PER LOOP WHILE IN SECTION 1,
        OTHERWISE IT WILL ENTER SECTION 2.
```

PRINTOUTS = NO

SWITCH REGISTER OPTIONS = YES

SW0=1 OR UP	HALT ON ERROR.
SW1=1 OR UP	SCOPE LOOP.
SW2=1 OR UP	INHIBIT PRINTOUT
SW3=1 OR UP	TEST SYSTEM FOR SWITCHING POINTS
SW6 TO 11=1 OR UP	EXIT SECTION ONE AND ENTER SECTION TWO.

MAINDEC-08-D6RB-DL

AF04 DIAGNOSTIC TEST

ABSTRACT

THESE ROUTINES ARE DESIGNED TO BE AN INCREMENTAL TEST OF THE INTERFACE LOGIC BETWEEN THE COMPUTER AND THE VIDAR IDVM. ALL MANUAL CHECKS SHOULD BE COMPLETED BEFORE USING THIS MAINDEC. FOR A VOLTAGE ACCURACY TEST USE MAINDEC 08-D6H.

REQUIREMENTS

PDP-8 OR 8/I STANDARD COMPUTER
AF04A

STORAGE = THE ROUTINE USES MEMORY FROM 0000 TO 3200

LOADING = BINARY LOADER

STARTING PROCEDURE

RESET THE VIDAR UNIT
SET ALL SWITCHES TO PROGRAM OR P.I. WITH THE EXCEPTION OF THE "IDVM CHECK WHICH SHOULD BE SET TO "+1 VOLT".
THE "DELAY" SHOULD BE C.C.W.
LOAD AND PROGRAM INTO MEMORY.
SET SWITCH REGISTER TO STARTING ADDRESS. 0200.
LOAD ADDRESS.
PRESS START.
THE PROGRAM WILL STAY IN SECTION AND LOOP.

PRINTOUTS = YES

SWITCH REGISTER OPTIONS = YES

SW0 = 1 OR UP ... HALT ON ERROR
SW1 = 1 OR UP ... SCOPE LOOP
SW2 = 1 OR UP ... INHIBIT PRINTOUT

MAINDEC 08 D6TA-D

AA05/AA07 CALIBRATION TAPE

ABSTRACT
THESE ROUTINES ARE TO BE USED FOR THE CALIBRATION OF
THE AA05 DIGITAL TO ANALOG CONVERTER AND THE AA07 EXPANDER UNIT.

REQUIREMENTS
PDP8, 8/I, 8/L, OR 8/S STANDARD COMPUTER
AA05 DIGITAL TO ANALOG CONVERTER
AA07 EXPANDER UNITS.

STORAGE = THE PROGRAM USES MEMORY FROM ADDRESS 0 TO 400

LOADING = BINARY LOADER

STARTING PROCEDURE
STARTING ADDRESS OR ADDRESSES
200 = NORMAL CALIBRATION STARTING ADDRESS
SPECIAL ADDRESS
201 RAMP SCOPE LOOP
202 SQUARE WAVE SCOPE LOOP
203 IOT SCOPE LOOP

SET SWITCH REGISTER TO 200
LOAD ADDRESS
CLEAR SWITCH REGISTER
PRESS START
THE START KEY SHOULD HAVE CLEARED THE CHANNEL SELECTOR
REGISTER (LIGHTS ON FRONT PANEL).
THE SWITCH REGISTER, BITS 0 TO 9, CONTAINS THE DIGITAL
VALUE SET INTO THE DAC; CHANNEL ZERO IS SELECTED. IF A NEW
CHANNEL IS DESIRED, PLACE SWITCH REGISTER BIT 11 TO A "ONE"
OR UP, WHEN SR 11 EQUALS A ONE, BITS 0 TO 5 OF THE SR SELECT
THE DIGITAL TO ANALOG CHANNEL.

PRINTOUTS = NO

SWITCH REGISTER OPTIONS = NO

MAINDEC-08-D6UB-D

AD01-A DIAGNOSTIC

ABSTRACT
FOR THE AD01-A, THIS IS A I/O INSTRUCTION TEST AND A LIMITED
TEST OF CALIBRATION AND REPEATABILITY

REQUIREMENTS
PDP-8/I AD01-A STANDARD COMPUTER
G735 TEST CARD (OPTIONAL)
APPLY .625 VDC TO CHANNEL 0
OF THE MULTIPLEXER

STORAGE = THE ROUTINE USES MEMORY FROM 0000 TO 3000.

```
LOADING = BINARY LOADER

STARTING PROCEDURE
        STARTING ADDRESS OR ADDRESSES
        200 = NORMAL STARTING ADDRESS
              AT 1ST HALT-LOAD INITIAL CHANNEL TO BE TESTED,
              AT 2ND HALT-LOAD LAST CHANNEL TO BE TESTED,
              AND GAIN TO BE USED FOR WAS-IS TEST,
              SET SR TO 0YXX, WHERE Y=0,1,2,3 FOR
              GAINS OF 1,2,4,8 AND XX=NUMBER OF CHANNELS
              1-37;
        201 = RESTART START, USING VALUES SELECTED IN SA 200
        202 = DISPLAYS CONVERTED VALUE IN AC (FOR CHECKING CAL-
              IBRATION), ALSO BITS 4 AND 5 CONTROL GAIN
        203 = IOT SCOPE LOOP 65XX,XX EQUALS SR=6-11
        204 = SWITCH REGISTER CONTROLS CONVERSION RATE;
        205 = SWITCH REGISTER BIT 7-11 EQUALS MULTIPLEXER
              CHANNEL, 4 AND 5 EQUAL GAIN OF AMPLIFIER
        206 = READ A-D BUFFER TWICE
        ITCH REGISTER 0-11 EQUALS DELAY BETWEEN READINGS

        SET SWITCH REGISTER TO STARTING ADDRESS,
        LOAD ADDRESS,
        PRESS START,
        THE PROGRAM WILL STAY IN SECTION AND LOOP,

PRINTOUTS = NO

SWITCH REGISTER OPTIONS = YES
        SW0 = 1 OR UP ,., HALT ON ERROR
        SW1 = 1 OR UP ,., SCOPE LOOP
        SW2 = 1 OR UP ,., INHIBIT PRINTOUT
        SW3 = 1 OR UP ,., INHIBIT "OR" 1LSB TESTING
        SW4 = GAIN
        SW5 = GAIN
        SW6 = 1 OR UP ,., INHIBIT AVERAGING
        SW7-SW11 = CHANNELS TO BE TESTED (AT 1ST AND 2ND HALT)


MAINDEC-08-D6VA-DL-(D)

AFC-8 DIAGNOSTIC

ABSTRACT
        THIS PROGRAM IS A DIAGNOSTIC AND EXERCISER FOR THE
        AFC-8 LOW LEVEL ANALOG INPUT SYSTEM.  THE PROGRAM IS COMPOSED
        OF THREE SECTIONS:

        SYSTEM UNIT EXERCISER
        CALIBRATION AND ADJUSTMENT ROUTINES
        DATA COLLECTION ROUTINES
```

REQUIREMENTS
PDP-8/I OR 8/L STANDARD COMPUTER WITH ASR-33 TELETYPE
AFC-8
ADJUSTABLE PRECISION VOLTAGE SOURCE, EDC MV100N OR EQUIVALENT
DIGITAL TEST CABLE (OPTIONAL)
OSCILLOSCOPE, TEKTRONIX 453 OR EQUIVALENT WITH DIRECT PROBE

STORAGE - THE PROGRAM USES MEMORY LOCATIONS 0-7577.

LOADING - BINARY LOADER

STARTING PROCEDURE
IF THE DIGITAL TEST CABLE IS INSTALLED IN THE SYSTEM UNIT
TO BE EXERCISED, ALL SWITCHES ARE SET TO 0 (DOWN).
THIS SETTING WILL ALLOW ERROR MESSAGES TO BE TYPED AND ALLOW
THE PROGRAM TO PROCEED TO THE NEXT TEST.
IF THE TEST CABLE IS NOT INSTALLED, SET SR05-1 (UP), THIS WILL
ALLOW THE CHANNEL ADDRESSING TEST TO BE BYPASSED, SO THAT
ERRORS GENERATED BY THE ABSENCE OF THE CABLE WILL NOT BE
REPORTED.
SET SWITCHES TO 0200
PRESS LOAD ADDRESS KEY
SET SWITCHES
PRESS START KEY
THE PROGRAM WILL RESPOND BY TYPING A PERIOD (.) ON THE
TELEPRINTER TO INDICATE THAT IS OPERATING IN THE
"KEYBOARD MONITOR" MODE AND IS READY TO RECEIVE COMMANDS.
TYPE "ADTST" THEN THE ALT MODE KEY.
AFTER EACH PASS "ADTST" IS TYPED

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES

MAINDEC-08-D6WB-D

AA-50 D/A CONVERTER DIAGNOSTIC

ABSTRACT
THIS PROGRAM IS EXERCISER FOR THE AA-50 DIGITAL TO ANALOG CONVERTER.
DUE TO THE NATURE OF THE EQUIPMENT UNDER TEST, NO DIAGNOSTIC ERROR
TYPEOUTS OR HALTS CAN BE PROVIDED. THEREFORE, EACH TEST WILL PROVIDE AN OUTPUT
WAVE FROM WHICH MUST BE SCOPED.

REQUIREMENTS
FAMILY OF 8 COMPUTER WITH TELETYPE AA-50 D/A CONVERTER TEKTRONIX
SCOPE 453 OR EQUIVALENT X1 PROBE

STORAGE - PROGRAM OCCUPIES CORE LOCATION 0-1600

LOADING - BINARY LOADER

STARTING PROCEDURE

LOAD ADDRESS = 200
START ADDRESS= 200
WHEN STARTED THE PROGRAM TYPES OUT THE FOLLOWING MESSAGE =

TEST, DAC

AT THIS POINT THE PROGRAM WILL WAIT TO BE INFORMED AS TO WHICH
TEST WILL BE SELECTED AND ON WHAT DAC THE TEST WILL BE RUN.
A TYPICAL RESPONSE WOULD BE MADE IN THE FOLLOWING FORMAT:

1,9

WITH THE PRECEDING INFORMATION INPUT ON THE TELETYPE AND
UPON RECEIPT OF THE CARRIAGE RETURN. THE PROGRAM WOULD RUN TEST 1, ON DAC 9.

THIS DIAGNOSTIC CONTAINS SIX (6) TESTS.

1. INTERACTION TEST
2. CALIBRATION ROUTINE
3. POSITIVE RAMP
4. NEGATIVE RAMP
5. SWITCH REGISTER CONVERSION
6. VARIABLE TIME TEST

ANY GIVEN TEST CAN BE RUN ON ONLY ONE DAC AT A TIME. ANY ONE OF
18 DAC'S (0-17) MAY BE SELECTED. ONCE SELECTED AND STARTED A TEST
WILL RUN CONTINUOUSLY. HITTING THE "SPACE BAR" ON THE TELETYPE WHILE
A TEST IS RUNNING WILL CAUSE THE PROGRAM TO TYPE OUT THE MESSAGE
"TEST, DAC" AND WAIT FOR THE NEXT TEST AND DAC NUMBER TO BE SELECTED.

PRINTOUTS = YES

SWITCH REGISTER OPTIONS = YES

TEST 2
S.R. 11 USED TO STEP PROGRAM THROUGH CALIBRATION TABLE
TEST 5
S.R. CONTENTS CONVERTED TO OUTPUT VOLTAGE.
TEST 6
S.R. CONTENTS CONVERTED TO PARAMETERS FOR PRF OF OUTPUT WAVEFORM.

MAINDEC-08-D7CA-D

TYPESET-8 SYSTEM EXERCISER (TCSE)

ABSTRACT

THE TYPESET-8 SYSTEM EXERCISER (TCSE) IS INTENDED AS A TOOL IN
VERIFYING THE OPERATING ABILITY OF A TYPESETTING SYSTEM'S HARDWARE,
AND AS THE NORMAL MEANS FOR SYSTEMS ACCEPTANCE. THE TCSE PROGRAM
EXERCISES THE SYSTEM HARDWARE SIMULTANEOUSLY.

A SYSTEM CUSTOMIZER PROGRAM IS AN INTEGRAL PART OF THE TCSE PACKAGE. ITS
PURPOSE IS TO GENERATE A PROGRAM TAPE MATCHED TO THE SPECIFIC
CONFIGURATION OF THE TYPESET SYSTEM TO BE TESTED. INFORMATION
IS GIVEN TO THE CUSTOMIZER PROGRAM BY MEANS OF THE TELETYPE KEYBOARD.

REQUIREMENTS
AT LEAST A BASIC TYPESETTING SYSTEM IS REQUIRED,
THE SYSTEM TELETYPE MUST BE OPERATIONAL,
THE FOLLWOING HARDWARE CAN ALSO BE TESTED:

1. TC01/TC08 OR 552 DECTAPE
2. DF32 OR RF08 DISK
3. LP08 LINE PRINTER

MAINDEC-08-D81B-D

DB08A TEST

ABSTRACT
THE DB08A TEST PROGRAM IS A GO-NO GO FORM OF TEST FOR THE DB08A PROCESSOR BUFFER. IT IS PRIMARILY USED BY THE TECHNICIAN DURING INITIAL CHECK-OUT OF THE DB08A OR TO HELP ISOLATE A PROBLEM IN THE DB98A OR DB88A INTERPROCESSOR BUFFERS. ERRORS ARE FLAGGED BY TYPE-OUTS ON THE MODEL 33 TELEPRINTER. THESE TYPE-OUTS MAY BE SUPPRESSED ALLOWING A SHORT LOOP TO BE GENERATED FOR OSCILLASCOPE TROUBLE SHOOTING PURPOSES.

REQUIREMENTS
TO RUN THE DB08A TEST, THE OPERATOR NEEDS A DB08A AND A PDP-8 COMPUTER, THE DB08A MUST BE PLACED IN THE MAINTENANCE CONFIGURATION WITH THE TRANSMIT CABLE CONNECTED BACK TO THE RECEIVE CABLE INPUT. SEE DB88, 98, AND 99 SPECIFICATION.

STORAGE - THE PROGRAM RESIDES IN OCTAL LOCATIONS 0000 8 TO 60000 8.

LOADING - BINARY LOADER

STARTING PROCEDURE
SET THE SWITCHES TO 31 8 AND PRESS LOAD ADDRESS. SET THE SWITCHES TO SELECT THE DESIRED TEST FUNCTION AND PRESS START.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS = YES

SWITCH	CONDITION	MEANING
0	UP	DO ALL TESTS SEVEN TIMES EACH.
1	UP	DO COMMAND STATUS REGISTER TEST.
2	UP	DO AC DATA TRANSFER TEST.
3	UP	DO FLAG TEST.
4	UP	DO INTERRUPT TEST.
5	UP	DO MICRO-INSTRUCTION TEST.
6	UP	DO DATA CHANNEL DATA TEST.
7	--	NO ASSIGNMENT
8	UP	CONTINUE WITH TEST AFTER ERROR HALTS.
8	DN	RESTART TEST FROM THE TOP AFTER ERROR HALTS.
9	UP	INHIBIT ALL TYPEOUTS.
10	UP	DO NOT HALT ON ERRORS.
10	DN	HALT ON ERRORS.
11	UP	DO ALTERNATE 1S AND 0S (7777, 0000, ETC.) ON DCH DATA TEST.
11	DN	DO COUNT PATTERN ON DCH DATA TEST (0001,0002 ETC.)

MAINDEC-08-D8EB-D

DP01A IOT AND
DATA TESTS (WITH DEVICE CODE 30'S)

ABSTRACT

THE DP01A TEST CONSISTS OF TWO INDEPENDENT TEST SEQUENCE INTENDED TO VERIFY CORRECT OPERATION OF THE IOT INSTRUCTIONS AND CONTROL LOGIC ASSOCIATED WITH THE DP01A BIT SYNCHRONOUS DATA COMMUNICATION SYSTEM. ALTHOUGH THE TESTS ARE TREATED SEPARATELY, THEY MAY BE IN MEMORY AT THE SAME TIME.

REQUIREMENTS

MINIMUM CONFIGURATION PDP-8
MINIMUM CONFIGURATION DP01A
DP01A TESTER OR A 201 DATA PHONE.

LOADING = BINARY LOADER

STARTING PROCEDURE

ONCE THE PROGRAM HAS BEEN READ IN, SET THE AC SWITCH REGISTER TO 201 8 AND DEPRESS LOAD ADDRESS AND START KEYS. WHEN THE PROGRAM IS STARTED AT LOCATION 201 8, IT ENTERS A SYNC CHARACTER SETUP ROUTINE. THE PROGRAM WILL HALT AND WAIT FOR THE OPERATOR TO SPECIFY THE CHARACTER LENGTH DESIRED.

SWITCH SETTINGS CHARACTER LENGTH	SWITCH SETTINGS
6 BITS	0 UP
7 BITS	1 UP
8 BITS	2 UP
9 BITS	3 UP

DEPRESS CONTINUE - THE PROGRAM WILL HALT TO ALLOW THE
OPERATOR TO SELECT THE SWITCH OPTIONS HE WANTS. IF THE
OPERATOR WISHES TO LOOP ON THE TEST, HE SHOULD PUT SWITCH
0 UP.
AND IF THE DATA SET BEING USED HAS AN AUTOMATIC ANSWERING FEATURE,
SWITCH 1 SHOULD BE UP.

DEPRESS CONTINUE - THE PROGRAM WILL TEST THE FLAGS AND IOT'S
USED IN THE DP01A. IF AN ERROR OCCURS, THE PROGRAM WILL TYPE
OUT ON THE TELETYPE "EH" FOLLOWED BY A NUMBER.

PRINTOUTS = YES

SWITCH REGISTER OPTIONS = YES

MAINDEC-08-D8GA-D

DB88 TEST

ABSTRACT
THE DB88 TEST IS MADE UP OF A SINGLE PROGRAM WHICH IS LOADED
INTO BOTH PDP-8'S. THE PROGRAM ALLWOS THE OPERATOR TO SPECIFY ALL
THE PARAMETERS OF THE TEST TRANSMISSION: DIRECTION OF TRANSFER,
DATA, WORD COUNT, ADDRESS OF TRANSFER, AND NUMBER OF REPETITIONS.
ALL COMMANDS TO THE PROGRAM ARE ENTERED VIA THE TELETYPE AND
COMMANDS MAY BE ENTERED AT EITHER MACHINE TO START A TRANSFER.

REQUIREMENTS
TO RUN THIS TEST THE USER MUST HAVE TWO PDP-8'S AND A DB88 WHICH IS
COMPOSED OF TWO DB08'S.

STORAGE = THE PROGRAM OCCUPIES LOCATIONS 0000 8 TO 3777 8 OF CORE BANK 0.

LOADING = BINARY LOADER

STARTING PROCEDURE
SET THEPDP-8 SWITCH REGISTER TO 0200 8 AND PRESS LOAD ADDRESS AND START.

PRINTOUTS = YES

SWITCH REGISTER OPTIONS = YES

SWITCH	MEANING
0 = 0	ALLOW ERROR DISPLAY.
= 1	INHIBIT ERROR DISPLAY.
1 = 0	ALLOW DISPLAY OF "TEST OVER" MESSAGE
= 1	INHIBIT DISPLAY OF "TEST OVER" MESSAGE

MAINDEC-08-D8PA

PT08 TEST PROGRAM FOR USE WITH DATAPHONE
OPTIONS

TEST PROGRAM FOR PT08 CONTROLS

THIS TEST PROVIDES A MEANS OF CHECKING CHARACTER TRANSMISSION AND RECEPTION USING PT08 CONTROLS. TESTING IS PERFORMED BY CONNECTING THE CONTROL OUTPUT OF THE CONTROL INPUT AND COMPARING TRANSMITTED AND RECEIVED CHARACTERS. IN NO WAY DOES THIS TEST SUPERCEDE ANY EXISTING TELETYPE TESTS, AND IN FACT, IT IS NOT NECESSARY FOR CHECKING TELETYPE CONTROL OPERATION. HOWEVER, WHEN A F OPTION IS ADDED TO A PT08B OR A PT08C CONTROL, THIS TEST PROVIDES SUFFICIENT TESTING TO GUARANTEE AN ACCEPTABLE PRODUCTION UNIT.

CHARACTERS ARE TRANSMITTED IN A PSEUDO-RANDOM MANNER AND ALL FLAGS AND INTERRUPT CONDITIONS ARE CHECKED. TRANSMISSIONS USING EITHER 5-OR 8-BIT CODES CAN BE CHECKED ACCORDING TO THE CONTENTS OF LOCATION 265. THE C (265) ARE INITIALLY SET AT 7401 FOR 8-BIT CODES AND SHULD BE CHANGED TO 7741 FOR 5-BIT CODES.

1. STARTING PROCEDURE
   LOAD AT 200
   START WITH RECEIVER DEVICE CODE IN SWITCH REGISTER
   BITS 3 THROUGH 8 AS IN ANY IOT INSTRUCTION.

2. ERROR HALTS
   261/ TRANSMITTED AND RECEIVED CHARACTER ARE NOT THE SAME.
   C(AC) DISPLAYS RECEIVED CHARACTER.
   LOCATION 262 CONTAINS TRANSMITTED CHARACTER.

   266/ NO SKIP OCCURRED ON TRANSMITTER FLAG. (W707)

   302/ NO SKIP OCCURRED ON RECEIVER FLAG. (W706)

   310/ INTERRUPT BUS DID NOT CLEAR WHEN ALL FLAGS WERE CLEARED.

2.1 NO HALT CONDITIONS;
   (1) A BINARY COUNT SEQUENCE APPEARING IN THE ACCUMULATOR INDICATES CORRECT PROGRAM OPERATION.

   (2) A LOOP IN LOCATION 236 INDICATES THAT ONE OR BOTH FLAGS (W706 OR W707) DID NOT APPEAR; UNDER THIS CONDITION THE AC WILL BE STATIC.

MAINDEC-08-D8SC-D

DM01 EXERCISER

ABSTRACT

THE DM01 EXERCISER IS A PROGRAM WRITTEN TO EXERCISE THE DM01
DATA BREAK MULTIPLEXER TO ASSURE THAT IT CAN PROPERLY INTERLACE
DATA BREAKS FROM SEVERAL PERIPHERAL DEVICES TO THE PDP-8 COMPUTER.
IT DOES THIS BY EXERCISING SEVERAL DATA BREAK DEVICES SIMULTANEOUSLY.

REQUIREMENTS

FAMILY-OF-8 COMPUTER AND
DM01 DATA BREAK MULTIPLEXER, PLUS AT LEAST ONE OF THE FOLLOWING
TC01 DECTAPE AND/OR
TC58 MAGTAPE AND/OR
338 DISPLAY AND/OR
EXTENDED MEMORY AND/OR
RM08 DRUM OR
DF32 DISK OR
RF08 DISK

STORAGE - THE PROGRAM OCCUPIES ALL OF THE LOWEST 4K OF THE COMPUTER'S MEMORY
AND USES SAME OF THIS AREA AND AREAS IN OTHER MEMORY BANKS (IF AVAILABLE)
FOR DATA STORAGE.

LOADING - BINARY LOADER

STARTING PROCEDURE

MOUNT ONTO A DECTAPE TRANSPORT A REEL OF DECTAPE WHICH HAS THE STANDARD
MARK AND TIMING TRACK FORMAT (2702 BLOCKS, 201 WORDS EACH);
SET THE TRANSPORT SELECTOR TO 8, SET SWITCHT TO WRITE ENABLE.
SET SWITCH TO REMOTE.

MOUNT ONTO A MAGTAPE TRANSPORTA REEL OF MAGTAPE WHICHIS CERTIFIED TO
OPERATE AT 800 BPI WITH THE "WRITE-LOCK" RING IN (ABLE TO WRITE).
SET THE TRANSPORT SELECTOR TO 0 AND ON LINE.

SET UP THE DF32, DISK 0, SO THAT THE UPPER 16K MAY BE WRITTEN ON (NOT WRITE-LOCK).

SET UP RF08, DISK 0, SO THAT UPPERMOST LOCATIONS MAY BE WRITTEN ON
(NOT WRITE-LOCK) (256K).

SET UP RM08 DRUM SO THAT TRACK 77, SECTORS 50 TO 77 MAY BE WRITTEN ON (NOT WRITE-LOCK).

SET UP 338 DISPLAY SO THAT IT CAN BE OPERATED BY THE 8,

SET ACS TO 00200,

DEPRESS LOAD ADDRESS,

SET ACS PER SECTION 4.1 (NORMAL SETTING IS 0000);

DEPRESS START,

ANSWER QUESTIONS ASKED BY PROGRAM WITH "Y" FOR YES, "N" FOR NO,
AND NUMBER OF EXTRA MEMORY BANKS (BETWEEN 1 AND 7) (IF APPLICABLE).

AFTER INTERROGATION IS COMPLETE, PROGRAM WILL START EXERCISING THE DEVICES
WHOSE ANSWERS ARE "YES" AND THE DM01.

PRINTOUTS = YES

SWITCH REGISTER OPTIONS = YES

AC SWITCH	SET AS	ACTION ON PROGRAMS
0	1	DON'T HALT ON HARDWARE ERRORS
	0	HALT ON HARDWARE ERRORS
1	1	DON'T HALT ON DATA ERRORS
	0	HALT ON DATA ERRORS
2	1	DON'T PRINT HARDWARE ERRORS
	0	PRINT HARDWARE ERRORS
3	1	DON'T PRINT DATA ERRORS
	0	PRINT DATA ERRORS
4	1	LOOK AT AC5 FOR DISK/DRUM TRANSFER DIRECTION
	0	IGNORE AC5
5	1	WRITE
	0	READ
6	1	SUPPRESS DECTAPE EXERCISING
	0	NONE
7	1	SUPPRESS MAGTAPE EXERCISING
	0	NONE
8	1	SUPPRESS DISK/DRUM EXERCISING
	0	NONE
9	1	
	0	
10	1	
	0	
11	1	FREEZE MEMORY FIELD
	0	NONE

MAINDEC-08-D8V8-D-(D)

KW08S CLOCK TEST

ABSTRACT
THE TEST CHECKS AND DIAGNOSES THE BASIC OPERATIONS OF THE KW08S CLOCK
TO ASSURE ITS PROPER OPERATION.

REQUIREMENTS
FAMILY-OF-8 COMPUTER
KW08S CLOCK OPTION

STORAGE - THE PROGRAM OCCUPIES PAGES 0 TO 3 OF THE COMPUTER MEMORY.

LOADING - BINARY LOADER

STARTING PROCEDURE
TO RUN THE COMPLETE TEST, START AT LOCATION 0200.
TO PUT IN A 'SCOPE LOOP TO CHECK COUNTING, FLAG SETTING, CLEARING,
CLOCK ENABLE, ETC., START AT LOCATION 0600.

PRINTOUTS - NO

SWITCH REGISTER OPTIONS - NO.

MAINDEC-08-D8WA-D (L)

DC02

ABSTRACT
THIS PROGRAM CONSISTS OF THREE PARTS AND WILL TEST ALL FLAGS AND DATA
HANDLING CAPABILITY OF THE DC02 AND FROM 1 TO 12 ASSOCIATED TELETYPES.

REQUIREMENTS
PDP-8/I - PDP-8/L - PDP-12
DC02
FROM 1 TO 12 TELETYPES WITH READER AND PUNCH

STARTING PROCEDURE
TEST I
LOAD ADDRESS 200 -
SELECT THE STATIONS TO BE TESTED
SR00=1 TEST STATION 1
SR00=1 TEST STATION 2
ETC ETC
DEPRESS START, PROGRAM WILL HALT AT 202.
DEPRESS START AGAIN, ANY FURTHER HALTS ARE ERRORS.
NOTE: ALL READERS MUST BE IN THE FREE POSITION.
TEST II - 0600
TEST III- 1600

PRINTOUTS = YES

SWITCH REGISTER OPTIONS = NO

MAINDEC 08-D8XA-D(L)

XOR BUFFER OPTION DIAGNOSTIC
FOR USE WITH DP01A

ABSTRACT
THE XOR BUFFER DIAGNOSTIC OF 12 TESTS WHICH TEST POWER CLEAR COB (6661), ROB (6662) AND BOTH THE INCLUSIVE AND EXCLUSIVE OR FUNCTIONS.

STARTING PROCEDURE:S
LOAD THE PROGRAM USING THE BINARY LOADER,
LOAD ADDRESS 0200,
DEPRESS START
MACHINE WILL HALT AT 0202 WITH 7777 IN THE AC,
DEPRESS START AGAIN,
PROPER OPERATION IS INDICATED BY THE TELETYPE BELL
RINGING CONTINOUSLY,

PRINTOUTS = NO

SWITCH REGISTER OPTIONS = NO

MAINDEC 08-D8YC-D

UDC8 SYSTEM FUNCTION EXERCISER

ABSTRACT
THIS PROGRAM ALLOWS THE USER TO CHECKOUT, DEBUG, OR DEMONSTRATE THE UNIVERSAL DIGITAL CONTROLLER. THROUGH A SET OF PARAMETERS THE PROGRAM WILL INPUT AND/OR OUTPUT DATA ON ONE OR MORE I/O CHANNELS. THE INPUT DATA IS GENERATED BY AND THE OUTPUT DATA IS DETECTED BY SOME EXTERNAL SOURCE SUCH AS SWITCH OR LIGHT PANNELS. THE PARAMETERS ARE ENTERED VIA A SET OF DIRECTIVIES FROM THE TELETYPE KEYBOARD. AT ANY TIME, ANY ONE OR MORE OF THE PARAMETERS MAY BE CHANGED. THE PROGRAM CONTAINS 7 TEST ROUTINES. ALL OF THE TEST ROUTINES DO NOT NECESSARILY USE ALL OF THE DIRECTIVES.

REQUIREMENTS
FAMILY OF 8 COMPUTER WITH 4K OF MEMORY, A TELETYPE, A UDC8 WITH ASSOCIATED I/O MODULES AND SOME FORM OF INPUT GENERATING DEVICES AND OUTPUT DETECTING DEVICES SUCH AS SWITCH OR LIGHT PANELS,

STORAGE = THIS PROGRAM OCCUPIES CORE LOCATIONS 0000-4577

LOADING = BINARY LOADER

STARTING PROCEDURE
START THE PROGRAM AT 0200. THE PROGRAM WILL TYPE OUT AN ASTERISK (*). THIS SIGNIFIES THAT THE PROGRAM IS READY TO RECEIVE DIRECTIVES.

PRINTOUTS = YES

SWITCH REGISTER OPTIONS = NO

MAINDEC-08-D9AD-D

TC58 DATA RELIABILITY TEST
(7 TRACK)

ABSTRACT

THE TC58 DATA RELIABILITY TEST IS PRIMARILY DESIGNED FOR THE COLLECTION OF STATISTICAL INFORMATION PERTAINING TO THE DATA RELIABILITY OF THE DRIVES THAT MAY BE ASSOCIATED WITH THE TC58 MAGNETIC TAPE CONTROL. THE PROGRAM IS ALSO DESIGNED TO BE USABLE AS AN AID TO THE HARDWARE DEBUGGING AND MAINTENANCE OF TC58 MAGNETIC TAPE CONTROL AND ITS ASSOCIATED MAGNETIC TAPE DRIVES. THIS PROGRAM MAY ALSO BE USED AS AN EXTENDED DATA RELIABILITY ACCEPTANCE TEST.

REQUIREMENTS

PDP-8
TC58 MAGNETIC TAPE CONTROL
1 TO 8 TU20 OR SIMILAR MAGNETIC TAPE TRANSPORTS
7 TRACK ONLY

STORAGE - THE PROGRAM OCCUPIES MOST OF MEMORY FROM ADDRESS 0 TO 7777.

LOADING - BINARY LOADER

STARTING PROCEDURE

THE TC58 DATA RELIABILITY TEST HAS 2 STARTING ADDRESSES.

0200 ENTER ALL PARAMETER AND TEST SELECTIONS VIA TELETYPE KEYBOARD.
2400 ENTER DRIVE AND TEST PARAMETERS VIA SWS, MAKE 1 WRITE OR WRITE/READ PASS TO EOT AND HALT. (SEE PARAGRAPH 4.1 FOR DRIVE AND TEST PARAMETERS THAT MAY BE SELECTED.)

TO START AT 2400
SET SWITCHES TO 2400 8
DEPRESS LOAD ADDRESS
SET AC SWITCHES TO SELECT DRIVE AND TEST PARAMETERS
DEPRESS START KEY
THE PROGRAM WILL REWIND THE DRIVE SELECTED TO LOAD POINT, SAVE THE TEST PARAMETERS AND HALT AT ADDRESS 2412. SET AC SWITCHES PER PARAGRAPH 4.1 FOR SECOND LOAD.
DEPRESS START KEY
THE SECOND SET OF PARAMETERS WILL BE SAVED AND THE PROGRAM WILL HALT AT ADDRESS 2417.
CLEAR ALL AC SWITCHES TO 0 OR SET AS DESIRED PER PARAGRAPH 5.1
DEPRESS START KEY
THE PROGRAM WILL EXERCISE TAPE IN THE TEST SEQUENCE SELECTED UNTIL EOT IS REACHED AND THEN TYPE OUT ACCUMULATED ERROR INFORMATION AND HALT.

```
        TO START AT 0200
        SET AC SWITCHES TO 200 8
        DEPRESS LOAD ADDRESS
        DEPRESS START KEY

PRINTOUTS = YES

SWITCH REGISTER OPTIONS = YES

AS SWITCHES     0  1  2  3  4  5  6  7  8  9  10  11

FIRST LOAD

        SWS             USAGE

        0,1,2           SELECT DRIVE
                        000 = DRIVE 0
                        001 = DRIVE 1
                         .        .
                         .        .
                         .        .
                        111 = DRIVE 7

        3               SELECT READ PASS
                        0 = NO READ PASS
                        1 = MAKE READ PASS

        4,5             SELECT WRITE STOP MODE
                        00 = NON STOP
                        01 = START STOP
                        10 OR 11 = RANDOM NON STOP, START STOP DELAYS

        6,7             SELECT RECORD LENGTH SEQUENCE
                        00 = MIN, 24 CHARACTER RECORDS
                        01 = MAX, 4008 CHARACTER RECORDS
                        10 = MIN TO MAX, 24 TO 4008
                        11 = MAX TO MIN, 4008 TO 24

        8               SELECT PARITY
                        0 EVEN
                        1 ODD

        9,10,11         SELECT PATTERN
                        (SEE PARAGRAPHS 4.3.2.4 AND 4.3.2.5)

        SECOND LOAD

        SWS             USAGE

        4,5             SELECT WRITE SEQUENCE
                        00 = WRITE PASS TO EOT
                        01 = WRITE PASS EXIT EVERY SEQUENCE
                        10 OR 11 = WRITE PASS EXIT EVERY RECORD
```

```
        7,8             SELECT WRITE STOP MODE
                        00 = NON STOP
                        01 = START STOP
                        10 OR 11 = RANDOM NON STOP, START STOP DELAYS


MAINDEC 08-D9BA-DL

TC-58 DRIVE FUNCTION TIMER

ABSTRACT
        THE TC58 DRIVE FUNCTION TIMER PROGRAM IS DESIGNED TO BE AN AID IN THE
        HARDWARE DEBUGGING AND MAINTENANCE OF THE TC58 MAGNETIC TAPE CONTROL
        AND ITS ASSOCIATED MAGNETIC TAPE DRIVES.  THE PROGRAM WILL OPERATE
        ON ANY CONFIGURATION OF 1 TO 8 45 OR 75 INCH PER SECOND 7 OR 9 TRACK DRIVES.

        SELECTED OPERATIONS ARE INITIATED, TIMED AND THE TIMES ARE THEN TYPED
        IN DECIMAL MILLISECONDS.  THERE IS NO LIMIT CHECKING ON TIMES BY THE
        PROGRAM, THE DECISIONS ON THE VALIDITY OF TIMES TYPED MUST BE MADE
        EXTERNAL TO THE PROGRAM OR BY THE PERSON OPERATION THIS TEST.

REQUIREMENTS
        PDP-8
        TC58 MAGNETIC TAPE CONTROL
        1 TO 8 TU20 7 OR 9 TRACK OR SIMILAR MAGNETIC TAPE TRANSPORTS

STORAGE - THE PROGRAM OCCUPIES MOST OF THE 4K OF MEMORY

LOADING - BINARY LOADER

STARTING PROCEDURE
        LOAD ADDRESS 200
        SET AC SWITCHES TO SELECT DRIVES
        PRESS START
        NORMAL HALT AT 0207
        SET AC SWITCHES TO INDICATE 9 TRACK DRIVES
        PRESS CONTINUE
        NORMAL HALT AT 0212,
        SET ALL AC SWITCHES TO 0 OR AS DESIRED
        PRESS CONTINUE,  THE PROGRAM WILL REWIND ALL
        DRIVES TO BOT, INITIATE SELECTED OPERATIONS
        AND PRINT ACCUMULATED TIMES IN MILLISECONDS.

PRINTOUTS - YES
```

```
SWITCH REGISTER OPTIONS - YES
        ANY CONFIGURATION OF 1 TO 8 (7 OR 9 TRACK) DRIVES MAY
        BE SELECTED VIA AC SWITCHES Ø TO 7.

        AC  SW Ø = 1    DRIVE Ø
        AC  SW 1 = 1          1
        AC  SW 2 = 1          2
        !   !  ! = !          !
        AC  SW 7 = 1    DRIVE 7

        AT LEAST ONE DRIVE MUST BE SELECTED.

        OPERATIONAL SWITCH SETTINGS

        THE TEST ONLY HAS 1 SWITCH OPTION
        SWØ=Ø IS HALT AT END OF TEST
        SWØ=1 IS REPEAT ALL TESTS ON DRIVES CURRENTLY SELECTED.
```

MAINDEC-08-D9CC-D

TC58 RANDOM EXERCISER

ABSTRACT
THE TC58 RANDOM EXERCISER TEST IS A TEST PROGRAM DESIGNED TO SIMULATE TAPE SYSTEM USAGE. ANY CONFIGURATION OF 1 THROUGH TU20 (OR SIMILAR) 7-AND/OR 9-TRACK DRIVES MAY BE CONCURRENTLY TESTED.

REQUIREMENTS
PDP-8
TC58 MAGNETIC TAPE CONTROL
1 THROUGH 8 TU20-7-OR 9-TRACK (OR SIMILAR MAGNETIC TAPE TRANSPORTS)
4K TO 32K OF CORE MEMORY

LOADING - BINARY LOADER

STARTING PROCEDURE
LOAD ADDRESS TO 0200
SET MEMORY PARAMETERS VIA AC SWS 9, 10 AND 11
0=4K 1=8K 2=12K 3=16K
4=20K 5=24K 6=28K 7=32K
PRESS START
AFTER MEMORY PARAMETERS HAVE BEEN CLEARED, THE FOLLOWING MESSAGE WILL BE TYPED

SELECT DRIVES
DRV TRK

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES

MAINDEC-08-D9DE-D

TC58 INSTRUCTION TEST - PART 1

ABSTRACT
THE TC58 INSTRUCTION TEST IS A SERIES OF INCREMENTAL SUBTESTS DESIGNED TO AID IN THE CHECKOUT AND MAINTENANCE OF THE TC58 MAGNETIC TAPE SYSTEM.

REQUIREMENTS
PDP-8
TC58
TU20, 7 OR 9 TRACK DRIVE
TU30, 7 OR 9 TRACK DRIVE

STORAGE - 4K

LOADING - BINARY LOADER

STARTING PROCEDURE
SET DRIVE 0 ON LINE AT BOT.
LOAD ADDRESS 200 8,
SET AC SW8-11
SET AC SW4 FOR CORRECT TRACK.

```
        SET AC SW6 IF DRIVE IS A TU30
        PRESS START.

PRINTOUTS = YES

SWITCH REGISTER OPTIONS = YES
        AC SW8-11       SELECT TESTS
             0=         IOT TEST PART 1
             1=         COMMAND REGISTER BIT AND DATA TEST
             2=         DATA CHANNEL TRANSFER DIRECTION
             3=         DATA BUFFER BIT AND DATA TEST
             4=         IOT TEST PART 2
             5=         COMMAND DECODING
             6=         TAPE MOTION TEST
             7=         FUNCTIONS TEST
            10=         WRITE PARITY TEST
            11=         WRITE HEAD POLARITY TEST
            12=         READ PARITY ERRORS TEST
            13=         TEST ERROR FUNCTIONS

        AC SW0=0        GO TO NEXT TEST
              =1        LOOP ON CURRENT TEST
             1=1        DC SCOPE LOOP
             2=1        POWER DOWN
             3=1        RING BELL ON ERROR
             4=0        7 TRACK
             4=1        9 TRACK
             5=1        SUPPRESS TEST NUMBER TYPEOUT
             6=1        DRIVE = TU30


MAINDEC-08-D9EC

TC58 INSTRUCTION TEST - PART 2

ABSTRACT
        THE TC58 INSTRUCTION TEST IS A SERIES AT INCREMENTAL SUBTESTS
        DESIGNED TO AID IN THE CHECKOUT AND MAINTENANCE OF THE TC58
         MAGNETIC TAPE SYSTEM.

REQUIREMENTS
        PDP-8
        TC58
        TU20, 7 OR 9 TRACK DRIVE

STORAGE - 4K

LOADING - BINARY LOADER

STARTING PROCEDURE
        SET DRIVE 0 ON LINE AT BOT.
        LOAD ADDRESS 200 8.
        SET AC SW9 = 11
        SET AC SW4 FOR CORRECT TRACK.
        PRESS START.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES
```

```
        AC      SW0=0           GO TO NEXT TEST
                  =1            LOOP ON CURRENT TEST
                 1=1            DC SCOPE LOOP
                 2=1            POWER DOWN
                 3=1            RING BELL ON ERROR
                 4=0            7 TRACK
                 4=1            9 TRACK
                 5=1            SUPPRESS TEST NUMBER TYPEOUT
        AC      SW9-11          SELECT TESTS
                 0=             MANUAL INTERVENTION TESTS
                 1=             CHANGE DIRECTION AND CONTINUE MODE
                 2=             CRC AND CORE DUMP 9 TRACK TESTS


MAINDEC-08-D9FC-D

TC58 DATA RELIABILITY TEST (9 TRACK)

ABSTRACT
        THE TC58 DATA RELIABILITY TEST IS PRIMARILY DESIGNED FOR THE COLLECTION
        OF STATISTICAL INFORMATION PERTAINING TO THE DATA RELIABILITY OF THE
        TAPE DRIVES THAT MAY BE ASSOCIATED WITH THE TC58 MAGNETIC TAPE CONTROL.
        THE PROGRAM IS ALSO DESIGNED TO BE USABLE AS AN AID TO THE HARDWARE DEBUGGING
        AND MAINTENANCE OF THE TC58 MAGNETIC TAPE CONTROL AND ITS ASSOCIATED
        MAGNETIC TAPE DRIVES.  THIS PROGRAM MAY ALSO BE USED AS AN EXTENDED
        DATA RELIABILITY ACCEPTANCE TEST.

REQUIREMENTS
        PDP-8
        TC58 MAGNETIC TAPE CONTROL
        1 TO 8 TU20 OR SIMILAR MAGNETIC TAPE TRANSPORTS
        9 TRACK ONLY

STORAGE - THE PROGRAM OCCUPIES MOST OF MEMORY FROM ADDRESS 0 TO 7777.

LOADING - BINARY LOADER

STARTING PROCEDURE
        0200            ENTER ALL PARAMETER AND TEST SELECTION VIA
                        TELETYPE KEYBOARD.
        2400            ENTER DRIVE AND TEST PARAMETERS VIA AC SWS, MAKE
                        1 WRITE OR WRITE/READ PASS TO EOT AND HALT.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES
        AC SWITCHES     0 1 2 3 4 5 6 7 8 9 10 11

        FIRST LOAD

            SWS         USAGE
            0,1,2       SELECT DRIVE
                        000=DRIVE0
                        001=DRIVE1
                         .    .
                         .    .
                         .    .
                        111=DRIVE7
```

```
            3           SELECT READ PASS
                        Ø=NO READ PASS
                        1=MAKE READ PASS

            4,5         SELECT WRITE STOP MODE
                        ØØ=NON STOP
                        Ø1=START STOP
                        1Ø OR 11 = RANDOM NON STOP, START STOP DELAYS

            6,7         SELECT RECORD LENGTH SEQUENCE
                        ØØ=MIN, 24 CHARACTER RECORDS
                        Ø1=MAX, 4ØØ8 CHARACTER RECORDS
                        1Ø=MIN TO MAX, 24 TO 4ØØ8
                        11=MAX TO MIN, 4ØØ8 TO 24

            8           SELECT PARITY
                        Ø EVEN
                        1 ODD

            9,1Ø,11     SELECT PATTERN

        SECOND LOAD

            SWS         USAGE
            4,5         SELECT WRITE SEQUENCE
                        ØØ=WRITE PASS TO EOT
                        Ø1=WRITE PASS EXIT EVERY SEQUENCE
                        1Ø OR 11 = WRITE PASS EXIT EVERY RECORD

            7,8         SELECT WRITE STOP MODE
                        ØØ=NON STOP
                        Ø1=START STOP
                        1Ø OR 11=RANDOM NON STOP, START STOP DELAYS

            1Ø,11       SELECT DENSITY
                        ØØ=2ØØ BPI
                                        ILLEGAL FOR 9 TRACK
                        Ø1=556 BPI
                        1Ø OR 11 = 8ØØ BPI


MAINDEC-Ø8-D9GA-D(D)

TC58 DATA RELIABILITY TEST
(9 TRACK TU-3Ø VERSION)

ABSTRACT
        THE TC58 DATA RELIABILITY TEST IS PRIMARILY DESIGNED FOR THE COLLECTION
        OF STATISTICAL INFORMATION PERTAINING TO THE DATA RELIABILITY OF THE
        TAPE DRIVES THAT MAY BE ASSOCIATED WITH THE TC58 MAGNETIC TAPE CONTROL.
        THE PROGRAM IS ALSO DESIGNED TO BE USABLE AS AN AID TO THE HARDWARE DE-
        BUGGING AND MAINTENANCE OF THE TC58 MAGNETIC TAPE CONTROL AND ITS ASSOCIATED
        MAGNETIC TAPE DRIVES.  THIS PROGRAM MAY ALSO BE USED AS AN EXTENDED DATA
        RELIABILITY ACCEPTANCE TEST.

REQUIREMENTS
        PDP-8
        TC58 MAGNETIC TAPE CONTROL
        1 TO 8 TU3Ø OR SIMILAR MAGNETIC TAPE TRANSPORTS
```

9 TRACK ONLY

STORAGE - THE PROGRAM OCCUPIES MOST OF MEMORY FROM ADDRESS 0 TO 7777.

LOADING - BINARY LOADER

STARTING PROCEDURE
SET AC SWITCHES TO 200(8)
DEPRESS LOAD ADDRESS
DEPRESS START KEY

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - NO

MAINDEC-08-D9IB-D

PDP-I/L DC04-C WIRE STORAGE
INTERFACE OPTION DIAGNOSTIC
PROGRAM (IN-FIELD VERSION)

ABSTRACT
THE DC04-C WIRE STORAGE INTERFACE DIAGNOSTIC PROGRAM (IN FIELD VERSION) TESTS THE DATA HANDLING CAPABILITIES OF THE DC04-C THROUGH THE USE OF A NON-PROGRAM CONTROLLED IN-FIELD TESTER. ONLY ONE DC04-C UNIT MAY BE TESTED AT ONE TIME.

THE DC04-C ECHO PROGRAM IS ALSO AVAILABLE IN CORE AND TRANSLATES NEWS LINE (TTS) CODE TO ASCII AND DISPLAYS THE INPUT ON THE TTY. (THIS APPLIES TO LOW AND MEDIUM SPEED LINES ONLY.)

IF AN LP08 LINE PRINTER OPTION IS AVAILABLE, HIGH SPEED LINE INFORMATION CAN BE ECHOED BY MAKING THE CHANGES TO THE EXISTING PROGRAM.

THE DIAGNOSTIC PORTION CONSISTS OF THE FOLLOWING TESTS;

TEST1: LIMITED CONTROL TEST
TEST2: DATA TEST

REQUIREMENTS
PDP-8/L WITH DC04-C OPTION, IN-FIELD TESTER, AND TELETYPE.

STORAGE - 4K OF CORE REQUIRED

LOADING - BINARY LOADER

STARTING PROCEDURE
SET SR TO STARTING ADDRESS (LISTED BELOW), LOAD ADDRESS, SET SR TO SELECT UNIT NUMBER AND SPEED AND ANY DESIRED OPTION, THEN START.
NOTE: THIS PROGRAM IS SET UP TO USE DEVICE CODE "15", IF IT IS DESIRED TO CHANGE THE DEVICE CODE, LOAD ADDRESS 100, SET SR 3-8 TO NEW DEVICE CODE, AND START, WHEN THE CHANGES HAVE BEEN MADE THE PROGRAM STOPS AT 121 WITH THE NEW DEVICE CODE IN THE AC.

STARTING ADDRESS	RESULT
100	RESET DEVICE CODE TO CODE IN SR3-8
200	RUN DIAGNOSTIC PROGRAM

```
1000                    RUN ECHO PROGRAM

PRINTOUTS = YES
```

SWITCH REGISTER OPTIONS - YES

SR BIT SET	YIELD
0	INHIBIT ERROR HALTS.
2	RUN TEST 2 CONTINUOUSLY
6	SET FOR MEDIUM SPEED UNIT.
7	SET FOR HIGH SPEED UNIT.

SR BITS 6 AND 7 MUST BE CLEAR FOR A LOW SPEED UNIT.

8-11	UNIT NUMBER TO BE TESTED IN OCTAL.

MAINDEC-08-D9KA-D-(D)

FAMILY-OF-8 MULTI BREAK
DEVICE EXERCISER

ABSTRACT

THE FAMILY-OF-8 MULTI BREAK DEVICE EXERCISER IS A PROGRAM WHICH VERIFIES THE PROPER INTERLACING OF DATA BREAKS BY EXERCISING ONE OR MORE OF THE DATA BREAK DEVICES SIMULTANEOUSLY. WHILE WAITING FOR INTERRUPTS, A BACKGROUND PROGRAM IS EXECUTED WHICH CONSISTS OF MONITORING THE CURRENT ADDRESS REGISTERS OF ALL THREE CYCLE BREAK DEVICES AND EXERCISING THE EXTENDED ARITHMETIC ELEMTNS (EAE). (THE EAE PORTION OF BACKGROUNG MAY BE INHIBITED.) THIS PROGRAM MAY BE LOADED INTO AND RUN FROM ANY EXISTING MEMORY FIELD, AND WILL AUTOMATICALLY RELOCATE TO A RANDOMLY SELECTED MEMORY FIELD AFTER EACH EIGHTH INTERRUPT (PROVIDED DECTAPE IS NOT IN SEARCH).

UNDER NO CIRCUMSTANCES SHOULD THIS EXERCISER BE CONSIDERED A COMPLETE TEST OF THE PROCESSOR AND THE DEVICES EXERCISED.

REQUIREMENTS

PDP-8, 8/I, 8/L, 8/E COMPUTER AND
APPROPRIATE DATA BREAK MULTIPLEXER AND/OR
TC01/TC08 DECTAPE (UP TO 8 TRANSPORTS) AND/OR
RK08 DISK SYSTEM (UP TO 4 DISK FILES) AND/OR
DF32 OR RF08 DISK SYSTEM (UP TO 4 DISKS) AND/OR
EXTENDED ARITHMETIC ELEMENT (EAE) WHICH IS PDP8, 8/I COMPATIBLE AND
ASR-33 TELETYPE OR EQUIVALENT DEVICE.

STORAGE - 4K REQUIRED, UP TO 32K MAY BE UTILIZED.

LOADING - BINARY LOADER

STARTING PROCEDURE
LOAD ADDRESS 0200 WITH THE IF AND DF SET TO THE PROGRAM FIELD.
CLEAR ALL SWITCHES
IF THERE IS NO EXTENDED MEMORY, SET SR BIT 10 TO A 1.
IF THERE IS NO EAE, SET SR BIT 9 TO A 1. IF THE EAE IS EXERCISED DATA REQUEST LATE ERRORS FOR THE RK08 AND/OR RF08 WILL BE COUNTED AND REPORTED PERIODICALLY.
DEPRESS "START" ("CLEAR" THEN "CONTINUE" ON A PDP8/E

PRINTOUTS = YES

SWITCH REGISTER OPTIONS = YES

SR BIT	YIELD
0	INHIBIT HARDWARE ERROR HALTS EXCEPT FOR BACKGROUND ERRORS.
1	INHIBIT DATA ERROR HALTS EXCEPT FOR BACKGROUND ERRORS.
2	INHIBIT HARDWARE ERROR PRINTOUTS.
3	INHIBIT DATA ERROR PRINTOUTS
4	RECOGNIZE SR5 CONTROL
5	IF SET TO 0, DF32 OR RF08 READ ONLY, IF SET TO 1, DF32 OR RF08 WRITE ONLY. (NO DATA CHECKING IS DONE.)
6	KILL DECTAPE EXERCISE.
7	KILL RK08 EXERCISE.
8	KILL DF32 OR RF08 EXERCISE.
9	KILL EAE PORTION OF BACKGROUND.
10	INHIBIT PROGRAM RELOCATION.
11	FREEZE PRESENT BREAK FIELDS AND DEVICE UNIT SELECTION.

MAINDEC-08-D9MA-D

DP01A BIT SYNCHRONOUS DATA
COMMUNICATION SYSTEM IOT
AND DATA TEST 6301

ABSTRACT
THE DP01A DIAGNOSTIC CONSISTS OF TWO TEST SEQUENCES INTENDED TO VERIFY PROPER OPERATION OF ALL IOT INSTRUCTIONS AND ASSOCIATED CONTROL LOGIC. THIS PROGRAM IS UNIQUE IN ITS OPERATION IN THAT DP01A TRANSMITTER IS CONNECTED BACK TO ITS OWN RECEIVER, AND THAT THE COMPUTER GENERATES ALL NECESSARY TIMING UNDER PROGRAM CONTROL.

REQUIREMENTS
A MINIMUM CONFIGURATION FAMILY OF 8 PROCESSOR
ASR-33
A MINIMUM CONFIGURATION DP01A
A DP01A TEST PLUG
JUMPER LEADS

STARTING PROCEDURE
REMOVE THE W023 PLUG AT LOCATION A3
INSERT DP01A TEST PLUG.

CONNECT A WIRE FROM THE OUTPUT OF THE IOT DECODER
6X54 TO THE PULSE INPUT OF THE DCD GATE OF THE
TIMING FLIP-FLOP.

REMOVE THE LOCAL TIMING CLOCK IF ANY.

INSERT THE NINE (9) BIT WORD LENGTH SELECTOR PLUG
INTO THE 50 PIN CANNON CONNECTOR.

SET THE ADDRESS SWITCHES TO 0200 AND THE DATA
SWITCHES AS SHOWN ABOVE TYPICALLY 6101 TO CAUSE THE
TYPE OUT, RING THE BELL AT END OF TEST AND NINE BIT
SELECTOR PLUG IS IN.

DEPRESS START.

PRINTOUTS = NO

SWITCH REGISTER OPTIONS = YES

SR00 = 1	HALT ON ERROR
SR01 = 1	PRINT ERROR NUMBER
SR02 = 1	SCOPE LOOP ON ROUTINE CAUSING ERROR
SR03 = 1	UNUSED
SR04 = 1	UNUSED
SR05 = 1	RING BELL AT END OF TEST
SR06 = 1	TYPE OF DATA TEST WANTED
SR07 = 1	TYPE OF DATA TEST WANTED
SR08 = 1	SIX BIT WORD LENGTH
SR09 = 1	SEVEN BIT WORD LENGTH
SR10 = 1	EIGHT BIT WORD LENGTH
SR11 = 1	NINE BIT WORD LENGTH

MAINDEC-08-D9NA-D

DP01A BIT SYNCHRONOUS DATA
COMMUNICATION SYSTEM IOT
AND DATA TEST 6501

ABSTRACT

THE DP01A DIAGNOSTIC CONSISTS OF TWO TEST SEQUENCES INTENDED
TO VERIFY PROPER OPERATION OF ALL IOT INSTRUCTIONS AND
ASSOCIATED CONTROL LOGIC. THIS PROGRAM IS UNIQUE IN ITS
OPERATION IN THAT THE DP01A TRANSMITTER IS CONNECTED BACK TO
ITS OWN RECEIVER, AND THAT THE COMPUTER GENERATES ALL
NECESSARY TIMING UNDER PROGRAM CONTROL.

REQUIREMENTS

A MINIMUM CONFIGURATION FAMILY OF 8 PROCESSOR
ASR-33
A MINIMUM CONFIGURATION DP01A
A DP01A TEST PLUG
JUMPER LEADS

STARTING PROCEDURE

```
        REMOVE THE W023 PLUG AT LOCATION A3
        INSERT CP01A TEST PLUG.

        CONNECT A WIRE FROM THE OUTPUT OF THE IOT DECODER
        6X54 TO THE PULSE INPUT OF THE DCD GATE OF THE
        TIMING FLIP-FLOP.

        REMOVE THE LOCAL TIMING CLOCK IF ANY.

        INSERT THE NINE (9) BIT WORD LENGTH SELECTOR PLUG
        INTO THE 50 PIN CANNON CONNECTOR

        SET THE ADDRESS SWITCHES TO 0200 AND THE DATA
        SWITCHES AS SHOWN ABOVE TYPICALLY 6101 TO CAUSE THE
        TYPE OUT, RING THE BELL AT END OF TEST AND NINE BIT
        SELECTOR PLUG IS IN.
        DEPRESS START.

PRINTOUTS = NO

SWITCH REGISTER OPTIONS = YES
        SR00 = 1        HALT ON ERROR
        SR01 = 1        PRINT ERROR NUMBER
        SR02 = 1        SCOPE LOOP ON ROUTINE CAUSING ERROR

        SR03 = 1        UNUSED
        SR04 = 1        UNUSED
        SR05 = 1        RING BELL AT END OF TEST

        SR06 = 1        TYPE OF DATA TEST WANTED
        SR07 = 1        TYPE OF DATA TEST WANTED
        SR08 = 1        SIX BIT WORD LENGTH

        SR09 = 1        SEVEN BIT WORD LENGTH
        SR10 = 1        EIGHT BIT WORD LENGTH
        SR11 = 1        NINE BIT WORD LENGTH


MAINDEC-08-D9PA-D

DP01A BIT SYNCHRONOUS DATA
COMMUNICATION SYSTEM IOT
AND DATA TEST 6601

ABSTRACT
        THE DP01A DIAGNOSTIC CONSISTS OF TWO TEST SEQUENCES INTENDED
        TO VERIFY PROPER OPERATION OF ALL IOT INSTRUCTIONS AND
        ASSOCIATED CONTROL LOGIC.  THIS PROGRAM IS UNIQUE IN ITS
        OPERATION IN THAT THE DP01A TRANSMITTER IS CONNECTED BACK TO
        ITS OWN RECEIVER, AND THAT THE COMPUTER GENERATES ALL
        NECESSARY TIMING UNDER PROGRAM CONTROL.

REQUIREMENTS
        A MINIMUM CONFIGURATION FAMILY OF 8 PROCESSOR
        ASR-33
        A MINIMUM CONFIGURATION DP01A
        A DP01A TEST PLUG
        JUMPER LEADS
```

STARTING PROCEDURE
REMOVE THE W023 PLUG AT LOCATION A3
INSERT DP01A TEST PLUG

CONNECT A WIRE FROM THE OUTPUT OF THE IOT DECODER
6X54 TO THE PULSE INPUT OF THE DCD GATE OF THE
TIMING FLIP-FLOP.

REMOVE THE LOCAL TIMING CLOCK IF ANY.

INSERT THE NINE (9) BIT WORD LENGTH SELECTOR PLUG
INTO THE 50 PIN CANNON CONNECTOR.

SET THE ADDRESS SWITCHES TO 0200 AND THE DATA
SWITCHES AS SHOWN ABOVE TYPICALLY 6101 TO CAUSE THE
TYPE OUT, RING THE BELL AT END OF TEST AND NINE BIT
SELECTOR PLUG IS IN.
DEPRESS START

PRINTOUTS = NO

SWITCH REGISTER OPTIONS = YES

SR00 = 1	HALT ON ERROR
SR01 = 1	PRINT ERROR NUMBER
SR02 = 1	SCOPE LOOP ON ROUTINE CAUSING ERROR
SR03 = 1	UNUSED
SR04 = 1	UNUSED
SR05 = 1	RING BELL AT END OF TEST
SR06 = 1	TYPE OF DATA TEST WANTED
SR07 = 1	TYPE OF DATA TEST WANTED
SR08 = 1	SIX BIT WORD LENGTH
SR09 = 1	SEVEN BIT WORD LENGTH
SR10 = 1	EIGTH BIT WORD LENGTH
SR11 = 1	NINE BIT WORD LENGTH

MAINDEC-08-D9QA-D

DP01A BIT SYNCHRONOUS DATA
COMMUNICATION SYSTEM IOT
AND DATA TEST 6701

ABSTRACT

THE DP01A DIAGNOSTIC CONSISTS OF TWO TEST SEQUENCES INTENDED
TO VERIFY PROPER OPERATION OF ALL IOT INSTRUCTIONS AND
ASSOCIATED CONTROL LOGIC. THIS PROGRAM IS UNIQUE IN ITS
OPERATION IN THAT THE DP01A TRANSMITTER IS CONNECTED BACK TO
ITS OWN RECEIVER, AND THAT THE COMPUTER GENERATES ALL
NECESSARY TIMING UNDER PROGRAM CONTROL.

REQUIREMENTS

A MINIMUM CONFIGURATION FAMILY OF 8 PROCESSOR
ASR-33
A MINIMUM CONFIGURATION DP01A
A DP01A TEST PLUG
JUMPER LEADS

STARTING PROCEDURE

REMOVE THE W023 PLUG AT LOCATION A3
INSERT DP01A TEST PLUG.

CONNECT A WIRE FROM THE OUTPUT OF THE IOT DECODER
6X54 TO THE PULSE INPUT OF THE DCD GATE OF THE
TIMING FLIP-FLOP.

REMOVE THE LOCAL TIMING CLOCK IF ANY.

INSERT THE NINE (9) BIT WORD LENGTH SELECTOR PLUG
INTO THE 50 PIN CANNON CONNECTOR.

SET THE ADDRESS SWITCHES TO 0200 AND THE DATA
SWITCHES AS SHOWN ABOVE TYPICALLY 6101 TO CAUSE THE
TYPE OUT, RING THE BELL AT END OF TEST AND NINE BIT
SELECTOR PLUG IS IN.

DEPRESS START

PRINTOUTS = NO

SWITCH REGISTER OPTIONS = YES

SR00 = 1		HALT ON ERROR
SR01 = 1		PRINT ERROR NUMBER
SR02 = 1		SCOPE LOOP ON ROUTINE CAUSING ERROR
SR03 = 1		UNUSED
SR04 = 1		UNUSED
SR05 = 1		RING BELL AT END OF TEST
SR06 = 1		TYPE OF DATA TEST WANTED
SR07 = 1		TYPE OF DATA TEST WANTED
SR08 = 1		SIX BIT WORD LENGTH
SR09 = 1		SEVEN BIT WORD LENGTH
SR10 = 1		EIGHT BIT WORD LENGTH
SR11 = 1		NINE BIT WORD LENGTH

MAINDEC-8L-D0AB-D

8L MEMORY PROTECT TEST

ABSTRACT

THIS PROGRAM TESTS THE BASIC OPERATION OF THE MEMORY PROTECT HARDWARE
OF THE PDP-8/L COMPUTER BY ATTEMPTING TO ACCESS MEMORY LOCATIONS ON
THE LAST PAGE OF COMPUTER MEMORY. ACCESS BY THE INSTRUCTIONS
ISZ Y, DCA Y AND JMS Y TO THE LAST PAGE OF MEMORY IS ILLEGAL IF THE
PROTECT SWITCH IS SET TO 1.

REQUIREMENTS

PDP-8/L

STORAGE = PROGRAM OCCUPIES LOCATIONS 0202 TO 0261 AND LOCATIONS 7600,
7601 AND 7777.

LOADING - BINARY LOADER WITH THE PROTECT SWITCH SET TO 0.

STARTING PROCEDURE
WITH THE PROTECT SWITCH SET TO 0, START THE COMPUTER AT 0202. IT SHOULD STOP AT LOCATION 0000 WITH THE FOLLOWING INDICATIONS:
MA=0000, MB=7402, AC=0002, FETCH, OPR.

WITH THE PROTECT SWITCH STILL SET TO 0, START THE COMPUTER AT 0230. IT SHOULD STOP AT LOCATION 0252 WITH THE FOLLOWING INDICATIONS:
MA=0252, MB=7402, AC=0000, FETCH, OPR.

WITH THE PROTECT SWITCH SET TO 1, START THE COMPUTER AT LOCATION 0202. IT SHOULD "HANG" AT LOCATION 0214 WITH THE FOLLOWING INDICATIONS:
MA=7777, MB=???? (UNIMPORTANT), AC=0000, EXECUTE, DCA, PROT.

WITH THE PROTECT SWITCH SET TO 1, DEPRESS CONTINUE. COMPUTER SHOULD "HANG" AT LOCATION 0220 WITH THE FOLLOWING INDICATIONS:
MA=7777, MB=????, AC=0001, EXECUTE, ISZ, PROT.

WITH THE PROTECT SWITCH SET TO 1, DEPRESS CONTINUE. COMPUTER SHOULD "HANG" AT LOCATION 0227 WITH THE FOLLOWING INDICATIONS:
MA=7777, MB=????, AC=0002, EXECUTE, JMS, PROT.

WITH THE PROTECT SWITCH SET TO 1, DEPRESS CONTINUE. COMPUTER SHOULD HALT AT LOCATION 0252 WITH THE FOLLOWING INDICATIONS:
MA=0252, MB=7402, AC=0000, FETCH, OPR.

PRINTOUTS - NO

SWITCH REGISTER OPTIONS - NO

MAINDEC-8L-D1GC-D

PDP-8/L EXTENDED MEMORY CONTROL TEST

ABSTRACT
THIS PROGRAM TESTS THE EXTENDED MEMORY CONTROL LOGIC FOR PROPER OPERATION. IT IS DESIGNED FOR USE WITH A PDP-8/L EQUIPPED WITH 8192 WORDS OF CORE MEMORY. THE PROGRAM EXERCISES AND TESTS THE CONTROL IOT'S; THE ABILITY TO REFERENCE FIELD 1 FROM FIELD 0; PROGRAM INTERRUPT AND INTERRUPT INHIBIT AND AUTO-INDEXING IN FIELD 1.

ERRORS ENCOUNTERED DURING RUNNING WILL RESULT IN A PROGRAM HALT. THE HALT LOCATIONS ARE LABELED, AND THE ERROR MAY BE IDENTIFIED BY REFERENCING THE PROGRAM LISTING OR TABLE OF ERROR HALTS.

REQUIREMENTS
PDP-8/L EQUIPPED WITH 8K OF MEMORY, EXTENDED MEMORY CONTROL.

STORAGE - PROGRAM RESIDES IN FIELD 0, AND REQUIRES 1200 (OCTAL) LOCATIONS.

LOADING - BINARY LOADER

STARTING PROCEDURE
LOAD ADDRESS 0200
PRESS START

PRINTOUTS - YES - ERRORS

SWITCH REGISTER OPTIONS - NO

MAINDEC-8L-D1HA-D

PDP-8/L EXTENDED MEMORY CONTROL TEST (12K)

ABSTRACT

THIS PROGRAM TESTS THE EXTENDED MEMORY CONTROL LOGIC FOR PROPER OPERATION. IT MAY BE USED WITH A PDP-8/L WITH UP TO 8K OF EXTENDED MEMORY. THE PROGRAM EXERCISES AND TESTS THE CONTROL IOTS; THE ABILITY TO REFERENCE ALL FIELDS FROM FIELD Ø; PROGRAM INTERRUPT AND INTERRUPT INHIBIT; AUTO-INDEXING IN EACH FIELD; AND A SPECIAL TEST FOR THE PDP-8/I WHICH TESTS THE PRESENCE OF A FALSE MEMORY PULSE WHEN A NON-EXISTENT MEMORY FIELD IS REFERENCED.

ERRORS ENCOUNTERED DURING RUNNING WILL RESULT IN A PROGRAM HALT. THE HALT LOCATIONS ARE LABELED, AND THE ERROR MAY BE IDENTIFIED BY REFERENCING THE PROGRAM LISTING OR TABLE OF ERROR HALTS.

REQUIREMENTS

PDP-8/L EXTENDED MEMORY CONTROL, AT LEAST 4K OF EXTENDED MEMORY.

STORAGE - THE PROGRAM REQUIRES 1726(8) LOCATIONS OF CODE MEMORY, THE PROGRAM MUST RESIDE IN MEMORY FIELD Ø ONLY.

LOADING - BINARY LOADER

STARTING PROCEDURE

SET THE SWITCH REGISTER TO Ø2ØØ
PRESS LOAD ADDRESS
SET SR 8 TO A 1 IF PDP-8/I IS BEING USED, OTHERWISE, SET SR 8 TO A Ø
PLACE THE OCTAL NUMBER OF EXTENDED MEMORY FIELDS AVAILABLE
IN SR 9, 1Ø AND 11
PRESS START

PRINTOUTS - NO

SWITCH REGISTER OPTIONS - NO

MAINDEC-8L-D1JA-D

BM8/L EXTENDED MEMORY CONTROL TEST

ABSTRACT

THIS PROGRAM TESTS THE BM8/L EXTENDED MEMORY CONTROL LOGIC FOR PROPER OPERATION. IT MAY BE USED WITH A PDP-8/L EQUIPPED WITH A MINIMUM OF 4K OF EXTENDED MEMORY. THE PROGRAM EXERCISES AND TESTS THE CONTROL IOT'S; THE ABILITY TO RERENCE ALL FIELDS FROM Ø; PROGRAM INTERRUPT AND INTERRUPT INHIBIT; AUTO-INDEXING IN EACH FIELD; AND A SPECIAL TEST WHICH CHECKS THAT ONLY ZEROES ARE READ WHEN A NON-EXISTENT MEMORY FIELD IS REFERENCED.

ERRORS ENCOUNTERED DURING RUNNING WILL RESULT IN A PROGRAM HALT. THE HALT LOCATIONS ARE LABELED, AND THE ERROR MAY BE IDENTIFIED BY REFERENCING THE PROGRAM LISTING OR TABLE OF ERROR HALTS.

REQUIREMENTS
PDP-8/L
BM8/L EXTENDED MEMORY CONTROL
AT LEAST 4K OF EXTENDED MEMORY.

STORAGE - PROGRAM REQUIRES 2400(8) LOCATIONS OF CORE MEMORY.
PROGRAM MUST RESIDE IN MEMORY FIELD 0 ONLY.

LOADING - BINARY LOADER

STARTING PROCEDURE
SET THE SWITCH REGISTER TO 0200
PRESS LOAD ADDRESS
SET SR8 TO A 1 IF IT IS DESIRED TO INHIBIT THE NON-EXISTENT
MEMORY TEST
PLACE THE OCTAL NUMBER OF EXTENDED MEMORY FIELDS AVAILABLE
IN SR9, 10 AND 11
PRESS START

PRINTOUTS - NO

SWITCH REGISTER OPTIONS - NO

MAINDEC-8L-D5AA

PDP-8/L MEMORY PARITY IOT TEST

ABSTRACT
THE PDP-8/L MEMORY PARITY IOT TEST IS DESIGNED TO EXERCISE AND
DETECT ERRORS ON THE MEMORY PARITY CONTROL LOGIC. A ROUTINE
IS ALSO INCLUDED WHICH WRITES RANDOM NUMBERS IN MEMORY FIELD 0,
AND THEN CHECKS FOR DATA PARITY ERRORS.

MANUAL INTERVENTION AFTER THE START OF THE TEST IS REQUIRED IN
ORDER TO TEST THE PARITY IOT'S. PRINTED INSTRUCTIONS ARE GIVEN
ON THE TTY PRINTER.

REQUIREMENTS
A PDP-8/L MEMORY PARITY OPTION, KEYBOARD READER AND TELEPRINTER,
1 JUMPER WIRE

STORAGE - THE PROGRAM OCCUPIES LOCATIONS 0000 TO 0712 OCTAL,
AND TESTS LOCATIONS 1000 TO 7700 OCTAL.

LOADING - BINARY LOADER

STARTING PROCEDURE
SET THE SR TO 0200
PRESS LOAD ADDRESS, AND THEN START
THE PROGRAM RESPONDS WITH A PRINT-OUT SHOWN BELOW,
AND THEN A HALT

GROUND PIN S1 M115 A14 SET PARITY ERROR
PRESS CONTINUE

GROUNDING S1 SETS THE PARITY ERROR FLIP-FLOP SO THE PROGRAM
MAY TEST IOT 6101, AND PROGRAM INTERRUPT

IF NO ERROR HALTS, THE PRINT-OUT SHOWN BELOW OCCURS

FOLLOWED BY A HALT

UNGROUND PIN S1 M115 A14
GROUND PIN U1 M115 A14
PRESS START

AFTER GROUNDING PIN U1, SET THE SR TO 0226, PRESS LOAD ADDRESS, AND THEN START

GROUNDING PIN U1 HOLDS THE PARITY ERROR FLIP-FLOP IN THE CLEAR STATE SO THAT IOT 6101 MAY BE TESTED FOR CORRECT OPERATION

IF NO ERROR HALTS, THE PRINT-OUT SHOWN BELOW OCCURS FOLLOWED BY A HALT

MOMENTARILY GROUND PIN S1 M115 A14
PRESS CONTINUE

REMOVE THE WIRE FROM PIN U1 AND TOUCH IT TO PIN S1 TO SET THE PARITY ERROR FLIP-FLOP. THE CLEAR PARITY ERROR IOT IS THEN TESTED

IF NO ERROR HALTS, TESTS T6 AND T7 ARE THEN PERFORMED, TEST T7 WILL LOOP UNTIL STOPPED BY THE OPERATOR

PRINTOUTS = YES

SWITCH REGISTER OPTIONS = NO

MAINDEC-8-D2B

PDP-8 LT08 TELEPRINTER TEST

ABSTRACT

THE LT08 TELEPRINTER TEST VERIFIES CORRECT OPERATION OF THE LT08 CONTROL LINE HAREWARE AND ANY CONFIGURATION OF FROM ONE TO FIVE TELEPRINTERS. HARDWARE MALFUNCTIONS DETECTED BY THE PROGRAM RESULT IN A PROCESSOR HALT. THE TEST INCLUDES A CONCURRENT OUTPUT ROUTINE, A CONCURRENT INPUT ROUTINE, AN OUTPUT SCOPE LOOP, AND A WRU TEST THAT VERIFIES THAT NONE OF THE TELEPRINTERS ASSOCIATED WITH THE LT08 RESPOND TO A WRU (WHO ARE YOU) CODE.

REQUIREMENTS

MINIMUM CONFIGURATION PDP-8
LT08 CONTROL LINE HARDWARE
1 TO 5 ASCII TELEPRINTERS

STORAGE = PROGRAM OCCUPIES MEMORY FROM ADDRESS 0 TO 1053

LOADING = BINARY LOADER

STARTING PROCEDURE

SET THE SWITCH REGISTER TO 0200
PRESS LOAD ADDRESS,
SET SWITCH REGISTER BITS 1 TO 5 TO SELECT LINES TO BE RUN
PRESS START,
THE PROGRAM OUTPUTS A FIXED MESSAGE ON ALL LINES SELECTED,

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - NO.

MAINDEC-T8-D8AA-D(L)

TIME SHARING 8 OPTION TEST KT8

ABSTRACT
THIS IS A TEST OF THE TIME SHARING OPTION, AND IS BASED
UPON SWITCHING BETWEEN THE EXECUTIVE AND USER MODES TESTING
ALL "TRAPABLE" INSTRUCTIONS.

REQUIREMENTS
PDP-8 STANDARD COMPUTER
TIME SHARING OPTION
DF 32 DISK

STORAGE - THE PROGRAM USES CORE 0 TO 1000.

LOADING - BINARY LOADER.

STARTING PROCEDURE
SET SWITCH REGISTER TO 200
LOAD ADDRESS
PRESS START
THE PROGRAM SHOULD HALT A PC211 AND PC 217, PRESS CONTINUE
IN EACH CASE. THE PROGRAM WILL THEN RUN FOR ABOUT 5 MINUTES
AND COME TO A REST (JUMP TO SELF) AT PC 100.

PRINTOUTS - NO

SWITCH REGISTER OPTIONS - NO

MAINDEC-T8-D8BB-D

TIME SHARE-8 HARDWARE EXERCISER KT8

ABSTRACT
TIME SHARE-8 HARDWARE EXERCISER IS A PROGRAM WRITTEN TO ASSURE THAT
THE HARDWARE CAN FUNCTION PROPERLY BOTH IN AND OUT OF TIME SHARE
MODE WITH DATA BREAK DEVICES RUNNING. IT DOES THIS BY EXERCISING
SEVERAL DATA BREAK DEVICES SIMULTANEOUSLY (IF AVAILABLE) AND RUNNING
A PROGRAM IN TIME SHARE MODE.

REQUIREMENTS
FAMILY-OF-8 COMPUTER WITH TIME SHARE OPTION AND EXTENDED MEMORY
DM01 DATA BREAK MULTIPLEXER PLUS AT LEAST ONE OF THE FOLLOWING
TC01 DECTAPE AND/OR DF32 DISK OR RF08 DISK

STORAGE - THE PROGRAM OCCUPIES ALL OF THE LOWEST 4K OF MEMORY OF THE
COMPUTER AND USES SOME OF THIS AREA AND AREAS IN OTHER MEMORY
BANKS FOR DATA STORAGE.

LOADING = BINARY LOADER

STARTING PROCEDURE
SET SWITCH REGISTER TO 00200,
DEPRESS LOAD ADDRESS,
SET SWITCH REGISTER TO 0000,
DEPRESS START,
ANSWER QUESTIONS ASKED BY PROGRAM WITH "Y" FOR YES, "N" FOR NO,
AND NUMBER OF EXTRA MEMORY BANKS (BETWEEN 1 AND 7),
AFTER INTERROGATION IS COMPLETE, PROGRAM WILL START EXERCISING
THE DEVICES WHOSE ANSWERS ARE "YES" AND THE TIME SHARE HARDWARE.

PRINTOUTS = YES

SWITCH REGISTER OPTIONS = YES,

AC SWITCH	SET AS	ACTION ON PROGRAM
0	1	DON'T HALT ON HARDWARE ERRORS
	0	HALT ON HARDWARE ERRORS
1	1	DON'T HALT ON DATA ERRORS
	0	HALT ON DATA ERRORS
2	1	DON'T PRINT HARDWARE ERRORS
	0	PRINT HARDWARE ERRORS
3	1	DON'T PRINT DATA ERRORS
	0	PRINT DATA ERRORS
4	1	LOOK AT AC5 FOR DISK TRANSFER DIRECTION
	0	IGNORE AC5
5	1	WRITE
	0	READ
6	1	SUPPRESS DECTAPE EXERCISING
	0	NONE
7	1	
	0	
8	1	SUPPRESS DISK EXERCISING
	0	NONE
9	1	
	0	
10	1	
	0	
11	1	FREEZE MEMORY FIELD
	0	NONE

MAINDEC-12-D8FB-D

DC02-F OPTION TEST

ABSTRACT
DC02-F IS A MODEM INTERFACE CONTROL, USED WITH THE FAMILY OF 8
COMPUTER SERIES, TO CONTROL TTY'S, TTY COMPATABLE DISPLAYS, ETC,
DC02-F OPTION TEST IS DESIGNED TO TEST THE CONTROL AND TTY LINES,
THE TEST CONSISTS OF THREE SECTIONS THE FIRST CHECKS THE
INTERFACE OPERATION INDEPENDENT OF EXTERNAL DEVICES WHILE THE
SECOND SECTION USES TTY'S FOR CHECKOUT, THE THIRD IS DESIGN FOR
THE KSR <NC READER-PUNCH> TTY OR A DISPLAY TERMINAL.

REQUIREMENTS
STANDARD PDP-8 COMPUTER WITH ASR-33 OR EQUIVALENT,
DC02-F OPTION

FROM 1 TO 32 TELETYPES WITH READER AND PUNCH OR 1 TO 32
M850 MODULE SETS.

STORAGE - THIS PROGRAM OCCUPIES MEMORY LOCATIONS 0 THRU 4400

LOADING - BINARY LOADER

STARTING PROCEDURES
SET SWITCH REGISTER TO 0200
PRESS LOAD ADDRESS
SET SWITCH REGISTER TO 00XX
XX=
BIT06=0 - CONTROL TEST ONLY
=1 - CONTROL TEST AND M850
DATA TEST
BIT 2-11- CONTAIN NUMBER OF
DC02-G'S INSTALLED.
PRESS START

PRINTOUTS - NO

SWITCH REGISTER OPTIONS - NO.

MAINDEC-12-D0MC-D

FPP-12 INSTRUCTION TEST 2A

ABSTRACT
FPP-12 INSTRUCTION TEST 2A IS DESIGNED TO TEST ALL FPP IOTS, FORCE AND TEST ALL STATUS CONDITIONS, TEST ALL COMMAND REGISTER FUNCTIONS AND EXECUTE ALL NON-MEMORY ALTERING INSTRUCTIONS ON SELECTED DATA PATTERNS. THIS PROGRAM REQUIRES NO TELETYPE COMMUNICATIONS AS ERROR HALTS ARE USED EXCLUSIVELY. THE ASSUMPTION IS MADE THAT THE PDP-8 OR PDP-12 USED IN CONJUNCTION WITH THE FPP IS A SOLID, ERROR FREE MACHINE.

REQUIREMENTS
A FPP-12 FLOATING POINT PROCESSOR
A STANDARD BASIC PDP-8 OR PDP-12
AN ASR-33 TELETYPE OR EQUIVALENT

STORAGE - THIS PROGRAM IS DESIGNED TO RUN IN MEMORY BANK 0 AND IT OCCUPIES VIRTUALLY ALL BANK 0 NOT OCCUPIED BY THE BINARY AND RIM LOADERS.

LOADING - BINARY LOADER

STARTING PROCEDURE - FOR 8 FAMILY PROCESSOR
SET SWITCH REGISTER TO 0020
PRESS LOAD ADDRESS.
SET SWITCH REGISTER TO 0001 IF USING PDP-8/I
OTHERWISE SET=0000
PRESS START

PRINTOUTS - NO

SWITCH REGISTER OPTIONS - NO.

MAINDEC-12-D0NB-D

FPP-12 INSTRUCTION TEST 2B

ABSTRACT

FPP-12 INSTRUCTION TEST 2B IS DESIGNED TO TEST ALL FPP JUMP INSTRUCTIONS. AT THE START OF THE TEST THE USER IS GIVEN THE OPTION OF SELECTING ONE OF TWO POSSIBLE MODES OF OPERATION:

A. RANDOM MODE WHERE THE ADDRESS JUMPED TO IS GENERATED RANDOMLY OUTSIDE THE AREA OF CORE OCCUPIED BY THE PROGRAM.

B. NON-RANDOM MODE WHERE THE ADDRESS JUMPED TO IS SELECT VIA THE SWITCH REGISTER AT THE OPERATORS DISCRETION. THE SPECIFIED ADDRESS IS TESTED TO DETERMINE IF IT IS A LEGAL ADDRESS OUTSIDE THE AREA OF CORE OCCUPIED BY THE PROGRAM.

ALL JUMP INSTRUCTIONS FOR THE FPP ARE TESTED IN A SIMILAR MANNER.

REQUIREMENTS

A FPP-12 FLOATING POINT PROCESSOR
A STANDARD BASIC PDP-8 OR PDP-12
AN ASR-33 TELETYPE OR EQUIVALENT

STORAGE - THIS PROGRAM IS DESIGNED TO RUN IN MEMORY BANK 0 AND MAY CLEAR OR USE ALL OF MEMORY NOT OCCUPIED BY THE PROGRAM.

LOADING - BINARY LOADER

STARTING PROCEDURE - 8 FAMILY PROCESSOR

SET SWITCH REGISTER TO 0020.
PRESS LOAD ADDRESS
IF PROCESSOR IS PDP-8/I SET SWITCH
REGISTER TO 0001 OTHERWISE
SET TO 0000.
PRESS START.

PRINTOUTS - NO

SWITCH REGISTER OPTIONS - YES

SR0=0 RANDOM MODE
SR0=1 NON-RANDOM MODE.

MAINDEC-12-D0DB-D

FPP-12 INSTRUCTION TEST 2C

ABSTRACT

THIS PROGRAM CHECKS THE FOLLOWING INSTRUCTIONS IN THE FPP-12 (THE PDP-12 FLOATING POINT PROCESSOR OPTION).

LDX LOAD INDEX REGISTER
ADDX ADD TO INDEX REGISTER
FSTA STORE FAC
ATX ACCUMULATOR TO INDEX REGISTER

```
        FADDM   ADD TO MEMORY
        FMULM   MULTIPLY TO MEMORY
        NOP     14 INSTRUCTIONS THAT PERFORM NO OPERATION

        THIS PROGRAM HALTS ON ERRORS AND USES NO TTY COMMUNICATIONS.

        THE WORD "FREE" IS DEFINED IN THE PROGRAM AS A NOP (7000).  THIS
        INSTRUCTION WAS PUT IN SEVERAL LOCATIONS IN THE PROGRAM TO MAKE
        AVAILABLE MEMORY LOCATIONS FOR THE USER TO MODIFY THE PROGRAM FOR
        SCOPE OR TEST LOOPS AT HIS OPTION,  IT IS ASSUMED THAT THE BASIC
        PDP-8 OR PDP-12 PROCESSOR AND MEMORY HAVE BEEN CHECKED AND ARE
        FULLY OPERATIONAL.

REQUIREMENTS
        AN FPP-12 FLOATING POINT PROCESSOR
        A BASIC PDP-8 OR PDP-12 WITH 4K OF CORE MEMORY
        AN INPUT DEVICE FOR LOADING THE PROGRAM

STORAGE - THIS PROGRAM OCCUPIES LOCATIONS 0000 THROUGH 6477 OF FIELD 0

LOADING - BINARY LOADER

STARTING PROCEDURE
        PDP-8/I SET SWITCH REGISTER = 0200
                PRESS LOAD ADDRESS
                SET SWITCH REGISTER = 0000
                PRESS START

        PDP-8/E SET SWITCH REGISTER = 0200
                PRESS LOAD ADDRESS
                SET SWITCH REGISTER = 0000
                PRESS CLEAR
                PRESS CONTINUE

PRINTOUTS - NO

SWITCH REGISTER OPTIONS - YES
        SR00=0  RUN CONTINUOUSLY
        SR00=1  STOP AT END OF PASS



MAINDEC-12-D0PC-D

FPP-12 ADDRESS TEST

ABSTRACT
        THIS PROGRAM IS DESIGNED TO DETECT A FAULT IN THE FPP-12
        MEMORY ADDRESSING HARDWARE, ALL OF AVAILABLE MEMORY IF FIRST
        SET TO 0707 OR 7070,  AT THE START OF EACH PASS THE MEMORY
        CONSTANT IS COMPLIMENTED,  THE FPP-12 THEN STORES ONE 36 BIT
        WORD INTO 3 CONSECUTIVE CORE LOCATIONS,  THE FPP READS BACK THIS
        36 BIT WORD AND STORES IT INTO THE BASE TABLE THEN GOES INTO
        PAUSE,  THIS ALLOWS THE OPERATION OF BOTH THE LOAD AND STORE
        FUNCTIONS TO BE CHECKED.  WHILE THE FPP-12 IS IN PAUSE, THE
        PDP CHECKS BOTH 36 BIT WORDS (THE WORD AT THE MEMORY ADDRESS
        AND THE WORD IN THE BASE TABLE.)  AT THE OPERATORS OPTION THE PDP WILL
        THEN CHECK ALL UNUSED MEMORY TO SEE THAT NOTHING HAS CHANGED
        THE PDP THEN CLEARS THE FPP WORD AT THE MEMORY ADDRESS AND
        INCREMENTS THE ADDRESS BY 1 MEMORY LOCATION AND REPEATS THE
```

PROCESS, WHEN ALL OF MEMORY IS CHECKED EXCEPT THE LOCATIONS OCCUPIED BY THE PROGRAM, AT THE OPERATORS OPTION, THE PROGRAM WILL RELOCATE ITSELF TO THE NEXT FIELD.

REQUIREMENTS
AN FPP-12 FLOATING POINT PROCESSOR
A PDP-8 OR PDP-12 WITH AT LEAST 4K OF MEMORY
AN ASR33 OR ASR35 TELETYPE

STORAGE - THE PROGRAM IS LOADED INTO LOCATIONS 0000-2577 OF FIELD 0. THE PROGRAM USES ALL LOCATIONS OF EVERY FIELD TESTED.

LOADING - BINARY LOADER

STARTING PROCEDURE
SET SWITCH REGISTER TO 0020
PRESS LOAD ADDRESS
CLEAR SWITCH REGISTER
PRESS START, PROGRAM WILL HALT.
SET SR09-11 TO HIGHEST MEMORY FIELD, TO BE TESTED.
PRESS CONTINUE, PROGRAM WILL HALT.
SET SWITCH REGISTER TO 0000
PRESS CONTINUE

PRINTOUTS - NO

SWITCH REGISTER OPTIONS - YES

SWITCH	STATE	REF.	OPERATION
00	0	9.3	HALT ON ERRORS
	1		BYPASS ERROR HALT
01	0	9.1	TYPE ERRORS
	1		BYPASS ERROR TYPEOUT
02	0	9.4	CONTINUE TEST AFTER AN ERROR
	1		LOOP ON ERROR
03	0	6.3	RELOCATE THE PROGRAM TO THE NEXT FIELD
	1		RUN THE PROGRAM IN THE SAME FIELD.
04	0	8.	TYPE END OF PASS INFORMATION
	1		SUPPRESS END OF PASS TYPEOUTS
05	0	8.	CONTINUE TO NEXT PASS
	1		HALT AT END OF A PASS
06	0	9.5	CONTINUE COMPARE AFTER AN ERROR
	1		START FPP AT THE NEXT ADDRESS AFTER AN ERROR
07	0	6.2	CHECK FPP DATA ONLY (NORMAL MODE)
	1		CHECK ALL OF MEMORY (COMPLETE MODE)
08	0	6.2	CHECK ALL OF MEMORY AFTER AN FPP DATA ERROR
	1		CHECK SR07
09	0	9.7	OUTPUT ERROR INFO TO THE TTY
	1		OUTPUT ERROR INFO TO THE LINE PRINTER

///

10	0	NONE	UNUSED
	1		UNUSED
11	0	9.6	OUTPUT COMPLETE ERROR INFORMATION
	1		OUTPUT SHORT FORM ERRORS

MAINDEC-12-D2AA-D (P)

VT06 (DATAPOINT 3300)

ABSTRACT

THE VT06 (DATAPOINT 3300) IS A TELETYPE COMPATABLE VIDEO DISPLAY TERMINAL CAPABLE OF BAUD RATES UP TO 2400 BAUD, THE VT06 ALSO HAS SEVERAL SPECIAL COMMAND CODES FOR THE ERASING OF THE DISPLAY SCREEN AND MOVEMENT OF THE CURSOR (BLINKING REFERENCE POINT). THE VT06 PROGRAM IS DESIGNED TO PROVEDE FLEXABLE USES OF INTERFACING LOGICS (IE DC02, PT08F). THE PROGRAM IS COMPLETELY WRITTEN IN PDP-8 LANGUAGE TO INSURE MACHINE COMPATIBILITY. THE VT06 PROGRAM IS DESIGNED TO EXERCISE THE VT06 AND NOT THE INTERFACING LOGIC. PARTS OF THIS PROGRAM WILL ONLY EXERCISE 1 VT06 AT A TIME.

REQUIREMENTS

STANDARD PDP-8, 8/I, 8/L, 12 COMPUTER WITH A ASR-33
CONSOLE TELETYPE,
VT06 (DATAPOINT 3300) DISPLAY TERMINAL,
MODEM INTERFACE CONTROL LOGIC (DC02, PT08F).

STORAGE - THIS PROGRAM OCCUPIES 0 THROUGH 3577 MEMORY LOCATIONS.

LOADING - BINARY LOADER

STARTING PROCEDURE

LOAD AND START 0200, THE COMPUTER WILL HALT, PLACE THE RECEIVER DEVICE CODE IN RSW(SR) 6-11, DEPRESS CONT. THE COMPUTER WILL HALT AGAIN, NOW PLACE THE TRANSMITTED (VT06 TO THE COMPUTER) BAUD RATE VALUE EQUIVALENT IN RSW(SR) 10-11, (IE, 0=110-150-300 BAUD, 1=600 BAUD, 2=1200 BAUD, 3=2400 BAUD) THIS IS USED IN RELATION TO THE NUMBER OF "FILLER" CHARACTERS AND MUST ALWAYS BE CORRECT FOR ALL ROUTINES, FAILURE TO DO THIS WILL AT HIGHER BAUD RATES CAUSE FAILURES. THE COMPUTER WILL HALT AGAIN TO ALLOW THE OPERATOR TO SELECT THE DESIRED SWITCH OPTIONS; SELECT THE OPTIONS AND DEPRESS CONTINUE.

STARTING ADDRESS

0200	CHARACTER OUTPUT ROUTINES
0201	OCTAL CONVERSION ROUTINE
0202	ECHO ROUTINE FROM THE VT06 KEYBOARD TO THE SCREEN AND THE CONSOLE PRINTER
0203	ECHO ROUTINE FROM THE CONSOLE KEYBOARD TO THE CONSOLE PRINTER AND THE VT06 SCREEN
0204	FOCUS ADJUSTMENT ROUTINE
0205	OUTPUT TO THE VT06 SCREEN 1 CHARACTER (ASCII CODE IN BITS 4-11 OF LOCATION 0102)

```
        0206    MARGIN OUTPUT ROUTINE
        0207    ECHO ROUTINE USING ALL DC02 INTERFACE LINES
                (REF. 6.)
        0210    OCTAL CONVERSIONS USING ALL DC02 INTERFACE LINES
                (REF. 6.)

PRINTOUTS = NO

SWITCH REGISTER OPTIONS = YES

        (SR) 0=1        INHIBIT THE DELAY (15 SECONDS BETWEEN EACH ROUTINE)
        (SR) 1=1        REMAIN IN THE CURRENT TEST
        (SR) 2=0        SELECT ONLY ONE DC02 LINE.  USABLE FOR ALL
                        STARTING ADDRESSES (REF. 4.2)
        (SR) 2=1        SELECT ALL DC02 LINES, USABLE ONLY FOR STARTING
                        ADDRESSES (REF. 4.2, 6.)  200,204,205 AND 206.
        (SR) 9-11       SET TO THE LINE NUMBER (IF
                        BEING TESTED THROUGH A DC02)


MAINDEC-8I-D01C-D

INSTRUCTION TEST 1

ABSTRACT
        THIS IS A DIAGNOSTIC PROGRAM FOR TESTING THE AND, TAD, AND OPERATE
        INSTRUCTIONS OF THE PDP-8/I ONLY.

REQUIREMENTS
        A PDP-8/I EQUIPPED WITH TELETYPE

STORAGE = PROGRAM USES LOCATIONS 0000-4421.

LOADING = BINARY LOADER

EXECUTION TIME = 256 LOOPS/SECOND

STARTING PROCEDURE
```

SET SR TO 144 AND PRESS LOAD ADDRESS
SET SR TO 7777 AND PUSH START
PROGRAM WILL HALT. MA=146
IF AC=0000 AN ERROR HAS OCCURRED
PUSH CONTINUE. PROGRAM WILL RUN UNTIL STOPPED OR
UNTIL AN ERROR IS ENCOUNTERED

PRINTOUTS = NO

SWITCH REGISTER OPTIONS = NO

MAINDEC-8I-D02B-D

INSTRUCTION TEST 2

ABSTRACT
THIS PROGRAM IS AN EXTENSIVE TEST OF AUTOINDEXING, INDIRECT ADDRESSING, AND THE DCA INSTRUCTION FOR THE PDP-8/I. IT ALSO OFFERS MINIMAL TESTING FOR INTERRUPT AND THE AND, TAD, ISZ, JMP AND JMS INSTRUCTIONS.

REQUIREMENTS
PDP-8/I, 8/S EQUIPPED WITH TELETYPE

STORAGE = PROGRAM OCCUPIES MEMORY LOCATIONS 0000-4021

LOADING = BINARY LOADER

EXECUTION TIME = FIVE PROGRAM LOOPS PER SECOND.

STARTING PROCEDURE
SET THE SWITCH REGISTER TO 201;
PRESS LOAD ADDRESS.
PUSH START;

PRINTOUTS = NO

SWITCH REGISTER OPTIONS = NO

MAINDEC-8I-D0AA-D

PDP-8/I INSTRUCTION TEST-PART 3A

ABSTRACT
THIS PROGRAM IS A TEST OF THE EXTENDED ARITHMETIC ELEMENT, THE FOLLOWING INSTRUCTIONS ARE TESTED: MQL, MQA, SHL, LSR, ASR, NMI, SCA, SCL.

AN ATTEMPT IS MADE TO DETECT AND ISOLATE ERRORS TO ITS MOST BASIC FAULT AND TO THE MINIMUM NUMBER OF LOGIC CARDS. MULTIPLY AND DIVIDE ARE TESTED MAINDEC 8I-3B.

REQUIREMENTS
PDP-8/I, EAE, KEYBOARD READER AND TELEPRINTER

LOADING = BINARY LOADER

EXECUTION TIME - 35 SECONDS

STARTING PROCEDURES
SET 0200(8) IN THE SWITCH REGISTER KEYS AND PRESS THE LOAD ADDRESS KEY. SET 5000(8) IN THE SWITCH REGISTER KEYS AND PRESS THE START KEY.

PRINTOUTS - YES, ON ERROR

SWITCH REGISTER OPTIONS - NO

MAINDEC-8I-D0BA-D

EXTENDED ARITHMETIC PDP-8/I INSTRUCTION TEST PART 3_B

ABSTRACT
THE PDP-8/I EAE (KE-8/I) MULTIPLY-DIVIDE TEST TESTS AND EXERCISES THE MULTIPLY AND DIVIDE HARDWARE OF THE KE-8/I OPTION. FIXED NUMBERS WITH PREDETERMINED SOLUTIONS, AND RANDOM NUMBERS WITH SIMULATED SOLUTIONS ARE USED. ABILITY TO OPERATE WITH INTERRUPT ENABLED IS ALSO TESTED.

REQUIREMENTS
PDP-8/I PROCESSOR KE-8/I OPTION, AND ASR 33/35 TELETYPE ARE REQUIRED.

STORAGE - LOCATIONS 0000 THROUGH 7570 ARE USED.

LOADING - BINARY LOADER

EXECUTION TIME - 7 MINUTES PER COMPLETE PASS.

STARTING PROCEDURE
IF INTERRUPT INTERACTION IS TO BE TESTED, LOAD ANY TAPE IN TAPE READER AND TURN IT ON. LOAD ADDRESS 0200, PRESS START. PROGRAM HALTS AT LOC 0200. SET ANY DESIRED OPTIONS IN SR AND PRESS CONTINUE. THE PROGRAM WILL HALT AT PROGRAM END HALT (LOC 0256) AFTER LAST ROUTINE HAS BEEN EXECUTED, PROVIDED NO LOOP OPTIONS HAVE BEEN SET.

PRINTOUTS - YES, ON ERROR

SWITCH REGISTER OPTIONS - YES

SR0	HALT AFTER CURRENT ROUTINE. PROGRAM HALTS AT COMPLETION OF CURRENT TEST ROUTINE. THE AC DISPLAYS NUMBER OF COMPLETED ROUTINE.
SR1	SELECT ROUTINE THE PROGRAM JUMPS TO ROUTINE WHOSE NUMBER IS SET IN SR9 THROUGH SR11. ROUTINE SELECTION OCCURS AT START OF PROGRAM, OR AT COMPLETION OF CURRENT ROUTINE.
SR2	LOOP ROUTINE. CURRENT ROUTINE IS REPEATED.
SR3	LOOP PROGRAM. ENTIRE PROGRAM IS REPEATED.
SR4	LOCK ON TEST. THE TEST CURRENTLY BEING EXECUTED IS REPEATED.
SR5=0	PRINT ON ERROR.
SR5=1	HALT ON ERROR.
SR6	HALT AFTER PRINT. PROGRAM HALTS AFTER ERROR PRINTOUT
SR7	PRINT FAILURE RATE. THE PROGRAM PRINTS THE NUMBER OF FAILURES PER HUNDRED REPETITIONS OF SAME TEST. PROGRAM

HALTS AFTER THE PRINTOUT SR5 MUST BE SET TO 0 FOR THE PRINTOUT TO OCCUR.

SR8 — PRINT SIMULATION AND/OR ENTER SCOPE LOOP. FOR ROUTINES 0 AND 1 PROGRAM PRINTS MULTIPLY SIMULATION AND ENTERS MULTIPLY SCOPE LOOP. FOR ROUTINES 2 AND 3 PROGRAM PRINTS DIVIDE SIMULATION AND ENTERS DIVIDE SCOPE LOOP. FOR ROUTINES 4 THROUGH 7 PROGRAM ENTERS THE EXERCISER SCOPE LOOP FOR INDIVIDUAL ROUTINE. SR5 MUST BE SET TO 0 FOR THIS OPTION TO BECOME ACTIVE.

SR9 THROUGH SR11 — ROUTINE NUMBER. THESE SWITCHES SPECIFY THE NUMBER OF ROUTINE TO BE SELECTED. SR1 MUST BE ON TO SELECT A ROUTINE.

MAINDEC-8I-D2AC

LP08 LINE PRINTER TEST

ABSTRACT

THE LP08 LINE PRINTER DIAGNOSTIC TEST PROGRAM IS DESIGNED TO PROVIDE A THOROUGH CHECK-OUT OF THE PRINTER CONTROL INTERFACE ELECTRONICS AS WELL AS THE ELECTRONIC AND MECHANICAL PORTIONS OF THE LINE PRINTER MECHANISM ITSELF. THE PROGRAM CONSISTS OF A SERIES OF SEVEN (7) TESTS AND DRIVE ROUTINES, EACH OF WHICH CAN BE SELECTED AND OPERATED INDEPENDENTLY OF THE OTHERS USING THE ACCUMULATOR SWITCHES. INTERNALLY DETECTED ERROR CONDITIONS ARE DISPLAYED ON THE TELEPRINTER WHILE DETAILED DESCRIPTIONS OF EACH ERROR AND WHAT WAS HAPPENING AT THE TIME THE ERROR OCCURRED, IS PRESENTED ON THE ERROR TABLES CORRESPONDING TO EACH OF THE TESTS. PRINT PATTERNS USED IN THESE TESTS HAVE BEEN CHOSEN FOR EASE OF VISUAL VERIFICATION.

THE FIRST TEST(TEST 1) IS COMPOSED OF FOUR SEGMENTS DESIGNED TO CHECK-OUT THE PROCESSOR INTERFACE CONTROL ELECTRONICS AND INTERCOMMUNICATIONS DATA PATHS, TEST 2, 3, AND 4 USE WORST CASE PATTERNS TO TEST PRINTER PERFORMANCE AND ENDURANCE WHILE TESTS 5 AND 6 PROVIDE DRIVE FOR PRINTER HAMMER ALIGNMENT AND INTENSITY ADJUSTMENT PROCEDURES AND A TEST OF THE PAPER SLEW AND CLUTCH OPERATIONS.

TEST 7 CONSISTS OF SEVERAL SUB-TESTS AND MAINTENANCE AIDS AMONG THEM A SCOPE DRIVE TEST, HAMMER POWER SUPPLY TEST, AND A PRINT SINGLE SEGMENTS DRIVE, ALSO INCLUDED AS ADDITIONAL ROUTINES ARE A PRINTER SPEED TEST, AND A RIBBON TEST.

REQUIREMENTS

PDP-8 PROCESSOR
TELETYPE MODEL 33 ASCII KEYBOARD PRINTER
DATA PRODUCTS, MODEL 2310, LINE PRINTER
PDP-8 LINE PRINTER CONTROL UNIT

STORAGE - PROGRAM OCCUPIES AND USES MEMORY FROM 10 TO 6500.

LOADING - BINARY LOADER

STARTING PROCEDURE

ENSURE LINE PRINTER HAS BEEN POWERED DOWN
START AT 0200
RESTART AT 0201
ADDRESS 0202 - PRINT SPEED TEST
0203 - RIBBON TEST

PRINTOUTS - YES
SWITCH REGISTER SETTINGS - YES

MAINDEC-8I-D2BA

OPTICAL MARK CARD READER TEST

ABSTRACT
THE PROGRAM TESTS THE OPTICAL MARK CARD READER FOR CORRECT ALPHA-NUMERIC AND BINARY OPERATIONS, IT ALSO TESTS CONTROL INTERRUPT ANC TIMING.

REQUIREMENTS
PDP-8 OR 8/I WITH OPTICAL MARK G.D.I. 100MS CARD READER
OPTICAL MARK ALPHA-NUMERIC CARD DECK (MAINDEC-89-D2B1-C)
OPTICAL MARK BINARY CARD DECK (MAINDEC-89-D2B2-C)
OPTICAL MARK SENSE CARD DECK (MAINDEC-89-D2B3-C)

LOADING - BINARY LOADER

STARTING PROCEDURE
TURN ON CARD READER POWER, AT THIS POINT THE ONLY RED LIGHT TO BE ON SHOULD BE CARD SUPPLY. REFERENCE G.D.I. MANUAL TO REMEDY OTHER RED LIGHT ERROR CONDITIONS. LOAD ADDRESS 204(8)
DEPRESS START, PROGRAM WILL PRINT "IOTS OK" IF TEST RUNS, PROGRAM WILL HALT IF TEST FAILS, REFERENCE SYMBOLIC LISTING AND COMMENTS FOR APPROPRIATE ERROR DESCRIPTION.

OPTIONAL STARTING ADDRESSES
0200(8) = DATA TESTS (PDP-8 OR 8/I
0202(8) = MARK SENSE TEST (PDP-8 OR 8/I
0204(8) = STATIC IOT TESTS
0700(8) = SCOPE LOOP

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - NO

MAINDEC-8I-D4CA-D(L)

PDP-8/I MEMORY PARITY IOT TEST

ABSTRACT
THE PDP-8/I MEMORY PARITY IOT TEST IS DESIGNED TO EXERCISE AND DETECT ERRORS ON THE MEMORY PARITY CONTROL LOGIC. A ROUTINE IS ALSO INCLUDED WHICH WRITES RANDOM NUMBERS IN MEMORY FIELD 0, ANC THEN CHECKS FOR DATA PARITY ERRORS.

MANUAL INTERVENTION AFTER THE START OF THE TEST IS REQUIRED IN ORDER TO TEST THE PARITY IOT'S. PRINTED INSTRUCTIONS ARE GIVEN ON THE TTY PRINTER.

REQUIREMENTS
PDP-8/I, MEMORY PARITY OPTION, KEYBOARD READER AND TELEPRINTER, 1 JUMPER WIRE.
STORAGE - PROGRAM OCCUPIES LOCATIONS 0000 TO 0712

LOADING - RIM LOADER

STARTING PROCEDURE
SET THE SR TO 0200, PRESS LOAD ADDRESS, AND THEN START, THE

PROGRAM RESPONDS WITH A PRINT-OUT SHOWN BELOW, AND THEN A HALT.

GROUND PIN S1 M113 B09 SET PARITY ERROR
PRESS CONTINUE

GROUNDING S1 SETS THE PARITY ERROR FLIP-FLOP SO THE PROGRAM MAY TEST IOT 6101, AND PROGRAM INTERRUPT. IF NO ERROR HALTS, THE PRINT-OUT SHOWN BELOW OCCURS FOLLOWED BY A HALT.

UNGROUND PIN S1 M113 B09
GROUND PIN S2 M113 B09
PRESS START

AFTER GROUNDING PIN S2, SET THE SR TO 0226, PRESS LOAD ADDRESS, AND THEN START. GROUNDING PIN S2 HOLDS THE PARITY ERROR FLIP-FLOP IN THE CLEAR STATE SO THAT IOT 6101 MAY BE TESTED FOR CORRECT OPERATION. IF NO ERROR HALTS, THE PRINT-OUT SHOWN BELOW OCCURS FOLLOWED BY A HALT.

MOMENTARILY GROUND PIN S1 M113 B09
PRESS CONTINUE

REMOVE THE WIRE FROM PIN S2 AND TOUCH IT TO PIN S1 TO SET THE PARITY ERROR FLIP-FLOP. THE CLEAR PARITY ERROR IOT IS THEN TESTED. IF NO ERROR HALTS, TESTS T6 AND T7 ARE THEN PERFORMED. TEST T7 WILL LOOP UNTIL STOPPED BY THE OPERATOR.

PRINTOUTS = YES

SWITCH REGISTER OPTIONS = NO

MAINDEC-8I-D5BB-D

DF32 DISCLESS LOGIC TEST, MINIDISK

ABSTRACT
DISCLESS IS A TEST OF THE DF32 DISC LOGIC AND ITS COMPUTER INTERFACE. THIS PROGRAM DOES NOT TEST THE DISC, NOR ASSOCIATED ANALOG INTERFACE CIRCUITS.

(THE DISC IS NOT NEEDED FOR THESE ROUTINES) IF THE DISC IS CONNECTED, THE DISC MOTOR SHOULD BE TURNED OFF. FOR A COMPLETE TEST OF THE DISC SYSTEM, USE DF32 DISC DATA TEST.)

REQUIREMENTS
STANDARD PDP-8/I COMPUTER
DF32 DISC LOGIC
LIGHT CARD (FOR TESTING TRACK SELECTOR)

STORAGE = PROGRAM OCCUPIES MOST OF MEMORY FROM ADDRESS 100 TO 3400 AND LOCATIONS 0, 1 AND 2.

LOADING = BINARY LOADER

STARTING PROCEDURE
TURN DISC MOTOR OFF
LOAD DISCLESS INTO MEMORY
SELECT EM0 (DISC ZERO) (ALL OTHER UNITS TO OFF)

```
        WRITE INHIBIT SWITCHES OFF
        CONNECT LIGHT CARD IF TRACKS ARE TO BE TESTED (NOT NECESSARY
        FOR TEST)
        SET THE SWITCH REGISTER TO 100
        LOAD ADDRESS
        SET THE SWITCH REGISTER TO ALL ZERO (DOWN)
        PRESS START
        PROGRAM WILL RUN; IF THE LIGHTCARD IS USED, LIGHTS WILL LIGHT FROM
        0 TO 17(8) IN SEQUENCE AND THE PROGRAM WILL LOOP UPON COMPLETION.

PRINTOUTS = YES, ON ERROR

SWITCH REGISTER OPTIONS = YES
        SW0     UP      DELETE PRINT OUT
        SW1     UP      HALT AFTER ERROR
        SW2     UP      SUB TEST SCOPE LOOP
        SW3     UP      DO NOT EXIT SECTION
        SW4     UP      DELETE LIGHT BOX


MAINDEC-8I-D5FB

DF32D DISCLESS LOGIC TEST  MINIDISC

ABSTRACT
        DISCLESS IS A TEST OF THE DF32D DISC LOGIC AND ITS COMPUTER
        INTERFACE.  THIS PROGRAM DOES NOT TEST THE DISC, NOR ASSOCIATED
        ANALOG INTERFACE CIRCUITS.

        (THE DISC IS NOT NEEDED FOR THESE ROUTINES.  IF IT IS CONNECTED,
        THE DISC MOTOR SHOULD BE TURNED OFF.  FOR A COMPLETE TEST OF
        THE DISC SYSTEM USE DF32 DISC DATA TEST.)

REQUIREMENTS
        FAMILY-OF-EIGHT COMPUTER
        DF32D DISC LOGIC
        LIGHT CARD (FOR TESTING TRACK SELECTOR)

STORAGE = THE PROGRAM USES MEMORY FROM ADDRESS 0 TO 2600.

LOADING = BINARY LOADER

STARTING PROCEDURE
        TURN DISC MOTOR OFF.
        SELECT EM0 (DISC ZERO).  (ALL OTHER UNITS TO OFF).
        WRITE INHIBIT SWITCHES OFF.
        CONNECT LIGHT CARD IF TRACKS ARE TO BE TESTED (NOT NECESSARY
        FOR TEST).
        SET THE SWITCH REGISTER TO 200
        LOAD ADDRESS
        SET THE SWITCH REGISTER TO ALL ZERO (DOWN).
        PRESS START
        PROGRAM WILL RUN; IF THE LIGHT CARD IS USED, LIGHTS WILL LIGHT
        FROM 0 TO 17 IN SEQUENCE AND THE PROGRAM WILL LOOP UPON
        COMPLETION.

PRINTOUTS = YES, ON ERROR

SWITCH REGISTER OPTIONS = YES
```

SW0	UP	DELETE PRINT OUT
SW1	UP	HALT AFTER ERROR
SW2	UP	SUB TEST SCOPE LOOP
SW3	UP	DO NOT EXIT SECTION
SW4	UP	DELETE LIGHT BOX

MAINDEC-8I-D6AC-D

AX08 DIAGNOSTIC

ABSTRACT

THIS UNIT IS TESTED IN THREE SECTIONS; (A) AN INSTRUCTION TEST OF THE LOGIC; (B) A DISPLAY TEST FOR THE SCOPE; (C) A CALIBRATION SECTION FOR THE A/D CONVERTER.

REQUIREMENTS

PDP-8, 8/L OR 8/I STANDARD COMPUTER.
AX08 OPTION
ADJUSTABLE VOLTAGE SOURCE (0.01% OR BETTER, Z OUT <1.0 OHM)

STORAGE - PROGRAM USES MEMORY FROM ADDRESS 0 TO 4500.

LOADING - BINARY LOADER.

STARTING PROCEDURE

CONNECT NON-ZERO VOLTAGE SOURCE TO INPUT CONNECTOR FOR CHANNEL ZERO.
SET "TIMING CONTROL" MIMIMUM (C.C.W.)
SET SWITCH REGISTER TO STARTING ADDRESS - SA=0200
LOAD ADDRESS.
PRESS START.

PRINTOUTS - NO

SWITCH REGISTER OPTIONS - YES

SWITCHES

FOR DISPLAY — SELECT MUX CHANNEL

0 1 2 3 4 5 6 7 8 9 10 11

11=1 INHIBIT PRINTOUT

10=1 SCOPE LOOP
9=1 HALT ON ERROR
WITH 6=1 ENTER CALIBRATION CHECK
IN CALIBRATION TEST6 - 11=CHANNEL SELECTED
INTENSITY, 10=BRIGHT, 01=NORMAL, 00=DIM
ENTER DISPLAY TEST2=1(FOR MONITORING DISPLAY SWITCHES)
00=LEFT DIAGONAL(\)
01=RIGHT DIAGONAL (/)
11=ANGLE( )
10=BOX WITH AN "X" AND A CROSS IN IT( )

MAINDEC-8I-D6BB-(D)

GASCHROM-8 DIAGNOSTIC

ABSTRACT

THIS DIAGNOSTIC IS FOR TESTING THE UNIQUE HARDWARE OF THE GASCHROM-8 SYSTEMS. THIS TEST ASSUMES THAT THE COMPUTER, MULTIPLEXER, ANALOG TO DIGITAL CONVERTER, AND THE DISK HAVE ALL BEEN PREVIOUSLY CHECKED WITH THEIR RESPECTIVE DIAGNOSTIC.

REQUIREMENTS

PDP-8/I
DF 32 DISK
ADC1-A (A/D CONVERTER)
AMC8 (MULTIPLEXER CONTROL)
AFC6-A GASCHROM -8 INTERFACE
AF67
LOCAL OPERATOR CONSOLE BOXES

STORAGE - PROGRAM USES MEMORY FROM ADDRESS 0 TO 3000.

LOADING - BINARY LOADER

STARTING PROCEDURE

SET SWITCH REGISTER TO STARTING ADDRESS SA = 200
LOAD ADDRESS
CLEAR SWITCH REGISTER
PRESS START

STARTING ADDRESSES

200 NORMAL STARTING ADDRESS
201 SCOPE LOOP FOR LOC, BOXES, SR 0 TO 5=CHANNEL, 6 TO 11= LIGHTS AND RELAYS
PUSH BUTTONS ON LOC, BOX ARE EQUAL TO AC BIT 6 TO 8
202 SCOPE LOOP FOR REAL TIME CLOCK ENABLE ADJUST
203 SCOPE LOOP FOR CALIBRATING GAIN OR PROGRAMABLE AMPLIFIER
SR0=1, SR 6 TO 11 = MULTIPLEXER CHANNEL,
SR0=0, SR 5 TO 11 = GAIN
204 SCOPE LOOP FOR IOT'S 61XX, XX = SR 6 TO 11

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES

SW0 = 1 OR UP	HALT ON ERROR
SW1 = 1 OR UP	SCOPE LOOP
SW2 = 1 OR UP	INHIBIT PRINTOUT
SW3 = 1 OR UP	FOR TAKING MARGINS
SW4 = 1 OR UP	STATUS PRINTOUT OF SWITCH GAIN AMPLIFIER
SW5 = 1 OR UP	SWITCH GAIN AMPLIFIER IS USED WITH ALL CHANNELS,
SW5 = 0 OR DOWN	USE SR 6 TO 11 TO SELECT CHANNEL FOR SWITCH GAIN AMLIFIER (BIT 11 IS LSB)

MAINDEC-8I-D6CE-D

KV8/I DISPLAY DIAGNOSTIC

ABSTRACT
THE KV8/I DISPLAY DIAGNOSTIC IS WRITTEN TO ENABLE THE ALIGNMENT, ADJUSTMENT; EXERCISING, AND DIAGNOSIS OF THE KV8/I DISPLAY SO THAT A USER MAY OBTAIN A HIGH QUALITY PICTURE AND PROPER COMPUTER-OPERATOR INTERACTION VIA THE HARDWARE. THE PROGRAM IS COMPOSED OF VARIOUS CALIBRATION/ALIGNMENT ROUTINES AND DIAGNOSTIC ROUTINES WITH ERROR HALTS TO INDICATE PROGRAM DIAGNOSIBLE ERRORS, ERRORS WHICH ARE NOT PROGRAM DIAGNOSIBLE ARE GENERALLY VISUALLY DIAGNOSIBLE.

REQUIREMENTS
PDP-8/I COMPUTER WITH ASR-33 TELETYPE
KV8/I CONTROL
VT8/I STORAGE CRT DISPLAY
H306 JOYSTICK

STORAGE - MOST OF BANK 0

LOADING - BINARY LOADER

STARTING PROCEDURE
SET SWITCH REGISTER TO 0200
PRESS LOAD ADDRESS
CLEAR SWITCH REGISTER
PRESS START

PRINTOUTS - NO

SWITCH REGISTER OPTIONS - YES

MAINDEC-8I-D6DA-D

KV8/I MULTIPLEX DISPLAY DIAGNOSTIC

ABSTRACT
THE KV8I MULTIPLEX DISPLAY DIAGNOSTIC IS WRITTEN TO ENABLE THE ALIGNMENT, ADJUSTMENT, EXERCISING, AND DIAGNOSIS OF THE KV8I MULTIPLEX DISPLAY SO THAT A USER MAY OBTAIN A HIGH QUALITY PICTURE AND PROPER COMPUTER-OPERATOR INTERACTION VIA THE HARD WARE. THE PROGRAM IS COMPOSED OF VARIOUS CALIBRATION/ALIGN MENT ROUTINES AND DIAGNOSTIC ROUTINES WITH ERROR HALTS TO INDICATE PROGRAM DIAGNOSIBLE ERRORS. ERRORS WHICH ARE NOT PROGRAM DIAGNOSIBLE ARE GENERALLY VISUALLY DIAGNOSIBLE.

REQUIREMENTS
PDP-8/I COMPUTER WITH ASR-33 TELETYPE
KV8I MULTIPLEX CONTROL.
AT LEAST ONE VT01 STORAGE CRT DISPLAY WITH JOYSTICK

STORAGE - MOST OF BANK 0

LOADING - BINARY LOADER

STARTING PROCEDURE
SET SWITCH REGISTER TO 0200
PRESS LOAD ADDRESS
CLEAR SWITCH REGISTER
PRESS START

PRINTOUTS - NO

SWITCH REGISTER OPTIONS - YES

MAINDEC-8I-D8AC-D

DC08T1: DC08 OFF-LINE
IOT AND DATA TEST

ABSTRACT

PROGRAM DC08T1 IS DESIGNED TO COMPLETELY TEST THE IOTS AND DATA CONTROL LOGIC ASSOCIATED WITH FROM 1 TO THE FULL COMPLEMENT OF 128 ASYNCHRONOUS DATA LINES IN AN OFF-LINE CONFIGURATION.

REQUIREMENTS

PDP-8/I
DL8/I
DC08A,B,C,D,E

STORAGE - PROGRAM OCCUPIES LOCATIONS 0-7100

LOADING - BINARY LOADER

STARTING PROCEDURE

SET THE AC SWITCHES TO 0200.
PRESS LOAD ADDRESS
PRESS START.
FOLLOW INSTRUCTIONS.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES

MAINDEC-8I-D8AE-D

KW8/I REAL TIME CLOCK

ABSTRACT

THE KW8/I REAL TIME CLOCK, DIAGNOSTIC PROGRAM, IS DESIGNED TO THOROUGHLY TEST ALL IOT AND DATA TRANSFER INSTRUCTIONS USED IN THE M708 CLOCK CONTROL AND M709 CLOCK COUNTER. THE PROGRAM CONSISTS OF TWO ROUTINES; THE FIRST ROUTINE WHICH STARTS AT ADDRESS 200, TESTS ALL FLAGS, ENABLES, ETC. TO ASCERTAIN IF INITIALIZE HAS CLEARED THEM, AND THE SECOND PHASE OF THE CLOCK CONTROL PROGRAM TESTS EACH OF THE IOT'S TO DETERMINE IF THEY WILL SET AND/OR CLEAR EACH OF THE CONTROLLABLE FLIP-FLOPS, IT TEST FOR PROPER SKIPS, PROGRAM INTERRUPT AND FOR PROPER OPERATION OF ANY OF THE THREE CLOCKS. THE ERROR TYPE OUT FOR AN ERROR IN THE CLOCK CONTROL TEST IS AS FOLLOWS:

ERROR 0001

NOTE

ANY CLOCK SYSTEM WHICH SUPPLIES A CLOCK AT A FREQUENCY OF LESS THAN ONE CLOCK PULSE PER 10 SECONDS WILL CAUSE A FAILURE ERROR

0003.

THE SECOND ROUTINE STARTS AT ADDRESS 400, AND IS USED ONLY WHEN A M709 CLOCK COUNTER MODULE IS CONNECTED TO THE CLOCK CONTROL. THE CLOCK I.E. CRYSTAL, ADJUSTABLE OR LINE, MUST BE REMOVED FROM THE COMPUTER IN ORDER FOR THIS TEST TO RUN. THE ERROR TYPEOUT FOR AN ERROR IN THE CLOCK CONTROL TEST IS AS FOLLOWS:

```
CLOCK COUNTER FAILED
SENT RXED
0001 0000
```

THE SENT REFERS TO A 12-DIGIT NUMBER WHICH WAS LOADED INTO THE CLOCK CONTROL COUNTER, AND THE RXED REFERS TO THE NUMBER WHICH WAS TRANSFERRED BACK TO THE COMPUTER FROM THE COUNTER.

REQUIREMENTS
A STANDARD 4K PDP-8/I WITH AN ASR-33 TELETYPE
A KW8/I REAL TIME CLOCK CONTROL WITH ANY OF THE THREE BASIC CLOCKS
AS AN OPTION, THE CLOCK COUNTER

STORAGE - PROGRAM OCCUPIES MEMORY FROM ADDRESS 0 TO 0500 AND 1400 TO 1600.

LOADING - BINARY LOADER.

STARTING PROCEDURE
LOAD 0200 INTO SWITCH REGISTER
CLEAR SWITCH REGISTER
PRESS START

PRINTOUTS - YES, ON ERROR

SWITCH REGISTER OPTIONS - YES
SR0 0 HALT ON AN ERROR
SR1 0 PRINT ERROR NUMBER
SR2 1 SCOPE LOOP ON ERROR

MAINDEC-8I-D8BB-D

DC08T2-DC08 ON-LINE
DATA EXERCISE

ABSTRACT
PROGRAM DC08T2 PROVIDES A DC08 DATA TRANSFER EXERCISE CAPABLE OF COMMUNICATING WITH LOCAL 5 OR 8 LEVEL CODE DATA TERMINALS SUCH AS MODELS 28, 33 OR 35 TELETYPE.

THE PROGRAM OFFERS DATA ECHO AND DATA TRANSMIT OPERATION ON A PRESPECIFIED MIX OF LINES ASSOCIATED WITH A 5 LEVEL CODE OR 8 LEVEL CODE DATA CLOCK.

REQUIREMENTS
PDP-8/I, DL8/I, DC08/A AND TERMINAL DEVICE

STORAGE - PROGRAM OCCUPIES MEMORY FROM ADDRESS 0 TO 5600

LOADING - BINARY LOADER

STARTING PROCEDURE

SET THE AC SWITCHES TO 0200,
PRESS LOAD ADDRESS,
PRESS START,

THE PROGRAM WILL IDENTIFY ITSELF AND REQUEST DESIGNATION OF ALL 8 LEVEL CODE LINES TO BE EXERCISED. IF THE SYSTEM DOES NOT INCLUDE ANY 8 LEVEL CODE LINES, TYPE (CR). THE PROGRAM WILL PROCEED TO 5 LEVEL CODE LINE # DESIGNATION,

LINE NUMBERS (IN OCTAL) MAY BE DESIGNATED IN THE FOLLOWING FORMATS:

(A) 00,03,10, (CR) (I.E: LINE 0, 3 & 10)
(B) 00-17, (CR) (I.E: LINES 0-17)

NOTE THAT EACH LINE # OR GROUP OF LINES MUST BE FOLLOWED BY A COMMA (,). A (CR) TERMINATES LINE # DESIGNATION.

WHEN THE 8 LEVEL LINE #S ARE DESIGNATED, THE PROGRAM WILL REQUEST DESIGNATION OF THE 8 LEVEL CODE DATA CLOCK(1,2,3, OR 4).

THE DATA CLOCK IS DESIGNATED BY TYPING THE ASSOCIATED CLOCK # (1,2,3 OR 4) FOLLOWED BY (CR).

AFTER 8 LEVEL LINE # AND CLOCK DESIGNATION, THE PROGRAM WILL REQUEST DESIGNATION OF ALL 5 LEVEL CODE LINES TO BE EXERCISED. IF THE SYSTEM DOES NOT INCLUDE ANY 5 LEVEL CODE LINES, TYPE (CR). THE PROGRAM WILL PROCEED TO SELECTION OF ECHO MODE OR TRANSMIT MODE.

SPECIFY 5 LEVEL CODE LINE #S AND CLOCK NUMBER IN THE SAME MANNER AS INDICATED FOR 8 LEVEL CODE.

NEVER DESIGNATE THE SAME LINE #(S) OR CLOCK # FOR BOTH 8 & 5 LEVEL CODE OPERATION.

FOLLOWING 8 & 5 LEVEL CODE LINE # & CLOCK DESIGNATION, THE PROGRAM REQUESTS SELECTION OF ECHO MODE (SEC,4,3), OR TRANSMIT MODE (SEC,4,4), BY TYPING THE QUERRY ECHO MODE?-

TO SELECT ECHO MODE, TYPE Y (CR)
TO SELECT TRANSMIT MODE, TYPE N (CR)

THE PROGRAM WILL NOW INITIATE THE SELECTED OPERATION.

RESTART PROCEDURE
TO RESTART PROGRAM DC08T2 WITH NEW LINE # OR CLOCK # DESIGNATIONS, REPEAT STARTING PROCEDURE.

TO RESTART WITH A NEW OPERATION MODE SELECTION (I.E; TRANSMIT OR ECHO MODE): SET AC SWITCHES TO 0400, PRESS LOAD ADDRESS AND START. THE PROGRAM WILL REQUEST SELECTION OF THE NEW OPERATION MODE AS INDICATED IN THE START PROCEDURE.

TO RESTART WITH NO NEW PARAMETER DESIGNATIONS, SET THE AC SWITCHES TO 0436 AND PRESS LOAD ADDRESS & START.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES

MAINDEC-8I-D8EA-D

DC08-F & DC08-H OFF-LINE DIAGNOSTIC TEST

ABSTRACT
THE DC08-F & DC08-H OFF-LINE DIAGNOSTIC TEST IS A PROGRAM WHICH PROVIDES A METHOD FOR TESTING THE DC08-F, -FE, -FF, -FX AND/OR DC08-H OPTIONS OF THE DC08 DATA COMMUNICATIONS SYSTEM BY USING SPECIAL TEST CABLES WHICH ELIMINATE THE NEED FOR A MODEM (DATASET).

REQUIREMENTS
A DC08 DATA COMMUNICATION SYSTEM WHICH INCLUDES A PDP-8/I WITH AND ON-LINE TELEPRINTER, A DL8/I, AND A DC08-AI

ONE DC08-F (WITH 2 TO 128(10) COMMUNICATION LINES) AND/OR ONE TO TEN DC08-H UNITS)

ONE TEST CABLE FOR THE DC08-F AND/OR ONE TEST PLUG FOR THE DC08-H UNIT(S).

STORAGE - PROGRAM WILL OPERATE IN 4K WORDS OF CORE MEMORY.

LOADING - BINARY LOADERS

STARTING PROCEDURE
INSERT THE DC08-F TEST CABLE AND/OR DC08-H TEST PLUG
SET SR TO 0200* AND PRESS LOAD ADDRESS KEY,
SET THE PROPER SWITCH REGISTER SWITCHES (SRS)**
ACCORDING TO THE WAY THE TEST IS TO BE PERFORMED,
(UNDER "NORMAL" CONDITIONS, I.E., TESTING BOTH DC08-F AND DC08-H WITHOUT THE DC08-FX OPTION, ALL SRS SHOULD BE RESET.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES
SRS01 SET TO DELETE ERROR HALTS & TYPEOUTS AND ENABLE 'SCOPE LOOP.
(DO NOT SET SRS01 UNTIL AN ERROR HALT HAS OCCURRED.)
SRS 02 SET TO DELETE DC08-F CONTROL TESTS.
" 03 " " " " DATA TESTS.
" 04 " " " DC08-H (ACU) " .
" 06 " " SUPPRESS TELETYPE BELL RING AT END OF EACH PASS.
" 11 " IF DC08-FX OPTION IS TO BE TESTED.

PRESS START.

MAINDEC-8I-D8FA-D

DC08-F & DC08-H ON-LINE DIAGNOSTIC EXERCISER

ABSTRACT
THE DC08-F & DC08-H ON-LINE DIAGNOSTIC EXERCISER IS A PROGRAM WHICH PROVIDES A METHOD FOR TESTING THE DC08-F INTERFACE WITH UP TO 32 COMMUNICATION LINES AND THEIR ASSOCIATED DATA

SETS AND (OPTIONALLY) ONE ACU (DC08-H) ALL AT THE SAME TIME UNDER REALISTIC, ON-LINE CONDITIONS.

REQUIREMENTS
A DC08 DATA COMMUNICATION SYSTEM WHICH INCLUDES A PDP-8/I WITH AN ON-LINE TELEPRINTER, A DL8I, AND A DC08-A;
ONE DC08-F
TWO MODEMS; AND EITHER ONE COMMUNICATION LINE AND A REMOTE TERMINAL (TELETYPE) OR TWO COMMUNICATION LINES ARRANGED BACK-TO-BACK (I.E., FORMING A CLOSED LOOP).

STORAGE - THE PROGRAM WILL OPERATE IN 4K WORDS OF CORE MEMORY.

LOADING - BINARY LOADERS

STARTING PROCEDURE
SET SR TO 0200
PRESS LOAD ADDRESS KEY.
PRESS START.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - NO

MAINDEC-8I-D8HA-D

DM04 BREAK MULT CONTROL PRIORITY

ABSTRACT
THIS PROGRAM TESTS FOR PROPER OPERATION OF THE DM04 BREAK MULT CONTROL PRIORITY. IT SHOULD BE NOTED THAT CERTAIN AREAS OF THE DM04 ARE ONLY TESTED IN GO-NO-GO FASHION IN THAT A FAILURE IN THESE AREAS WILL CAUSE PROGRAM WIPEOUT. THE PROGRAM CONSISTS OF 10 TESTS AND A SPECIAL SCOPE LOOP.

A. POWER CLEAR AND DATA LINES TEST
B. CHANNEL 1 TEST
C. CHANNEL 2 TEST
D. CHANNEL 3 TEST
E. CHANNEL FLAGS TEST
F. EXTRA BREAK TEST
G. DATA TRANSFER TEST
H. CHANNEL 1 PRIORITY TEST
I. CHANNEL 2 PRIORITY TEST
J. CHANNEL 3 PRIORITY TEST
K. SPECIAL DATA SCOPE LOOP

REQUIREMENTS
FAMILY OF 8 COMPUTER WITH 4K OF MEMORY, A DM04 TESTER, AND THE DM04 BREAK MULT CONTROL PRIORITY TO BE TESTED.

STORAGE - THIS PROGRAM OCCUPIES CORE LOCATIONS 0000-7617 OCTAL.

LOADING - BINARY LOADER

STARTING PROCEDURE
TURN ALL CHANNEL CLOCKS TO "OFF"
LOAD ADDRESS 0200.

SET THE SWITCH REGISTER FOR DESIRED OPERATION.
NORMAL OPERATION IS WITH ALL SWITCHES DOWN.
PRESS KEY START.
NOTE 1. AFTER NORMAL HALTS FOR CLOCK SETTINGS, PRESS KEY START.
NOTE 2. IF A HALT OCCURS WITHOUT A PRINTOUT, KEY START WILL
STOP CHANNEL CLOCKS AND GIVE A PRINTOUT, KEY CONTINUE MAY CAUSE
PROGRAM WIPEOUT.

STARTING ADDRESSES

0200	NORMAL STARTING ADDRESS
0201	CHANNEL 1 TEST
0202	CHANNEL 2 TEST
0203	CHANNEL 3 TEST
0204	CHANNEL FLAGS TEST
0205	EXTRA BREAK TEST
0206	DATA TRANSFER TEST
0207	CHANNEL 1 PRIORITY TEST
0210	CHANNEL 2 PRIORITY TEST
0211	CHANNEL 3 PRIORITY TEST
0212	SPECIAL DATA SCOPE LOOP - THIS ROUTINE LOOPS DATA IN SWITCHES THRU CHANNEL 1, DATA SHIFTED LEFT ONCE THRU CHANNEL 2, AND DATA SHIFTED LEFT TWICE THRU CHANNEL 3.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES

SWITCH	0 (DOWN)	1 (UP)
0	CONTINUE TO NEXT TEST	REPEAT SAME TEST
1	CONTINUE AFTER ERROR	LOOP ERROR CONDITION
2	CHANGE DATA PATTERN	LOOP ON SAME DATA
3	HALT ON ERROR	CONTINUE AFTER ERROR
4	TYPEOUT ERRORS	INHIBIT ERROR TYPEOUTS
5	CONTINUE AFTER END OF PASS	HALT AT END OF PASS

MAINDEC-8/E-D0AB

PDP-8/E INSTRUCTION TEST 1

ABSTRACT
THIS IS A DIAGNOSTIC PROGRAM FOR TESTING THE AND, TAD,
OPERATE, AND BASIC MQ, INSTRUCTIONS OF THE PDP-8/E ONLY.

REQUIREMENTS
A PDP-8/E EQUIPPED WITH TELETYPE.

STORAGE - THIS PROGRAM USES LOCATIONS 0000-5314.

EXECUTION TIME - 1440 PROGRAM PASSES EVERY 5 SECONDS

LOADING - BINARY LOADER

STARTING PROCEDURE
SET SR TO 200 AND PRESS LOAD ADDRESS.
SET SR TO 7777 AND PUSH CLEAR AND CONTINUE
PROGRAM WILL HALT. MA=147
IF AC IS NOT EQUAL TO 0000 AN ERROR HAS OCCURRED.
PUSH CONTINUE, PROGRAM WILL RUN UNTIL STOPPED OR UNTIL

AN ERROR IS ENCOUNTERED.

PRINTOUTS = NO

SWITCH REGISTER OPTIONS = NO

MAINDEC-8E-D0BB

PDP-8/E INSTRUCTION TEST 2

ABSTRACT
THIS PROGRAM IS AN EXTENSIVE TEST OF AUTOINDEXING, INDIRECT ADDRESSING, AND THE DCA INSTRUCTION FOR THE PDP-8/E. IT ALSO OFFERS MINIMAL TESTING FOR INTERRUPT AND THE AND, TAD, ISZ, JMS, JMP, AND PROCESSOR IOT INSTRUCTIONS.

REQUIREMENTS
PDP-8/E EQUIPPED WITH TELETYPE

STORAGE = THE PROGRAM OCCUPIES MEMORY LOCATIONS 0000-4416

LOADING = BINARY LOADER

STARTING PROCEDURE
SET THE SWITCH REGISTER TO 200. PRESS LOAD ADDRESS, PUSH CLEAR AND THEN CONTINUE. A PROGRAMMED HALT OCCURS WHEN AN ERROR IS ENCOUNTERED.

PRINTOUTS = NO

SWITCH REGISTER OPTIONS = NO

MAINDEC-8E-D0CC-D

8E ADDER TESTS

ABSTRACT
THIS PROGRAM TESTS THE ADDER CIRCUITS OF THE PDP-8E. THE PROGRAM IS COMPOSED OF FIVE PARTS,
A SIMULATOR FOR THE TAD INSTRUCTION WHICH TESTS ALL COMBINATIONS OF TWO ARGUMENT ADDITIONS.
A SIMULATOR FOR ROTATE INSTRUCTIONS THAT TESTS ROTATION OF ALL POSSIBLE ARGUMENTS WITH RAL, RAR, RTL, RTR AND BSW.
A CARRY GENERATION TEST
A SERIES OF RANDOM NUMBER TESTS
A FIELD RELOCATION ADDER TEST

REQUIREMENTS
PDP-8E EQUIPPED WITH AT LEAST 4K OF MEMORY AND A TELETYPE

STORAGE = THE PROGRAM IS STORED IN LOCATIONS 0000-6000 AND UTILIZES LOCATIONS 7775-7777 AS A TEST AREA.

LOADING = BINARY LOADER

STARTING PROCEDURE
NORMAL STARTING ADDRESS-0200
RESTORE LOADERS-7600

```
        SET SR=0200
        PRESS ADDR LOAD SWITCH
        SET SWITCH REGISTER TO DESIRED FUNCTIONS
        PRESS CLEAR AND CONT SWITCHES

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES
        SR00=1  SUPRESS HALT ON ERROR
        SR01=1  SUPRESS ERROR TYPEOUT
        SR02=1  LOOP ON ERROR
        SR03=1  FAST TEST
        SR04=0  LOOP IN CURRENT MEMORY BANK
        SR04=1  RELOCATE TO NEXT EXISTING BANK
        SR06-08 AMOUNT OF EXTENDED BANKS OF MEMORY
        SR09=1  HALT AT END OF TEST
        SR10=1  SUPPRESS END OF TEST TYPEOUT
        SR11=1  LOOP ON PRESENT TEST


MAINDEC-8E-D0DB-D

RANDOM AND TEST

ABSTRACT
        THIS PROGRAM TESTS THE AND INSTRUCTING OF THE PDP-8E.
        THE AND INSTRUCTION, INSTRUCTION ADDRESS, OPERAND ADDRESS
        AND BOTH OPERANDS ARE PRODUCED BY RANDOM NUMBER GENERATORS.

REQUIREMENTS
        PDP-8E EQUIPPED WITH AT LEAST 4K OF MEMORY.
        TELETYPE.

STORAGE - THE PROGRAM IS INITIALLY LOADED INTO LOCATIONS 0000
        THRU 1177.  THE INITIAL TEST AREA IS 1200-7777.  WHEN
        THE PROGRAM RELOCATES, IT OCCUPIES 6600-7777.  THE TEST
        AREA IS THEN 0000-6577.
```

```
LOADING - BINARY LOADER

STARTING PROCEDURE
        SET SR TO 0200
        PRESS LOAD ADDRESS SWITCH
        SET SR TO 0000
        PRESS CLEAR AND CONTINUE SWITCHES

PRINTOUTS - NO

SWITCH REGISTER OPTIONS - YES
        SR00=1, SUPRESS HALT ON ERROR
        SR01=1, HALT AT END OF PASS, RESTORE LOADERS
        SR02=1, SUPPRESS PROGRAM RELOCATION
        SR03=1, SUPPRESS END OF PASS TYPEOUT
        SR09=1, HOLD DATA 1 CONSTANT
        SR10=1, HOLD DATA 2 CONSTANT
        SR11=1, HOLD INSTRUCTION CONSTANT


MAINDEC-8E-D0ER-D

RANDOM TAD TEST

ABSTRACT
        THIS PROGRAM TESTS THE TAD INSTRUCTING OF THE PDP-8E,  THE
        TAD INSTRUCTION, INSTRUCTION ADDRESS, OPERAND ADDRESS AND
        BOTH OPERANDS ARE PRODUCED BY RANDOM NUMBER GENERATORS.

REQUIREMENTS
        PDP-8E EQUIPPED WITH AT LEAST 4K OF MEMORY!
        TELETYPE

STORAGE - THE PROGRAM IS LOADED INTO LOCATIONS 6600 THRU 7577,
        THE TEST AREA IS 0000-6577;  TEMPORARY STORAGE LOCATIONS
        ARE LOCATED ON PAGE 0.

LOADING - BINARY LOADER

STARTING PROCEDURE
        SET SR TO 0200
        PRESS LOAD ADDRESS SWITCH
        SET SR TO 0000
        PRESS CLEAR AND CONTINUE SWITCHES

PRINTOUTS - NO

SWITCH REGISTER OPTIONS - YES
        SR00=1, SUPPRESS HALT ON ERROR
        SR03=1, SUPPRESS END OF PASS TYPEOUT
        SR09=1, HOLD DATA 1 CONSTANT
        SR10=1, HOLD DATA 2 CONSTANT
        SR11=1, HOLD INSTRUCTION CONSTANT


MAINDEC-8E-D0FC-D

RANDOM ISZ TEST
```

ABSTRACT
THIS PROGRAM IS WRITTEN TO TEST THE ISZ INSTRUCTION OF THE PDP-8/E. AN ISZ INSTRUCTION IS PLACED IN A FROM LOCATION, AND A TO LOCATION CONTAINS THE OPERAND. PART 1 OF THE PROGRAM SELECTS FROM, TO, AND OPERAND FROM A RANDOM NUMBER GENERATOR, WITH THE OPTION OF HOLDING ANY OR ALL CONSTANT. PART 2 USED A FIXED SET OF FROM, TO, AND OPERAND NUMBERS.

REQUIREMENTS
ONE PDP-8/E EQUIPPED WITH TELETYPE.

STORAGE - THIS PROGRAM USES LOCATIONS 0000-7600(8)

LOADING - BINARY LOADER

STARTING PROCEDURE
SET SR (SWITCH REGISTER) TO 0200 AND PRESS LOAD ADDRESS.
SET SR TO DESIRED MODE OF OPERATION; FOR MOST RUNS, SR9=0 ALLOWS THE MOST TESTING IN THE LEAST AMOUNT OF TIME.

FOR FIXED FROM, TO, OR OPERAND USAGE, THE FIXED NUMBER MAY BE SELECTED AND ENTERED INTO THE MEMORY LOCATIONS SHOWN BELOW:

FROM =0002
TO =0021
OPERAND =0022

PRESS, CLEAR AND THEN CONTINUE.

PRINTOUTS - ON ERROR

SWITCH REGISTER OPTIONS - YES
SR0(0) = HALT ON ERROR
SR1(1) = ELIMINATE ERROR PRINTOUTS
SR3 = FIXED FROMS (1)
RANDOM FROMS (0)
SR4 = FIXED TOS (1)
RANDOM TOS (0)
SR5 = FIXED OPERAND (1)
RANDOM OPERAND (0)
SR9(0) = DO ONE ISZ ONLY
SR11(1) = DO TEST PART 2 SR3, 4, 5, MUST BE 0'S
SR11(0) = DO TEST PART 1

MAINDEC-8E-D0GC-D

RANDOM DCA TEST

ABSTRACT
THIS PROGRAM TESTS THE DCA INSTRUCTION OF THE PDP-8/E. THE DCA INSTRUCTION ADDRESS, OPERAND ADDRESS, AND OPERANDS ARE TAKEN FROM A RANDOM NUMBER GENERATOR.

REQUIREMENTS
PDP-8/E EQUIPPED WITH TELETYPE.

STORAGE = THE DIAGNOSTIC PROGRAM IS STORED IN LOCATIONS 0000 THROUGH
0407. THE PROGRAM USES 0410 THROUGH 7600 FOR A TEST AREA.

LOADING = BINARY LOADER

STARTING PROCEDURE
SET SR TO 0200
PRESS LOAD ADDRESS
SET SR TO 0000
PRESS CLEAR THEN CONTINUE

PRINTOUTS = ON ERROR

SWITCH REGISTER OPTIONS = YES
SR0 (0) HALT AFTER ERROR PRINTOUT.
SR1 (1) BYPASS ERROR PRINTOUT
SR2 HOLD "FROM" CONSTANT (1). SELECT RANDOM "FROM" (0).
SR3 HOLD "OPERAND ADDRESS" CONSTANT (1). SELECT RANDOM "OPERAND
ADDRESS" (0).
SR4 HOLD "OPERAND" CONSTANT (1). SELECT RANDOM "OPERAND" (0).

MAINDEC-8E-D0HC-D

RANDOM JMP TEST

ABSTRACT
THIS PROGRAM TESTS THE JMP INSTRUCTION OF THE PDP-8/E. MOST OF
MEMORY IS USED AS A JUMP FIELD WITH A RANDOM NUMBER GENERATOR
SELECTING EACH JUMP FROM AND JUMP TO LOCATION.

REQUIREMENTS
PDP-8/E EQUIPPED WITH TELETYPE

STORAGE = PROGRAM OCCUPIES MEMORY FROM 0 TO 0421

LOADING = BINARY LOADER

STARTING PROCEDURE
SET SR TO DESIRED MODE. IF A PARTICULAR MEMORY LOCATION
IS DESIRED FOR EITHER A "CONSTANT FROM" OR "CONSTANT TO",
THIS MEMORY ADDRESS IS ENTERED INTO ONE OF THE LOCATIONS
SHOWN BELOW:

FROM 1 ADDRESS = 0120
FROM ADDRESS = 0117
TO ADDRESS = 0116

NOTE: ALWAYS MAKE (FROM1) = (FROM) =1

IF SR2 OR SR3 IS SET AFTER THE PROGRAM HAS BEEN STARTED, THE
LAST ADDRESS TAKEN FROM THE RANDOM NUMBER GENERATOR IS
USED REPEATEDLY.

PRESS CLEAR THEN CONTINUE.

PRINTOUTS = ON ERROR

SWITCH REGISTER OPTIONS = YES

SR0(0) HALT ON ERROR.

SR2 HOLD JUMP FROM ADDRESSES CONSTANT. (1)
SELECT RANDOM JUMP FROM ADDRESSES. (0)

SR3 HOLD JUMP TO ADDRESSES CONSTANT. (1)
SELECT RANDOM JUMP TO ADDRESSES. (0)

MAINDEC-8E-D0IB-D

BASIC JMP-JMS TEST

ABSTRACT
THIS IS A DIAGNOSTIC PROGRAM FOR TESTING THE JMP AND JMS INSTRUCTIONS OF THE PDP-8/E.

REQUIREMENTS
A PDP-8/E EQUIPPED WITH TELETYPE

STORAGE - THIS PROGRAM USES MOST OF MEMORY

LOADING - BINARY LOADER

EXECUTION TIME -THREE HUNDRED AND FORTY-FIVE PROGRAM LOOPS PER SECOND. A BELL IS SOUNDED EVERY 10 SECONDS, WHICH EQUALS 3456 PROGRAM LOOPS.

STARTING PROCEDURE
SET SR TO 200 AND PRESS LOAD ADDRESS.

PUSH CLEAR AND THEN CONTINUE. THE PROGRAM WILL STORE PARTS OF THE RIM AND BINARY LOADERS THAT WILL BE DESTROYED, AND THEN JMP TO 4200 TO BEGIN TESTING.

PRINTOUTS - NO

SWITCH REGISTER OPTIONS - NO

MAINDEC-8E-D0JC-D

RANDOM JMP-JMS TEST

ABSTRACT
THIS IS A DIAGNOSTIC PROGRAM TO TEST THE JMS INSTRUCTION OF THE PDP-8E. RANDOM FROM AND TO ADDRESSES ARE SELECTED FOR EACH TEST. THE JMP INSTRUCTION IS TESTED IN THAT EACH TEST REQUIRES A JMP TO REACH THE JMS.

REQUIREMENTS
PDP-8E EQUIPPED WITH TELETYPE.

STORAGE - LOCATIONS 0000-0574

LOADING - BINARY LOADER

STARTING PROCEDURE

SET SR TO 0200 AND PRESS LOAD ADDRESS.
IF IT IS DESIRED TO SET EITHER SR2 OR SR3, THE FROM OR
TO ADDRESS MAY BE SPECIFIED BY ENTERING THE ADDRESS INTO
THE LOCATIONS SHOWN BELOW

FROM = LOCATION 133
TO = LOCATION 131

IF SR2 OR SR3 IS SET AFTER THE PROGRAM HAS BEEN STARTED,
THE LAST ADDRESS TAKEN FROM THE RANDOM NUMBER GENERATOR
IS USED REPEATEDLY.
PRESS CLEAR, AND THEN CONT.

PRINTOUTS = ON ERROR

SWITCH REGISTER OPTIONS = YES
SR0(0) HALT ON ERROR.
SR2(1) HOLD THE FROM ADDRESS CONSTANT
SR2(0) SELECT RANDOM FROM ADDRESSES
SR3(1) HOLD THE TO ADDRESS CONSTANT
SR3(0) SELECT RANDOM TO ADDRESSES

MAINDEC-8E-D0LB-D

KE8-E (EAE) INSTRUCTION TEST 1

ABSTRACT
THIS PROGRAM IS A TEST OF ALL THE KE8-E EAE INSTRUCTIONS,
(EXCEPT MULTIPLY AND DIVIDE).

REQUIREMENTS
PDP-8/E OR /M PROCESSOR, KE8-E OPTION, AND A TELETYPE ARE
REQUIRED.

STORAGE = LOCATIONS 0000 THROUGH 7600 ARE USED.

LOADING = BINARY LOADER

STARTING PROCEDURE
LOAD ADDRESS 0200
SET ANY DESIRED OPTIONS IN THE SR, NORMAL = 5000
PRESS CLEAR AND CONTINUE.

PRINTOUTS = ON ERROR

SWITCH REGISTER OPTIONS = YES
CONTROL SWITCH SETTINGS DO NOT APPLY TO STEP COUNTER, GT,
MODE, AND COMBINED TESTS. AN ERROR WILL BE INDICATED BY
A PROGRAM HALT.

SR0=1 HALT ON ERROR
SR1=1 SCOPE MODE (REPEAT PATTERN AND/OR TEST)
SR2=1 PRINT ERROR INFORMATION
SR3=1 DO NOT EXIT CURRENT TEST
SR10=11

SR10	SR11	
0	0	EXECUTE TEST IN "A" AND "B" MODES
0	1	EXECUTE TEST IN "A" AND "B" MODES
1	0	SELECT "A" MODE.

```
MAINDEC-8E-D0MB-D

KE8-E (EAE) INSTRUCTION TEST 2
MULTIPLY AND DIVIDE

ABSTRACT
        THE PDP-8/E EAE (KE8-E) MULTIPLY-DIVIDE TEST, TESTS AND EX-
        ERCISES THE MULTIPLY AND DIVIDE HARDWARE OF THE KE8-E OPTION.
        FIXED NUMBERS WITH PREDETERMINED SOLUTIONS, AND RANDOM NUMBERS
        WITH SIMULATED SOLUTIONS ARE USED.  THE ABILITY TO OPERATE
        WITH THE INTERRUPT ENABLED IS ALSO TESTED.

REQUIREMENTS
        PDP-8/E OR /M PROCESSOR, KE8-E OPTION, AND AN ASR 33/35
        TELETYPE ARE REQUIRED.

STORAGE - LOCATIONS 0000 THROUGH 7570 ARE USED.

LOADING - BINARY LOADER

STARTING PROCEDURE
        LOAD ANY PAPER TAPE IN THE TELETYPE READER AND TURN IT ON.
        IF AN ERROR OCCURS, TURN THE TELETYPE READER OFF TO DE-
        TERMINE IF THE CAUSE WAS FROM INTERRUPT INTERACTION.
        LOAD ADDRESS 0200.  PRESS CLEAR AND CONTINUE.
        PROGRAM HALTS AT LOCATION 0201.

        SET ANY DESIRED OPTIONS IN SR AND PRESS CONTINUE.  IF SR1
        WAS SET THE PROGRAM WILL HALT AT LOCATION 4574 WITH THE
        SELECTED ROUTINE NUMBER IN THE AC.  SET SR1=0 AND SELECT
        THE DESIRED MODE OF OPERATION IN SR10 AND 11, THEN PRESS
        CONTINUE.

        THE PROGRAM WILL HALT AT PROGRAM END HALT (LOCATION 0250)
        AFTER THE LAST ROUTINE HAS BEEN EXECUTED, PROVIDED NO LOOP
        OPTIONS HAVE BEEN SET.

        NOTE:
                FOR A NORMAL PROGRAM RUN, SET SR SWITCHES TO 0000.
                PROGRAM WILL RUN FROM START TO FINISH, EXECUTING EACH
                ROUTINE IN "A" AND "B" MODES, PRINTING ALL ERRORS
                AS THEY OCCUR.

PRINTOUTS - ON ERROR

SWITCH REGISTER OPTIONS - YES
        SR0=1   HALT AFTER CURRENT ROUTINE.  PROGRAM HALTS AT THE
                COMPLETION OF THE CURRENT TEST ROUTINE.  THE COM-
                PLETED ROUTINE NUMBER IS DISPLAYED IN THE AC.

        SR1=0   SELECT MODE OF OPERATION ACCORDING TO SR10 AND SR11
        SR1=1   SELECT THE ROUTINE NUMBER WHICH IS IN SR9-11.  IF
                WHILE RUNNING THE PROGRAM SR1 IS SET TO A "1",
                THE PROGRAM WILL HALT WITH THE CURRENT ROUTINE
                NUMBER DISPLAYED IN THE AC, TO SELECT A NEW ROU-
                TINE AT THIS POINT, PLACE THE NEW DESIRED ROUTINE
```

IN SR9=11 AND PRESS CONTINUE, THE NEW ROUTINE NUMBER WILL NOW BE DISPLAYED IN THE AC.

SR2=1 LOOP ROUTINE, CURRENT ROUTINE IS REPEATED

SR3=1 LOOP PROGRAM, ENTIRE PROGRAM IS REPEATED.

SR4=1 LOCK ON TEST, THE TEST CURRENTLY BEING EXECUTED IS REPEATED.

SR5=0 PRINT ON ERROR.

SR5=1 HALT ON ERROR.

SR6=1 HALT AFTER PRINT, PROGRAM HALTS AFTER ERROR PRINTOUT.

SR7=1 PRINT FAILURE RATE, THE PROGRAM PRINTS THE NUMBER OF FAILURES PER HUNDRED REPETITIONS OF THE SAME TEST, PROGRAM HALTS AFTER THE PRINTOUT, SR5 MUST BE SET FOR THE PRINTOUT TO OCCUR.

SR8=1 PRINT SIMULATION AND/OR ENTER SCOPE LOOP, FOR ROUTINES 0 AND 1 PROGRAM PRINTS MULTIPLY SIMULATION AND ENTERS MULTIPLY SCOPE LOOP, FOR ROUTINES 2 AND 3 THE PROGRAM PRINTS DIVIDE SIMULATION AND ENTERS THE DIVIDE SCOPE LOOP, FOR ROUTINES 4 THROUGH 7 PROGRAM ENTERS THE EXERCISER SCOPE LOOP FOR THE INDIVIDUAL ROUTINE, SR5 MUST BE SET TO 0 FOR THIS OPTION TO BECOME ACTIVE.

SR9=11 WITH SR1=0	SR9	SR10	SR11	
	X	0	0	EXECUTE EACH ROUTINE IN "A" AND "B" MODES.
	X	0	1	EXECUTE EACH ROUTINE IN "A" AND "B" MODES.
	X	1	0	SELECT "A" MODE.
	X	1	1	SELECT "B" MODE.

SR9=11 WITH SR1=1	SR9	SR10	SR11	
	0	0	0	SELECT ROUTINE 0, FIXED MULTIPLY TEST.
	0	0	1	SELECT ROUTINE 1, RANDOM MULTIPLY TEST.
	0	1	0	SELECT ROUTINE 2, FIXED DIVIDE TEST.
	0	1	1	SELECT ROUTINE 3, RANDOM DIVIDE TEST.
	1	0	0	SELECT ROUTINE 4, MULTIPLY/DIVIDE EXERCISE TEST.
	1	0	1	SELECT ROUTINE 5, MULTIPLY/DIVIDE EXERCISE TEST.
	1	1	0	SELECT ROUTINE 6, MULTIPLY/DIVIDE EXERCISE TEST.
	1	1	1	SELECT ROUTINE 7, MULTIPLY/DIVIDE EXERCISE TEST.

MAINDEC-8E-D0NA-D-(D)

PDP8-E JMP SELF TEST

ABSTRACT

"JMP SELF" IS A WORST CASE TEST OF CORE MEMORY READ/WRITE GATES, IT WAS DESIGNED TO TEST THE ABILITY OF THE MEMORY ADDRESS SELECT GATES TO RAPIDLY SWITCH BETWEEN READ AND WRITE CURRENT I.E. REVERSE DIRECTION, THE PROGRAM LOADS CORE MEMORY FROM ADDRESS 0500(8) TO 7755(8) INCLUSIVELY IN MEMORY FIELD 0 AND ENTIRE CORE MEMORY IN EXTENDED FIELDS TO (JMP SELF).

THE PROGRAM TYPES A NULL CHARACTER ON THE TELETYPE, TURNS ON THE PROGRAM INTERRUPT (PI) AND THEN JUMPS TO THE MEMORY LOCATION TO BE TESTED. WHEN A PI OCCURS, THE INTERRUPTED CORE MEMORY LOCATION IS TESTED TO BE SURE IT WAS THE EXPECTED CORE MEMORY TO BE INTERRUPTED, ANY ERRORS WILL BE INDICATED BY A HALT AND AN ERROR MESSAGE ON THE TELETYPE, DEPENDING ON THE SWITCH SETTINGS.

REQUIREMENTS
A STANDARD 8E WITH AN ASR-33 OR EQUIVALANT TELETYPE.

STORAGE - THIS PROGRAM UTILIZES 0500(8) MEMORY LOCATIONS AND MUST RESIDE IN FIELD 0 ONLY.

LOADING - BINARY LOADER

STARTING PROCEDURE
WITH THE PROGRAM IN MEMORY, SET THE SWITCH REGISTER TO 0000
THEN PRESS KEY "EXT ADDR".
SET SWITCH REG. TO 0200 (OCTAL).
PRESS KEY "ADDR LOAD".
PLACE OCTAL VALUE OF EXTENDED FIELDS AVAILABLE IN 8E UNDER TEST IN SR09 THRU SR11.
PRESS KEY "CLEAR" THEN KEY "CONT".

PRINTOUTS - ON ERROR

SWITCH REGISTER OPTIONS - YES
SR00=1 INHIBIT ANY ERROR HALT, TEST NEXT SWITCH
SR01=1 INHIBIT ERROR TYPE OUT, COUNT FIELD ERRORS
SR02=1 SCOPE LOOP ON ERROR, SUPPRESS ERROR COUNT
SR03=1 TEST ONLY THE EXTENDED FIELD SET IN SWITCHES 9-11
SR09= EXTENDED MEMORY
SR10= EXTENDED MEMORY
SR11= EXTENDED MEMORY

MAINDEC-8E-D0PC-D

DB8-E INTERPROCESSOR BUFFER TEST
(FOR M8326 MODULE REVISION D OR BELOW)

ABSTRACT
THIS IS A DIAGNOSTIC PROGRAM TO CHECK THE IOT COMMANDS AND AC DATA TRANSFERS OF THE DB8-E. PART 1 OF THE DB8-E TEST IS SETUP SO THAT A PDP-8E CAN COMMUNICATE WITH ITSELF. PART 2 OF THE DB8-E TEST USES TWO PDP-8E PROCESSORS. THEY ARE CABLED TOGETHER SO THAT DATA TRANSFERS MAY TAKE PLACE BETWEEN THE TWO MACHINES.

REQUIREMENTS
TWO PDP-8E PROCESSORS EQUIPPED WITH TELETYPES AND DB8-E(M8326 BOARD) AND TWO CABLES BC08-R AND ONE BC08-J CABLE.

STORAGE - THIS PROGRAM USES LOCATIONS 0000-2123 IN FIELD 0.

LOADING - BINARY LOADER

STARTING PROCEDURE
PART 1
TAKE ONE CABLE BC08-J AND CONNECT THE OUTPUT TO THE INPUT ON THE DB8-E. SET SR=0200 AND PRESS LOAD ADDRESS.
SET SR=0000 AND PRESS CLEAR AND THEN CONTINUE.

PART 2
TAKE ONE CABLE BC08-R AND CONNECT ONE END TO THE OUTPUT OF DB8-E IN 8E#1 AND TO THE INPUT OF DB8-E IN 8E#2. TAKE THE

OTHER CABLE AND DO THE SAME WITH 8E#2 TO 8E#1. SET THE SR=2000 IN 8E#2, THIS COMPUTOR MUST BE STARTED FIRST. PRESS LOAD ADDRESS. SET THE SR=0000 AND PRESS CLEAR THEN CONTINUE. NOW SET THE SR=1000 IN 8E#1 AND PRESS LOAD ADDRESS. SET SR=0000 AND PRESS CLEAR AND THEN CONTINUE.

PART 2 FOR THE MOST PART IS A DATA VALIDITY CHECK. IF SOMETHING HAPPENS TO ONE OF THE FLAGS THE COMPUTER WILL HANG UP IN A LOOP. IF THIS HAPPENS RETRY OR GO BACK TO PART 1. ALWAYS STOP AND PRESS CLEAR KEY ON BOTH COMPUTERS BEFORE A RE-START OF THE PROGRAMS. IF THIS IS NOT DONE, THE PROGRAM MAY BE STARTED OUT OF SYNC DUE TO A FLAG BEING SET IN ONE OF THE COMPUTERS.

PRINTOUTS = ON ERROR

SWITCH REGISTER OPTIONS = YES
SR00=1 SUPPRESS HALT ON ERROR
SR01=1 SUPPRESS ERROR TYPEOUTS
SR02=1 LOOP ON ERROR, CONSTANT DATA IF DATA TEST
SR03=1 LOOP ON TEST
SR04=1 LOOP ON IOT TEST

MAINDEC-8E-D0RA-D-(D)

KE8-E EAE EXTENDED MEMORY EXERCISER

ABSTRACT
THE KE8-E EXTENDED MEMORY EXERCISER IS A TEST OF THE KE8-E "B MODE" INSTRUCTIONS WHICH DURING THE DEFER CYCLE USE THE WORD FOLLOWING THE INSTRUCTION TO OBTAIN THE OPERAND. THE CAPABILITY OF EACH INSTRUCTION TO ACCESS EVERY MEMORY FIELD FROM EVERY MEMORY FIELD THROUGH NON-AUTO INDEX AND AUTO INDEX IS TESTED.

REQUIREMENTS
PDP-8/E PROCESSOR WITH AT LEAST 4K OF MEMORY.
KE-8E OPTION, AND A TELETYPE ARE REQUIRED.

STORAGE - LOCATIONS 0000 THROUGH 7300

LOADING - BINARY LOADER

STARTING PROCEDURE
LOAD ADDRESS 0200.
SET ANY DESIRED OPTIONS IN THE SR
PRESS CLEAR AND CONTINUE.
TYPE IN THE VALUE OF THE HIGHEST MEMORY IN THE SYSTEM FOLLOWED BY A CARRIAGE RETURN.
(EG. 0 FOR 4K, 1 FOR 8K ON UP TO 7 FOR 32K)
IF THE INCORRECT NUMBER WAS TYPED, TYPE RUBOUT AND THEN RETYPE THE MEMORY FIELD VALUE.

NOTE:
FOR A NORMAL PROGRAM RUN, LOAD THE PROGRAM IN FIELD 0, SET SR TO 0200 AND PRESS LOAD ADDRESS, NOW SET SR TO 0000 AND PRESS CLEAR AND CONTINUE, AND RESPOND TO THE TELETYPE WITH THE VALUE OF THE HIGHEST FIELD

FOLLOWED BY A CARRIAGE RETURN. THE PROGRAM WILL NOW ACCESS EVERY FIELD FROM EVERY FIELD. AT THE COMPLETION OF A COMPLETE PROGRAM PASS, "KE8-EME" WILL BE TYPED ON THE TELETYPE.

PRINTOUTS = NO

SWITCH REGISTER OPTIONS = YES

SR0=0	HALT ON ERROR			
SR0=1	NO HALT ON ERROR			
SR1=0	NO LOOP			
SR1=1	SCOPE LOOP (REPEAT PATTERN)			
SR2=0	PRINT ON ERROR			
SR2=1	NO PRINT ON ERROR			
SR3=0	SEQUENTIALLY RUN TESTS			
SR3=1	SELECT TEST ACCORDING TO SR4-6			
SR3=1	SR4	SR5	SR6	
	0	0	0	SELECT DAD TEST
	0	0	1	SELECT DST TEST
	0	1	0	SELECT MUY TEST
	0	1	1	SELECT DIV TEST
	1	0	0	SELECT DAD AUTO INDEX TEST
	1	0	1	SELECT DST AUTO INDEX TEST
	1	1	0	SELECT MUY AUTO INDEX TEST
	1	1	1	SELECT DIV AUTO INDEX TEST
SR7=0	RELOCATE IF SR3 AND 8 ARE BOTH 0.			
SR7=1	HOLD IF			
SR8=0	SEQUENTIALLY CHANGE DF IF SR3=0			
SR8=1	HOLD DF			
SR9-11	STARTING DATA FIELD			
	9	10	11	
	0	0	0	DF0
	0	0	1	DF1
	0	1	0	DF2
	0	1	1	DF3
	1	0	0	DF4
	1	0	1	DF5
	1	1	0	DF6
	1	1	1	DF7

MAINDEC-8E-D0SA-D

DB8-E INTERPROCESSOR BUFFER TEST

ABSTRACT

THIS IS A DIAGNOSTIC PROGRAM TO CHECK THE IOT COMMANDS AND AC DATA TRANSFERS OF THE DR8-E. PART 1 OF THE DB8-E TEST IS SETUP SO THAT A PDP-8E CAN COMMUNICATE WITH ITSELF. PART 2 OF THE DB8-E TEST USES TWO PDP-8E PROCESSORS. THEY ARE CABLED TOGETHER SO THAT DATA TRANSFERS MAY TAKE PLACE BETWEEN THE TWO MACHINES.

REQUIREMENTS

TWO PDP-8E PROCESSORS EQUIPPED WITH TELETYPES AND DB8-E (M8326 BOARD) AND TWO CABLES BC08R AND ONE BC08-J CABLE.

STORAGE = THIS PROGRAM USES LOCATIONS 0000-2123 IN FIELD 0.

LOADING - BINARY LOADER

STARTING PROCEDURE

NOTE: IF IOTS OTHER THAN 650X ARE USED CHANGE THE FOLLOWING LOCATIONS IN THAT COMPUTER IN WHICH THIS DB8-E IS PLACED;

0701	65X1	0720	65X4	0737	65X7
0706	65X2	0725	65X5		
0713	65X3	0732	65X6		

PART 1
TAKE ONE CABLE BC08-J AND CONNECT THE OUTPUT TO THE INPUT ON THE DB8-E, SET SR=0200 AND PRESS LOAD ADDRESS, SET SR=0000 AND PRESS CLEAR AND THEN CONTINUE.

PART 2
TAKE ONE CABLE BC08-R AND CONNECT ONE END TO THE OUTPUT OF DB8-E IN 8E#1 AND TO THE INPUT OF DB8-E IN 8E#2, TAKE THE OTHER BC08-R CABLE AND DO THE SAME WITH 8E#2 TO 8E#1, SET THE SR=2000 IN 8E#2, THIS COMPUTOR MUST BE STARTED FIRST, PRESS LOAD ADDRESS, SET THE SR=0000 AND PRESS CLEAR THEN CONTINUE, NOW SET THE SR=1000 IN 8E#1 AND PRESS LOAD ADDRESS, SET SR=0000 AND PRESS CLEAR AND THEN CONTINUE.

PART 2 FOR THE MOST PART IS A DATA VALIDITY CHECK, IF SOMETHING HAPPENS TO ONE OF THE FLAGS THE COMPUTER WILL HANG UP IN A LOOP, IF THIS HAPPENS RETRY OR GO BACK TO PART 1, ALWAYS STOP AND PRESS CLEAR KEY ON BOTH COMPUTERS BEFORE A RESTART OF THE PROGRAMS, IF THIS IS NOT DONE, THE PROGRAM MAY BE STARTED OUT OF SYNC DUE TO A FLAG BEING SET IN ONE OF THE COMPUTERS.

PRINTOUTS - ON ERROR

SWITCH REGISTER OPTIONS - YES,
- SR00=1 SUPPRESS HALT ON ERROR
- SR01=1 SUPPRESS ERROR TYPEOUTS
- SR02=1 LOOP ON ERROR, CONSTANT DATA IF DATA TEST
- SR03=1 LOOP ON TEST
- SR04=1 LOOP ON IOT TEST

MAINDEC-8E-D1AB-D

MM8E 4K MEMORY CHECKERBOARD

ABSTRACT

THIS PROGRAM IS DESIGNED TO DETECT CORE FAILURES ON HALF-SELECTED LINES UNDER WORST CASE NOISE CONDITIONS, IT'S USE IS INTENDED FOR THE PDP-8E WITH A BASIC 4K MEMORY SYSTEM.

REQUIREMENTS

A PDP-8E COMPUTER WITH 4K OF MEMORY.

STORAGE - INITIALLY THE PROGRAM IS IN CORE LOCATIONS 200-777 AND IN CORE LOCATIONS 7000-7577

LOADING - BINARY LOADER

```
STARTING PROCEDURE
        LOAD ADDRESS WITH DESIRED ENTRY ADDRESS
        LOAD ADDRESS    0200    TEST UPPER CORE (1000-7777)
        LOAD ADDRESS    7000    TEST LOWER CORE (0000-6777)
        SET SWITCH REGISTER TO DESIRED OPERATION ACCORDING TO THE
        FOLLOWING TABLE
        SWITCH          0(DOWN)         1(UP)
         SR00       CONTINUE TESTING    1(UP)
         SR07       RELOCATE PROGRAM    INHIBIT RELOCATION
        PRESS KEY START

PRINTOUTS = NO

SWITCH REGISTER OPTIONS = YES



MAINDEC-8E-D1EC-D

MEMORY ADDRESS TEST

ABSTRACT
        MEMORY ADDRESS TEST, A RELOCATABLE PROGRAM, CHECKS FOR PROPER
        MEMORY ADDRESS SELECTION ON THE PDP-8/E.

REQUIREMENTS
        PDP-8/E EQUIPPED WITH A TELETYPE

STORAGE = MEMORY ADDRESS TEST OCCUPIES LOCATION 7200-7507.
        AFTER RELOCATING, THE TEST OCCUPIES LOCATION 0000-0307.

LOADING = BINARY LOADER

STARTING PROCEDURE
        SET SR TO 0200 AND PRESS LOAD ADDRESS
        SET SR FOR DESIRED OPERATION, PRESS CLEAR, THEN
        CONTINUE.  FOR MOST CASES THE SWITCH REGISTER SHOULD
        EQUAL ZERO.

PRINTOUTS = ON ERROR

SWITCH REGISTER OPTIONS = YES
        INITIAL SWITCH SETTINGS

        ALL SR'S = 0 RUN ADDRESS TEST HIGH AND RELOCATE PROGRAM AFTER
        1 PASS TO ADDRESS TEST LOW AND THEN RELOCATE PROGRAM TO ADDRESS
        TEST HIGH, REPEATEDLY.

        SR0(0)  HALT AFTER ERROR PRINTOUT
        SR1(1)  AND SR2(0)  RUN ADDRESS TEST HIGH ONLY
        SR1(1)  AND SR2(1)  RELOCATE PROGRAM AND RUN ADDRESS TEST LOW ONLY
        SR1(0)  PROGRAM WILL RELOCATE AFTER A PASS
        SR1(1)  PROGRAM WILL STAY IN TEST AND WILL NOT RELOCATE

        SWITCH SETTINGS AFTER PROGRAM IS RUNNING

        SR0(0)  HALT AFTER ERROR PRINTOUT
        SR1(0)  RUN TEST AND RELOCATE
        SR1(1)  RUN SAME TEST, DO NOT RELOCATE
```

MAINDEC-8E-D1FB

PDP-8/E EXTENDED MEMORY
ADDRESS TEST

ABSTRACT
THE PDP-8/E EXTENDED MEMORY ADDRESS TEST IS DESIGNED TO DETECT ANY LOCATION THAT CANNOT BE UNIQUELY ADDRESSED. THIS IS PERFORMED BY A SERIES OF FOUR TEST ROUTINES WHICH WILL TEST SYSTEMS EQUIPPED WITH FROM 8K TO 32K WORDS OF CORE MEMORY. AUTOMATIC PROGRAM RELOCATION IS PROVIDED IN ORDER TO TEST ALL MEMORY FIELDS FROM EACH MEMORY FIELD. TELETYPE PRINT-OUTS ARE PROVIDED FOR ERROR IDENTIFICATION, AND THE OPERATOR IS GIVEN A DEGREE OF CONTROL OVER THE PROGRAM BY VARIOUS SR SETTINGS.

REQUIREMENTS
A PDP-8/E COMPUTER EQUIPPED WITH A MINIMUM OF 8K WORDS OF CORE MEMORY.

STORAGE - THE PROGRAM OCCUPIES CORE LOCATIONS 0000 TO 3777.

LOADING - BINARY LOADER

STARTING PROCEDURE
SET THE SR TO THE INSTRUCTION FIELD AND DATA FIELD OF THE STACK WHICH CONTAINS THE PROGRAM.
PRESS KEY EXTD ADDR LOAD.
SET THE SR FOR DESIRED STARTING ADDRESS ACCORDING TO THE FOLLOWING TABLE.

ADDRESS	TEST EXECUTION
0200	RUN ALL TESTS
0201	RUN ONLY TEST 1
0202	RUN ONLY TEST 2
0203	RUN ONLY TEST 3
0204	RUN ONLY TEST 4

PRESS KEYS ADDR, LOAD, CLEAR, AND CONT. A SETUP SR MESSAGE WILL BE PRINTED.

SET THE SR FOR DESIRED OPERATION ACCORDING TO THE FOLLOWING TABLE.

SWITCH	0 (DOWN)	1 (UP)
SR00	CONTINUE AFTER ERROR	HALT AFTER ERROR
SR01	TYPEOUT ERRORS	INHIBIT ERROR TYPEOUTS
SR02	NORMAL	TTY BELL ON ERROR
SR03	RELOCATE PROGRAM	INHIBIT PROGRAM RELOCATION
SR04	NORMAL	CHANGE STACK LIMITS
SR05	NORMAL	HALT AFTER CURRENT TEST
SR06-08	STARTING STACK LIMIT (0-7)	
SR09-11	ENDING STACK LIMIT (0-7)	

PRESS KEY CONT.

PRINTOUTS = YES

SWITCH REGISTER OPTIONS = YES

MAINDEC-8E-D1GB-D

PDP-8/E MEMORY POWER ON/OFF TEST

ABSTRACT
THIS PROGRAM IS A MEMORY DATA VALIDITY TEST TO BE USED AFTER A SIMULATED POWER FAIL.

REQUIREMENTS
PDP-8/E EQUIPPED WITH TELETYPE

STORAGE = MEMORY LOCATIONS 0000(8) = 7601(8)

LOADING = BINARY LOADER

STARTING PROCEDURE
LOAD ADDRESS 0200, PRESS CLEAR AND THEN CONT. THE PROGRAM SHOULD THEN HALT AT LOCATION 0031(8). LOAD ADDRESS 0201, PRESS CLEAR AND THEN CONT. THE PROGRAM SHOULD NOW LOOP.

PRINTOUTS = ON ERROR

SWITCH REGISTER OPTIONS = NO

MAINDEC-8E-D1HB-D

PDP-8/E MEMORY EXTENSION AND TIME SHARE CONTROL TEST

ABSTRACT
THIS PROGRAM TESTS THE MEMORY EXTENSION AND TIME SHARE CONTROL LOGIC FOR PROPER OPERATION. THE PROGRAM EXERCISES AND TESTS ALL IOT'S ASSOCIATED WITH MEMORY EXTENSION AND TIME SHARE CONTROL.

ERRORS ENCOUNTERED DURING RUNNING WILL RESULT IN A PROGRAM "HALT" OR A "JUMP TO SELF", WHICH MAY OCCUR IN ANY FIELD DEPENDING ON THE PORTION OF THE TEST EXECUTED. ERRORS MAY BE IDENTIFIED BY REFERENCING THE PROGRAM LISTING.

REQUIREMENTS
PDP-8/E COMPUTER WITH THE KM8/E OPTION INSTALLED AND AT LEAST 4K OF EXTENDED MEMORY.

STORAGE = THE PROGRAM REQUIRES 4200(8) LOCATIONS OF CORE MEMORY AND MUST RESIDE IN FIELD 0 ONLY.

EXECUTION TIME = 3.75 MINUTES FOR 32K OF MEMORY

LOADING = BINARY LOADER

STARTING PROCEDURE
SR 9, 10, AND 11 MUST CONTAIN AN OCTAL VALUE EQUAL TO THE

NUMBER OF EXTENDED FIELDS AVAILABLE. NOTE THAT FIELD Ø
IS NOT INCLUDED.

SRØ=Ø WILL RESULT IN COMPLETE PROGRAM EXECUTION OF THE MEMORY

EXTENSION AND TIME SHARE CONTROL.

SRØ=1 WILL LOOP THE PROGRAM ON THE MEMORY EXTENSION PORTION
AND TEST THAT THE TIME SHARE IS DISABLED.

SR1=1 WILL RESULT IN AN END OF TEST HALT AT LOCATION 1565(8).

SET THE REGISTER TO Ø2ØØ OCTAL.
PRESS ADDRESS LOAD
PLACE THE OCTAL VALUE OF EXTENDED FIELDS AVAILABLE IN SR9-11.
PRESS CLEAR AND THEN CONTINUE.

THE PROGRAM SHOULD RUN UNTIL A FAILURE OCCURS OR UNTIL
STOPPED BY THE OPERATOR WITH SR1=1. NOTE THAT THE PROGRAM
SHOULD ALWAYS BE STOPPED WITH SR1=1.

THE TTY BELL WILL SIGNAL A SUCCESSFUL TEST AT THE COMPLETION
OF EVERY PASS.

PRINTOUTS = NO

SWITCH REGISTER OPTIONS = YES

MAINDEC-8E-D1IB-D

MI8/E BOOTSTRAP DIAGNOSTIC

ABSTRACT

THE MI8/E BOOTSTRAP DIAGNOSTIC VERIFIES CORRECT OPERATION OF
THE MI8/E BOOTSTRAP LOADER OPTION IN ALL ITS STANDARD
CONFIGURATIONS. THE DIAGNOSTIC PRODUCES A VISUAL TYPE OUT
AND/OR A BINARY OBJECT TAPE OF THE BOOTSTRAP BLOCK OF DATA
INFORMATION LOADED INTO CORE BY THE MI8/E MODULE UNDER TEST.
THIS VISUAL TYPEOUT AND BINARY OBJECT TAPE CAN THEN BE SAVED
FOR THE TESTING OF MI8/E MODULES OF THE SAME CONFIGURATION.

THE DIAGNOSTIC IS AVAILABLE IN A LOW AND HIGH CORE VERSION.
THE VERSION TO BE USED TO TEST A MI8/E MODULE WILL DEPEND ON THE
MEMORY LOCATIONS UTILIZED BY THAT PARTICULAR MODULE. THE LOW
CORE VERSION OF THE DIAGNOSTIC OCCUPIES AND USES MEMORY
LOCATIONS Ø2ØØ-1777 AND THE HIGH CORE VERSION OCCUPIES AND
USES MEMORY LOCATIONS 42ØØ-5777. USE THE VERSION THAT DOES
NOT CONFLICT WITH THE MEMORY LOCATIONS OF THE BOOTSTRAP BLOCK
FOR THE MI8/E MODULE UNDER TEST.

REQUIREMENTS

PDP-8/E COMPUTER
ASR-33 TELETYPE OR EQUIVALENT.
LOW OR HIGH SPEED PAPER TAPE READER.
LOW OR HIGH SPEED PAPER TAPE PUNCH.
M8I/E BOOTSTRAP DIAGNOSTIC;
MI8/E BOOTSTRAP LOADER OPTION.

STARTING PROCEDURE
INSTALL THE MI8/E MODULE TO BE TESTED

LOAD THE DIAGNOSTIC INTO THE SAME MEMORY FIELD AS UTILIZED BY THE MI8/E MODULE UNDER TEST USING THE STANDARD BINARY LOADER TECHNIQUE.

IF THE OPERATOR WISHES TO TEST THE MODULE USING ITS BINARY OBJECT TAPE, LOAD THE BINARY OBJECT TAPE INTO THE SAME MEMORY FIELD AS OCCUPIED BY THE DIAGNOSTIC USING THE STANDARD BINARY LOADER TECHNIQUE

DISABLE THE I/O DEVICE USED BY THE MODULE UNDER TEST. FOR EXAMPLE, PLACE NO TAPE IN READER, TURN OFF READER OR PUNCH, OR DISCONNECT THE M8350 TO THE DEVICE.

SET THE SWITCH REGISTER TO THE STARTING ADDRESS OF THE DIAGNOSTIC 0200/4200 AND PRESS ADDRESS LOAD.

SET THE SWITCH REGISTER TO THE INITIAL ADDRESS OF THE BOOTSTRAP DATA BLOCK OF INFORMATION OF THE PARTICULAR MODULE UNDER TEST AND PRESS CLEAR AND THEN CONTINUE. THE COMPUTER SHOULD HALT AT ADDRESS 0202/4202.

SET THE SWITCH REGISTER TO THE STARTUP ADDRESS OF THE MODULE UNDER TEST AND PRESS CLEAR AND THEN CONTINUE. THE COMPUTER SHOULD HALT AT ADDRESS 0205/4205.

IF THE OPERATOR HAS SELECTED TO TEST THE MODULE USING THE BINARY OBJECT TAPE, SET SWR0=1, IF VERIFICATION IS DESIRED BY VISUAL TYPEOUT, SET SWR0=0.

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES

SWR0=1 VERIFICATION BY BINARY OBJECT TAPE.
SWR0=0 VERIFICATION BY VISUAL TYPEOUT.
SWR1=1 PUNCH BINARY OBJECT TAPE.
SWR2=1 LOW SPEED PAPER TAPE PUNCH.
SWR2=0 HIGH SPEED PAPER TAPE PUNCH.
SWR6=8 MEMORY FIELD OF BINARY LOADER.
SWR9=11 AMOUNT OF EXTENDED MEMORY FIELDS

MAINDEC-8E-D1JB-D-(D)

MR8-EA READ ONLY MEMORY TEST

ABSTRACT
THE READ ONLY MEMORY TEST IS A PROGRAM TO COMPARE A WIRED MEMORY TO A BINARY TAPE. THE BINARY TAPE IS PROVIDED BY THE CUSTOMER. THROUGHOUT THIS WRITE UP AND MESSAGE TYPEOUTS, THE DIAGNOSTIC WILL BE REFERRED TO AS (ROM TEST TAPE). THE BINARY TAPE THAT IS PROVEDED BY THE CUSTOMER WILL, BE REFERRED TO AS (ROM CONTENTS TAPE). THIS ROM CONTENTS TAPE MAY ALSO BE SUPPLIED BY DIGITAL EQUIPMENT INC. AS ROM TO8E SYSTEMS HANDLER (MR8-EC) WHICH WILL CONSIST OF A LISTING AND A PAPER TAPE (8E-D1KA-PB).
THE ROM TEST TAPE MAY BE LOADED AND RUN IN ANY FIELD.

THE ROM TEST TAPE WILL COMPARE THE ROM CONTENTS TAPE AND THE
ROM IN THREE WAYS, TEST 1 IS A DIRECT COMPARISON OF THE TWO,
THE SECOND TEST IS A RANDOM ACCESS DATA COMPARE, AND
THE THIRD TEST IS A VARIABLE DELAY WITH RANDOM ACCESS.
IN EACH OF THE THREE TESTS ALL 400 LOCATIONS WILL BE EXAMINED.

REQUIREMENTS
PDP-8/E WITH 4K MEMORY AND 2 PAGE MR8-EA ROM, LOW SPEED OR HIGH
SPEED READER AND ASR 33 TELETYPE OR EQUIVALENT.

STORAGE - ROM TEST TAPE LOW (MAINDEC 8E-D1JA-PR1) WILL OCCUPY 0-4000, ROM TEST
TAPE HIGH (MAINDEC 8E-D1JA-PB2) WILL OCCUPY 4600-7700. THE ROM ITSELF
MAY OCCUPY 400 LOCATIONS IN ANY FIELD.

LOADING - CHECK ADDRESS OF ROM AND THE ROM TEST TAPE TO SEE THAT THEY DO
NOT OVERLAY EACH OTHER IN CORE.

USING BINARY LOADER, LOAD IN ROM TEST TAPE LOW OR ROM TEST
TAPE HIGH DEPENDING ON WHERE ROM IS LOCATED.

STARTING PROCEDURE
SET SWITCH REGISTER TO 0400 OR 5200
PRESS LOAD ADDRESS, CLEAR AND CONTINUE
SET SWITCH 0 FOR HIGH OR LOW SPEED READER AND PLACE (ROM CONTENTS
TAPE) IN READER
"PRESS CONTINUE"
SET SWITCH REGISTER FOR ROM START ADDRESS AND FIELD
"PRESS CONTINUE"
SET SWITCH REGISTER FOR DESIRED FUNCTIONS
"PRESS CONTINUE"

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES
SWITCHES 0-2 = LOOP ON ERROR, INHIBIT ERROR TYPE OUTS, INHIBIT HALT ON ERROR
SWITCHES 6-8 = EXECUTION OF TEST 1, 2, 3
SW0 = 1 LOOP ON ERROR
SW1 = 1 NO ERROR PRINT OUT WILL OCCUR

SW2 = 1 INHIBIT ERROR HALTS
SW6 = 1 TEST ONE WILL BE PERFORMED
SW7 = 1 TEST TWO WILL BE PERFORMED
SW8 = 1 TEST THREE WILL BE PERFORMED
SW11 =1 CONTINUOUS LOOPING THROUGH THE SELECTED TESTS

IF SWITCHES 6,7,8 ARE NOT SET ALL TESTS WILL BE PERFORMED.

MAINDEC-8E-D1KA-D

MR8-EC ROM CONTENTS
(TD8-E DECTAPE SYSTEM
HANDLER

ABSTRACT

THE PURPOSE OF "MR8-EC ROM CONTENTS" IS TO SPECIFY THE CONTENTS OF THE TD8-E DECTAPE SYSTEM HANDLER ROM (MR8-EC) IN THE FORM OF A ROM CONTENTS BINARY TAPE AND PROGRAM LISTING. THIS MAINDEC IS NOT A PROGRAM BUT IS INTENDED TO BE USED ONLY IN CONJUNCTION WITH THE LATEST REVISION OF THE MR8-E ROM TEST (MAINDEC-8E-D1JB) TO TEST THE MR8-EC ROM. REFER TO THE MR8-E ROM TEST FOR A DETAILED TEST OPERATING PROCEDURE.

MAINDEC-8E-D2CA-D

HIGH-SPEED READER/PUNCH TESTS

ABSTRACT

THE PC8-E HIGH-SPEED READER AND PUNCH TESTS ARE A TEST PACKAGE USED TO TEST THE TYPE PC02 AND PC03 HIGH-SPEED READER-PUNCH WHEN ATTACHED TO A PDP-8/E SYSTEMS. THE TESTS PERFORM BASIC INPUT AND OUTPUT CONTROL LOGIC TESTS, READER AND PUNCH TESTS, READER AND PUNCH SPEED PRINTOUTS, AND PROVIDE MAINTENANCE LOOPS USEFUL IN ADJUSTING THE READER AND PUNCH.

THE AVAILABLE TEST PROGRAMS ARE:

PRG0 = BASIC READER AND READER CONTROL LOGIC TEST
PRG1 = BASIC PUNCH AND PUNCH CONTROL LOGIC TEST
PRG2 = READER TEST, SPECIAL BINARY COUNT PATTERN
PRG3 = PUNCH TEST, SPECIAL BINARY COUNT PATTERN
PRG4 = PUNCH VERIFY, SPECIAL BINARY COUNT PATTERN
PRG5 = PUNCH TEST, RANDOM CHARACTERS
PRG6 = PUNCH VERIFY, RANDOM CHARACTERS,
PRG7 = COMBINED READER-PUNCH TEST, SPECIAL BINARY COUNT PATTERN.
PRG10 = READ AMPLIFIER ADJUSTMENT LOOP, 1'S AND 0'S TAPE.
PRG11 = PUNCH ANY CHARACTER IN SR LOOP.
PRG12 = 1'S AND 0'S PUNCH LOOP.
PRG13 = READER SPEED PRINT LOOP.
PRG14 = PUNCH SPEED PRINT LOOP.
PRG15 = READ X CHARACTERS, STALL Y MS LOOP.

REQUIREMENTS

PDP-8/E WITH ASR33/35 TELETYPE, PR8-E READER, OR PP8-E PUNCH, OR

PC8-E READER/PUNCH, THE FOLLOWING TAPES ARE REQUIRED IN CON-
JUNCTION WITH THIS TEST:

MAINDEC-00-D2G1-PT
MAINDEC-00-D2G2-PT
MAINDEC-00-D2G4-PT

STORAGE - LOCATIONS 0000 THROUGH 4377 ARE USED.

LOADING - BINARY LOADER

STARTING PROCEDURE
PRG0
INSURE THAT THE TELETYPE IS ON-LINE.
LOAD READER WITH ALL 0'S TEST TAPE, PREFERABLY THE TAPE
SHOULD BE SPLICED INTO A LOOP
LOAD ADDRESS 0200
SET SR TO 0000, PRESS START.
PROGRAM HALTS AT LOC 0242 TO PERMIT SETTING OF SR OPTIONS.
SET DESIRED OPTIONS AND PRESS CONTINUE.

PRG0 SR OPTIONS

SR0 HALT AT ROUTINE END, ROUTINE NUMBER IN AC.
SR1 SELECT ROUTINE WHOSE NUMBER IS SET IN SR8-SR11.
SR2 LOOP PROGRAM.
SR3 0=HALT ON ERROR, 1=DO NOT HALT ON ERROR.
SR4 SKIP TEST AFTER ERROR.
SR5 ENTER SCOPE LOOP AFTER ERROR.
SR8
THROUTH ROUTINE NUMBER TO BE SELECTED.
SR11

THE PROGRAM RUNS AND HALTS AT PROGRAM END HALT, AT LOC 0305
UNLESS PREVENTED FROM ENDING BY ERRORS, OR SR OPTIONS.

PRINTOUTS - ON ERROR

SWITCH REGISTER OPTIONS - YES

MAINDEC-8E-D2D8-D

CM8E CARD READER TEST

ABSTRACT
THE PROGRAM TESTS THE OPTICAL MARK CARD READER FOR CORRECT
ALPHANUMERIC AND BINARY OPERATIONS, IT ALSO TESTS CONTROL
INTERRUPT AND TIMING.

REQUIREMENTS
PDP-8/E WITH OPTICAL MARK C,D,I 100 MS CARD READER
OPTICAL MARK ALPHANUMERIC CARD DECK (MAINDEC-89-D2C1-CA)
OPTICAL MARK BINARY CARD DECK (MAINDEC-89-D2B2-C)
OPTICAL MARK SENSE CARD DECK (MAINDEC-89-D2B3-C)

LOADING - BINARY LOADER

STARTING PROCEDURE

TURN ON CARD READER POWER

AT THIS POINT THE ONLY RED LIGHT TO BE ON SHOULD BE CARD SUPPLY, REFERENCE G,D,I, MANUAL TO REMEDY OTHER RED LIGHT ERROR CONDITIONS.

LOAD ADDRESS 0202

PROGRAM WILL PRINT "IOTS OK" IF TEST RUNS, PROGRAM WILL HALT IF TEST FIALS, REFERNECE SYMBOLIC LISTING AND COMMENTS FOR APPROPRIATE ERROR DESCRIPTION.

PLACE ALPHANUMERIC OR BINARY TEST DECK IN LOWER HOPPER

TURN ON CARD READER POWER

DEPRESS CARD READER START
AT THIS POINT ALL RED LIGHTS SHOULD BE OFF.

LOAD ADDRESS 0204

SELECT APPROPRIATE SWITCH CONTROL

AT THIS POINT PROGRAM WILL ATTEMPT TO READ FOUR CARDS AND THEN ISSUE MESSAGE "OPERATOR MUST NOW PRESS READ STOP."

AFTER READ STOP IS PRESSED PROGRAM WILL THEN ISSUE MESSAGE "OPERATOR MUST NOW PRESS READ START."

PROGRAM WILL PRINT "MANUAL TESTS OK" IF TEST RUNS, PROGRAM WILL HALT IF TEST FAILS, REFERENCE SYMBOLIC LISTING AND COMMENTS FOR APPROPRIATE ERROR DESCRIPTION.

STARTING ADDRESSES OF CARD READER TESTS

0200 = ALPHA AND BINARY DATA RELIABILITY TESTS
0202 = STATIC IOT TESTS
0204 = MANUAL INTERVENTION TESTS
0206 = COMPRESSED CODE DATA RELIABILITY TESTS
0210 = VALIDITY BIT DATA RELIABILITY TESTS
0212 = MARK SENSE DATA TEST
2300 = SCOPE LOOP

PRINTOUTS = YES

SWITCH REGISTER OPTIONS = YES

SW0=0	TEST ALPHANUMERIC DECK
SW0=1	TEST BINARY DECK
SW1=0	PRINT DATA ERROR
SW1=1	SUPPRESS PRINT DATA ERROR
SW2=0	HALT AFTER DATA ERROR
SW2=1	SUPPRESS HALT AFTER DATA ERROR
SW3=0	HALT AT END OF TEST DECK
SW3=1	CONTINUE TO NEXT TEST DECK WITHOUT HALT.

ABSTRACT

THE PROGRAM TESTS THE CRØ3 G,D,I CARD READER FOR CORRECT ALPHANUMERIC AND BINARY OPERATIONS. IT ALSO TESTS CONTROL INTERRUPT AND TIMING.

REQUIREMENTS

PDP-8/E WITH CRØ3 G,D,I 1ØØ MS CARD READER
CR03 ALPHANUMERIC CARD DECK
CR03 BINARY CARD DECK

LOADING - BINARY LOADER

STARTING PROCEDURE

STATIC IOT TESTS

PLACE A CARD DECK INTO INPUT HOPPER

TURN ON CARD READER POWER AND THEN DEPRESS MOTOR START

AT THIS POINT THE ONLY RED LIGHT TO BE ON SHOULD BE READ STOP. REFERNECE G,D,I, MANUAL TO REMEDY OTHER RED LIGHT ERROR CONDITIONS.

LOAD ADDRESS Ø2Ø2

DEPRESS CLEAR AND THEN DEPRESS CONTINUE

PROGRAM WILL PRINT "IOTS OK" IF TEST RUNS. PROGRAM WILL HALT IF TEST FAILS, REFERENCE SYMBOLIC LISTING AND COMMENTS FOR APPROPRIATE ERROR DESCRIPTION.

MANUAL INTERVENTION TESTS

PLACE ALPHANUMERIC OR BINARY TEST DECK IN LOWER HOPPER

TURN ON CARD READER POWER

DEPRESS MOTOR START AND THEN DEPRESS READ START
AT THIS POINT ALL RED LIGHTS SHOULD BE OFF

LOAD ADDRESS Ø2Ø4

SELECT APPROPRIATE SWITCH CONTROL (REFERENCE 4,1).

DEPRESS CLEAR AND THEN DEPRESS CONTINUE

AT THIS POINT PROGRAM WILL ATTEMPT TO READ FOUR CARDS AND THEN ISSUE MESSAGE "OPERATOR MUST NOW PRESS READ STOP."

AFTER READ STOP IS PRESSED PROGRAM WILL THEN ISSUE MESSAGE "OPERATOR MUST NOW PRESS READ START."

PROGRAM WILL PRINT "MANUAL TESTS OK" IF TEST RUNS. PROGRAM WILL HALT IF TEST FAILS, REFERENCE SYMBOLIC LISTING AND COMMENTS FOR APPROPRIATE ERROR DESCRIPTION.

STARTING ADDRESS OF CARD READER TESTS

```
        0200 =  ALPHA AND BINARY DATA RELIABILITY TESTS
        0202 =  STATIC IOT TESTS
        0204 =  MANUAL INTERVENTION TESTS
        0206 =  COMPRESSED CODE DATA RELIABILITY TESTS
        0210 =  VALIDITY BIT DATA RELIABILITY TESTS
        2300 =  SCOPE LOOP

PRINTOUTS = YES

SWITCH REGISTER OPTIONS = YES
        SW0=0   TEST ALPHANUMERIC DECK
        SW0=1   TEST BINARY DECK
        SW1=0   PRINT DATA ERROR
        SW1=1   SUPPRESS PRINT DATA ERROR
        SW2=0   HALT AFTER DATA ERROR
        SW2=1   SUPPRESS HALT AFTER DATA ERROR
        SW3=0   HALT AT END OF TEST DECK
        SW3=1   CONTINUE TO NEXT TEST DECK WITHOUT HALT.


MAINDEC-8E-D2FB-D

DECWRITER (LA30) CONTROL/EXERCISER TEST

ABSTRACT
        THE LA30 DECWRITER IS CAPABLE OF SELECTABLE 110, 150, AND 300
        BAUD PRINT RATES.

        IF THE DECWRITER IS AN LA30S (INDICATED SO WITH AC SWITCH 4 = 1)
        FILL (NON PRINTING) CHARACTERS WILL BE ISSUED AFTER A CARRIAGE
        RETURN IF OPERATING AT A 300 BAUD PRINT RATE (STARTING ADDRESS 201).

        ITEMS 12,13, AND 14 (TIMING TESTS) ARE NOT APPLICABLE FOR A LA30
        SERIAL LINE INTERFACE DECWRITER, AND ARE ABORTED WHEN AC SW 4 = 1.

        ITEM 4 PRINTS A MAXIMUM AND A MINIMUM OF 80 COLUMN WHEN THE
        LA30 IS SERIAL LINE INTERFACED, THEREFORE THE TYPEOUT!

        MAXIMUM COLUMNS IN LINE = 80

        SHOULD ALWAYS OCCUR BECAUSE THERE IS NO DIAGNOSTIC TESTING.

        THIS CONTROL/EXERCISER PROGRAM CHECKS THE FOLLOWING FUNCTIONS
        OF A LA30 OR LA30S DECWRITER.

REQUIREMENTS
        ANY OF THESE PROCESSORS: PDP-8, 8/I, 8/L, 8/E, 8/S; OR PDP-12
        DECWRITER (LA30 OR LA30S)
        A DC02 OR A PT08 (OPTIONAL)

STORAGE - THIS PROGRAM USES FROM 0 TO 4400 (OCTAL) FOR THE TESTS
        AND FROM 5000 TO 6600 (OCTAL) FOR STORAGE OF THE MESSAGES.
        THE PROGRAM MUST RESIDE IN FIELD 0 ONLY.

LOADING - BINARY LOADER

STARTING PROCEDURE
        LOAD ADDRESS 200, OR 201
        PRESS START
```

```
THE PROGRAM WILL HALT AT ADDRESS 3116 WITH THE AC = 7777.
     [FOR A PDP-8/E: START = CLEAR, THEN CONT.]

START-UP QUESTION #1:
        ? IS THE DECWRITER IN THE CONSOLE TTY POSITION ?

        (YES)   PUT THE OCTAL NUMBER 0304 IN THE SWITCHES AND
                PRESS "CONT".
        (NO)    GO IMMEDIATELY TO START-UP QUESTION #2.

START-UP QUESTION #2:
        ? ARE YOU TESTING THE DECWRITER WITH A DC02 ?

        (YES)   SELECT A "DC02 GROUP" AND A "DC02 STATION" FROM THE
                "DC02" TABLE AND PUT THE VALUE IN THE SWITCHES, PRESS
                "CONT"

        IF A "GROUP" IS NOT SELECTED (AC SWITCHES 08 THRU 11 = 0)
        THE PROGRAM WILL ASSUME A DC02 IS NOT AVAILABLE.

        (NO)    SET THE SWITCHES = 0000 THEN PRESS "CONT", GO
                IMMEDIATELY TO START-UP QUESTION #3.

START-UP QUESTION #3:

THE PROGRAM IS HALTED AT MEMORY ADDRESS 2744.

        ? WHAT ARE THE DEVICE CODES FOR THE STATION UNDER TEST ?

CONFIGURE A DEVICE CODE FROM THE PT08 "DEVICE CODE TABLE" INTO THE AC
SWITCHES.  PRESS "CONT"

THE PROGRAM WILL HALT AT ADDRESS 0401 WITH THE AC = 0000.
AT THIS TIME, SELECT THE DESIRED SWITCH OPTIONS-INCLUDING
ONE OF THE "PROCESSOR SELECTION SWITCHES"-THEN PRESS "CONT".

THE TITLE OF THE DIAGNOSTIC WILL BE PRINTED ON THE DECWRITER
IMMEDIATELY FOLLOWED BY THE SELECTED TESTS.  IF THE PROCESSOR IS
UNABLE TO COMMUNICATE (RETURN A PRINT DONE FLAG) THE PROGRAM WILL
HALT AT ADDRESS 1441.  CONTINUATION OF THE TEST FROM THIS ERROR
HALT WILL PROVIDE NO USEFUL DATA.

                DC02 TABLES:

SELECT SWITCH 00 THRU 07 FOR THE "DC02 STATION"
        SW00 = STATION #1
        SW01 = STATION #2
        SW02 = STATION #3
        SW03 = STATION #4
SELECT SWITCH 04 THRU 07 FOR A DC02-F
        SW04 = STATION #5
        SW05 = STATION #6
        SW06 = STATION #7
        SW07 = STATION #8
SELECT SWITCH 08 THRU 11 FOR THE "DC02 GROUP"
        SW08 = GROUP #1 CONTROL FOR STATIONS 1  TO 8
        SW09 = GROUP #2 CONTROL FOR STATIONS 9  TO 16
        SW10 = GROUP #3 CONTROL FOR STATIONS 17 TO 24
        SW11 = GROUP #4 CONTROL FOR STATIONS 25 TO 32
```

PT08 DEVICE CODE TABLE!

STATION #1	4041
STATION #2	4243
STATION #3	4445
STATION #4	4647
STATION #5	1112

PRINTOUTS = YES

SWITCH REGISTER OPTIONS = YES

SW00 = 1 INHIBIT ERROR HALT
SW00 = 0 ERROR HALT

SW01 = 1 INHIBIT ERROR MESSAGE PRINT OUT
SW01 = 0 PRINT ERROR MESSAGE

SW02 = 1 LOOP ON THE CURRENT TEST
SW02 = 0 DON'T LOOP

SW03 = 1 REPEAT THE CURRENT TEST SECTION
SW03 = 0 NORMAL TEST FLOW

SW04 = 1 LA30 HAS SERIAL LINE INTERFACE
SW04 = 0 LA30 HAS PARALLEL LINE INTERFACE

PROCESSOR SELECTION SWITCHES

05-06-07

00	PDP-8, OR PDP-8/I
01	PDP-8/L, OR PDP-12
10	PDP-8/E
11	PDP-8/S

TEST INHIBIT SWITCHES

SW08 = 1 INHIBIT BASIC IOT TEST
SW08 = 0 DO THE BASIC IOT TEST

SW09 = 1 INHIBIT THE PRINTER TESTS
SW09 = 0 DO THE PRINT TESTS

SW10 = 1 INHIBIT THE TIMING TESTS
SW10 = 0 DO THE TIMING TESTS

SW11 = 1 INHIBIT THE OPERATORS! TESTS
SW11 = 0 DO THE OPERATORS TESTS

MAINDEC-8E-D3AB-D

TD8E DECTAPE DIAGNOSTIC

ABSTRACT

TD8E DECTAPE DIAGNOSTIC IS A PROGRAM WHICH HAS BEEN WRITTEN TO CHECKOUT AND TEST TD8E DECTAPE CONTROLS WITH TU56 DECTAPE TRANSPORTS. THE PROGRAM TESTS THE BASIC FUNCTIONS OF THE

CONTROL (IOT SKIPS, DATA TRANSFERS, ETC) AS WELL AS CHECKING THE ABILITY TO READ AND WRITE ON DECTAPE.

REQUIREMENTS
PDP-8/E
TD8E DECTAPE CONTROL
TU56 DECTAPE TRANSPORT (AT LEAST ONE)
ALL NECESSARY CABLES AND MODULES

STORAGE - THE PROGRAM OCCUPIES MEMORY FROM LOCATION 20 TO LOCATION 7177 AND USES LOCATIONS 7200 TO 7577 AS DATA BUFFER AREA.

LOADING - BINARY LOADER

STARTING PROCEDURE
DUAL TRANSPORTS

ON THE TRANSPORTS, SET ONE TRANSPORT TO UNIT 0, ON-LINE, WRITE LOCK; SET THE OTHER TRANSPORT TO UNIT 1, OFF-LINE.

DEPRESS "LOAD ADDRESS", THEN "CLEAR", THEN "CONTINUE". THE PROGRAM SHOULD TYPE "OK".

REVERSE THE ROLES OF THE TWO TRANSPORTS AND REPEAT STEP C.

SET BOTH TRANSPORTS TO UNIT 1, ON-LINE. DEPRESS "LOAD ADDRESS", THEN "CLEAR", THEN "CONTINUE". THE PROGRAM SHOULD INDICATE NO UNIT 0 SELECTED

A) SET SWITCH REGISTER TO 0200

B) ON THE TRANSPORT, SET TO UNIT 0, ON-LINE, WRITE LOCK

C) DEPRESS "LOAD", THEN "CLEAR", THEN "CONTINUE". THE PROGRAM SHOULD TYPE "OK".

TO TEST CONTROL AND ABILITY TO PERFORM DATA TRANSFERS

A) SET SWITCH REGISTER TO 0201, DEPRESS "LOAD ADDRESS"

B) SET SWITCH REGISTER PER 4.1, SET SR10 IF THE PROCESSOR IS NOT A PDP-8/E, SET SR11 IF ONLY ONE TRANSPORT EXISTS OR ONLY ONLY ONE TRANSPORT IS TO BE TESTED.

C) MOUNT A STANDARD PDP-8 DECTAPE (2702 BLOCKS, 201 WORDS PER BLOCK) ON EACH TRANSPORT TO BE TESTED WITH THE TAPES WRAPPED AT LEAST 2 TURNS ON EACH TAKE UP REEL, RESPECTIVELY.

D) SET A TRANSPORT TO: UNIT 0, ON-LINE, WRITE ENABLE; SET THE OTHER TRANSPORT (IF IT EXISTS OR IS TO BE TESTED) TO UNIT 1, ON -LINE, WRITE ENABLE.

E) DEPRESS "CLEAR", THEN "CONTINUE". THE PROGRAM WILL PERFORM THE BASIC CONTROL TESTS ON THE TD8E, AND, IF SR2 IS A 0, PROCEED TO MOVE TAPE AND PERFORM DATA TRANSFERS TO AND FROM TAPE, CHECKING THE RESULTS.

0200 OPERATOR INTERVENTION TESTS
0201 CONTROL AND DATA TRANSFER TESTS
2100 SEARCH AND FIND ALL BLOCK NUMBERS

```
        2200    DISPLAY BLOCK NUMBERS IN AC
        2237    ROUTINE TO ROCK DECTAPE 0
                (TIME DEPENDENT ON SWITCH REGISTER)
        2400    READ AND CHECK THE MARK TRACK FROM ENDZONE TO
                ENDZONE
        7200    IOT MODIFICATION PROGRAM

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES
        0       1       LOOP ON CURRENT SUBTEST
                0       DON'T LOOP
        1       1       LOOP ON CURRENT TEST
                0       DON'T LOOP
        2       1       LOOP ON CONTROL TESTS
                0       DON'T LOOP
        3       1       DON'T PRINT ERRORS
                0       PRINT ERRORS
        4       1       DON'T HALT ON ERRORS
                0       HALT ON ERROR
        10      1       NOT A PDP-8/E
                0       PROCESSOR IS A PDP-8/E
        11      1       SINGLE UNIT TRANSPORT
                0       DUAL UNIT TRANSPORT


MAINDEC-8E-D6AB-D

PDP-8/E XY8-E PLOTTER
CONTROL AND DISPLAY
DIAGNOSTIC PROGRAM

ABSTRACT
        THE XY8-E PLOTTER OPTION CONTROL AND DISPLAY DIAGNOSTIC PRO-
        GRAM TESTS THE OVERALL OPERATION OF THE XY8-E CONTROL MODULE
        AND THE CALCOMP PLOTTER (SERIES 500 THROUGH 700), HOUSTON
        DP10 OR EDP10, OR EQUIVALENT, INSTALLED WITHIN A PDP-8/E SYSTEM.

        THIS PROGRAM IS SET UP TO USE DEVICE CODE 50.  IF THE DEVICE
        CODE IN THE SYSTEM UNDER TEST IS OTHER THAN 50, LOAD ADDRESS
        0225, CLEAR ALL SWITCHES, SET SR3-8 TO NEW DEVICE CODE, THEN
        DEPRESS CLEAR FOLLOWED BY CONTINUE.  THE PROGRAM WILL HALT WITH
        THE MA=0227 AND THE DEVICE CODE IN THE AC.

        ALL TIMING CHECKED IN THIS PROGRAM IS BASED UPON A 72.7 MILLISEC
        FLAG SETTING TIME FOR PEN UP AND PEN DOWN MOVEMENTS, AND A 7.5
        MILLISEC FLAG SETTING TIME FOR ALL OTHER MOVEMENTS.  IF THE SYSTEM
        IS CONFIGURED DIFFERENTLY, CHANGE THE CONTENTS OF THE FOLLOWING
        LOCATIONS AS SHOWN BELOW.

        (A = PEN UP AND PEN DOWN FLAG SETTING TIME.)
        (B = FLAG SETTING TIME FOR ALL OTHER MOVEMENTS.)

        RELATIVE        ABSOLUTE        OLD     NEW

        K70MIN          0115            0062    70% OF A
        K70MAX          0116            0055    60% OF A
        K5MIN           0117            0005    70% OF B
        K5MAX           0120            0005    60% OF B
```

K5ALL 0121 0010 130% OF B

REQUIREMENTS
PDP-8/E WITH XY8-E OPTION, CALCOMP OR HOUSTON PLOTTER WITH SPECIFICATIONS FITTING THOSE DELINEATED IN PARAGRAPH 1.2 ABOVE (FOR DISPLAY TEST ONLY), AND TELETYPE.

STORAGE - 4K OF CORE REQUIRED (FIELD 0).

LOADING - BINARY LOADER

STARTING PROCEDURE
DEENERGIZE THE PLOTTER.
LOAD ADDRESS 200.
CLEAR ALL SWITCHES.
DEPRESS CLEAR, THEN CONTINUE.
IF NO TEST 0 ERRORS OCCUR THE PROGRAM WILL INITIATE USER INTERROGATION.
ANSWER THE QUESTIONS USING THE METHOD DESCRIBED IN 5.1.2 BELOW.
AT THE COMPLETION OF INTERROGATION THE CONTROL TEST WILL BE RUN TEN TIMES, EACH PASS BEING INDICATED BY THE TTY BELL (EVERY 15 SECONDS).
AFTER COMPLETION OF THE CONTROL TEST, THE DISPLAY MONITOR ASSUMES CONTROL AND TYPES "*".
DISPLAY TEST PROCEDURE FOR CALCOMP PLOTTERS 5XX, 6XX, OR 7XX.

A. ENERGIZE THE PLOTTER AND POSITION THE PEN AT LEAST 2 INCHES FROM ANY PHYSICAL STOP. THEN RETURN ALL SWITCHES TO NEUTRAL.
B. TYPE "ALTMODE" FOLLOWED BY "D" FOLLOWED BY "RETURN".
C. THE PROGRAM WILL NOW DRAW THE COMPLETE SET OF PATTERNS.
D. WHEN ALL PATTERNS HAVE BEEN DISPLAYED, THE MONITOR WILL TYPE "*". THIS COMPLETES THE TEST AND IF NO ERRORS HAVE OCCURRED, NORMAL SYSTEM OPERATION MAY BE RESUMED.

DISPLAY TEST PROCEDURE FOR HOUSTON PLOTTERS DP10/EDP10.

[= ALTMODE
← = RETURN

PRIOR TO THE ACCOMPLISHMENT OF EACH STEP, A CLEAN SHEET OF PAPER SHOULD BE ON THE PLOT SURFACE, THE PEN POSITIONED TO THE CENTER OF THE PLOT AREA, ALL MANUAL CONTROL SWITCHES PLACED IN THEIR NEUTRAL POSITION, AND THE PLOTTER ENERGIZED. AN "*" IS TYPED AT THE COMPLETION OF EACH STEP.

A. DRAW P04 BY TYPING "[D;P04←".
B. DRAW P05 BY TYPING "[D;P05←".
C. DRAW P06 BY TYPING "[D;P06←".
D. THIS COMPLETES THE TEST, AND IF NO ERRORS HAVE OCCURRED, NORMAL SYSTEM OPERATION MAY BE RESUMED.

200 RUN COMPLETE TEST.
201 RUN COMPLETE TEST WITHOUT INIT AND TEST 0.
202 INITIALIZE ONLY.
204 DISPLAY TEST ONLY.
205 TEST 0, THEN HALT.
210 TEST 1, THEN HALT.
212 TEST 2, THEN HALT.
214 TEST 3, THEN HALT.
216 TEST 4, THEN HALT.

```
        220     TEST 5, THEN HALT.
        222     TEST 6, THEN HALT.
        225     CHANGE DEVICE CODE (REFER TO PARAGRAPH 1)

PRINTOUTS = YES

SWITCH REGISTER OPTIONS = YES
        SR BIT SET      YIELD

             0          INHIBIT ERROR HALTS.
             1          INHIBIT ERROR PRINTOUTS.
             2          BELL ON ERROR
             3          LOOP 1.
             4          LOOP 2.
             5          LOOP 3.
             9          INHIBIT RUNNING TEST0.
            *10         TAKE ERROR CONTINUE EXIT.
             11         LOOP ON CONTROL TEST (EXCEPT TEST0).

         * SETTING SR10 MAY RESULT IN MISLEADING ERROR PRINTOUTS
        OCCURRING AFTER THE FIRST ERROR PRINTOUT.  THIS OPTION SHOULD
        BE USED ONLY AFTER THE PROGRAM LISTING HAS BEEN CONSULTED TO
        DETERMINE THE CONSEQUENCES.  (ERROR 6E IS NOT AFFECTED BY
        THIS OPTION.)


MAINDEC-8E-D6CB-D

VC-8E DISPLAY DIAGNOSTIC

ABSTRACT
        THE VC-8E DISPLAY DIAGNOSTIC IS A PROGRAM WHICH FACILITATES
        THE CALIBRATION CHECK-OUT, AND DIAGNOSIS OF A VC-8E DISPLAY.
        ALL ERRORS ARE VISUAL EXCEPT FOR THE CONTROL LOGIC TEST, WHICH
        PROVIDES ERROR TYPEOUT AND SCOPE LOOPS.

REQUIREMENTS
        PDP-8/E COMPUTER, TTY OR HIGH SPEED READER
        M869 QUAD MODULE (DISPLAY CONTROL)
        M885 QUAD MODULE (D/A CONVERTER)
        TEKTRONIX 453 SCOPE OR EQUIVALENT
        VR-14, VR03A OR EQUIVALENT DISPLAY

STORAGE = THE PROGRAM OCCUPIES MEMORY LOCATIONS 0000 TO 4600

LOADING = BINARY LOADER

STARTING PROCEDURE
        SET ADDRESS TO 200

        TEST THAT IS TO BE RUN MAY NOW BE SELECTED VIA SWITCHES 8-11.
        SW7 MUST BE SET TO A ONE TO PERFORM TEST.  PROGRAM WILL TYPE
                "SELECT TEST"
        ANY TIME SW7 IS A ZERO AND WILL HANG IN DISPATCH ROUTINE UNTIL
        SW7 IS SET TO A ONE.

        THE VC-8E CAN OPERATE WITH EITHER OF TWO SETS OF IOT INSTRUC-
        TIONS, 605X AND 615X, THROUGH THE USE OF JUMPER CONNECTIONS ON
        THE M869 CONTROL BOARD, REFERENCE THE ENGINEERING SPECS FOR THE
```

CONFIGURATION OF THESE JUMPERS. THESE IOT'S CAN BE CHANGED AT ANY TIME BY THE SETTING OF SW6 (REFER TO CONTROL SWITCH SETTING TABLE). IT IS NECESSARY THAT SW6 BE PUT IN THE DESIRED POSITION BEFORE ENTERING THE DISPATCH ROUTINE THAT IS BEFORE PUTTING SW7 TO A ZERO.

DEPRESS CLEAR, CONTINUE.

DISPLAY TEST SELECTION

SW8 TO 11	TEST SELECTED
0000 (0)	NO TEST
0001 (1)	CONTROL LOGIC TEST
0010 (2)	RAMP SLEWING
0011 (3)	DC CALIBRATION
0100 (4)	DISPLAYED CALIBRATION
0101 (5)	CROSSING DIAGONALS TEST
0110 (6)	HORIZONTAL FLYBACK TEST
0111 (7)	VERTICAL FLYBACK TEST
1000 (10)	CORNERS TEST
1001 (11)	DIAGONAL LINE TEST
1010 (12)	VERTICAL BAR TEST
1011 (13)	HORIZONTAL BAR TEST
1100 (14)	SINGLE POINT PLOT TEST
1101 (15)	NO TEST
1110 (16)	NO TEST
1111 (17)	NO TEST

PRINTOUTS - YES

SWITCH REGISTER OPTIONS - YES

SWITCH REGISTER	SET AS	ACTION ON PROGRAM
0	1	PROCEED TO NEXT
	0	CALIBRATE BIT
1	1	Y AXIS
	0	X AXIS
2	1	VR03A
	0	VR14
3	1	VR14 CHANNEL 2
	0	VR14 CHANNEL 1
4	1	EXIT SCOPE LOOP
	0	HANG IN SCOPE LOOP
		(DIAGONAL LINE TEST)
5	1	PLOT UL TO LR DIAGONAL
	0	PLOT LL TO UR DIAGONAL
		(VERTICAL OR HORIZONTAL BAR TEST)
5	1	HALT LINE MOVEMENT
	0	CONTINUE LINE MOVEMENT
6	1	SELECT 615X IOT
	0	SELECT 605X IOT
7	1	PERFORM TEST SELECTED BY SWITCHES 8-11
	0	RETURN/STAY IN DISPATCH ROUTINE.
8	CONTAINS NUMBER OF TEST	
9	TO BE EXECUTED.	
10	(REFER TO TEST SELECTION TABLE)	

MAINDEC-8E-D7AA-D

RAD-8/E DIAGNOSTIC EXERCISER

IN ORDER TO UTILIZE THIS EXERCISER
THE COMPLETE DOCUMENT MUST BE USED.

MAINDEC-8E-D8AC-D

DK8E CLOCKS DIAGNOSTIC

ABSTRACT

THE DK8E CLOCKS DIAGNOSTIC IS DESIGNED TO VERIFY CORRECT OPERATION OF THE DK8-EA, DK8-EC, DK8-ES, AND DK8-EP REAL TIME CLOCK OPTIONS. THE PROGRAM UTILIZES AND TESTS IOT'S ASSOCIATED WITH THE DK8-EA LINE, DK8-EC CRYSTAL, AND THE DK8-EP/DK8-ES PROGRAMMABLE REAL TIME CLOCKS.

REQUIREMENTS

A PDP-8/E WITH THE DK8-EA, DK8-EC, DK8-ES, OR THE DK8-EP OPTION INSTALLED AND AN ASR-33 TELETYPE OR EQUIVALENT.

A SPECIAL TEST CABLE IS NECESSARY TO CONNECT THE CLOCK FRONT PANEL TO THE PDP-8/E POWER SUPPLY FOR THE DK8-ES CLOCK OPTION.

A SPECIAL CABLE IS NECESSARY TO CONNECT THE DK8-EA CLOCK MODULE TO THE PDP-8/E POWER SUPPLY FOR THE DK8-EA CLOCK OPTION.

STORAGE - THE PROGRAM OCCUPIES LOCATIONS 0000-6600.

LOADING - BINARY LOADER

STARTING PROCEDURE

DK8-EA/DK8-EC TEST

WITH THE PROGRAM IN BANK 0, SET SWITCH REGISTER TO 0200,
PRESS ADDRESS LOAD,
SET THE SWITCH REGISTER TO 0000,
SET SWITCH REGISTER TO INDICATE FREQUENCY OF DK8-EA OR DK8-EC CLOCK UNDER TEST,
PRESS CLEAR AND THEN PRESS CONTINUE.
THE PROGRAM SHOULD RUN UNTIL AN ERROR OCCURS OR UNTIL STOPPED BY THE OPERATOR.
THE TTY WILL SIGNAL "DK8E PASS COMPLETE" AT THE COMPLETION OF EVERY PASS.

DK8-EP/DK8-ES REGISTER TEST

WITH THE PROGRAM IN BANK 0, SET SWITCH REGISTER TO 0200,
PRESS ADDRESS LOAD,
SET SWITCH REGISTER TO 0000,
SET SWITCH REGISTER TO INDICATE DK8-EP/DK8-ES REGISTER TEST,

160

PRESS CLEAR AND THEN PRESS CONTINUE.
THE PROGRAM SHOULD RUN UNTIL AN ERROR OCCURS OR UNTIL STOPPED
BY THE OPERATOR.
THE TTY WILL SIGNAL "DK8E PASS COMPLETE" AT THE COMPLETION
OF EVERY PASS.

PRINTOUTS - ON ERROR

SWITCH REGISTER OPTIONS - YES
SWR0=1 FOR DK8-EP/DK8-ES REGISTER TEST
SWR1=1 FOR DK8-ES SCHMITT TRIGGER LOGIC TEST
SWR2=1 FOR INHIBIT ERROR PRINT OUT
SWR3=1 FOR INHIBIT ERROR BELL
SWR4=1 FOR INHIBIT ERROR HALT
SWR5=1 FOR ENTER SCOPE LOOP ON ERROR
SWR6=1 FOR LOOP ON NON-FAILING TEST
SWR7=1 FOR DK8-EP/DK8-ES EXTERNAL PULSE SCOPE LOOP TEST
SWR8=1 FOR DK8-ES EXTERNAL CLOCK SCOPE LOOP TEST

FREQUENCY SWITCH SETTINGS FOR DK8-EA/DK8-EC TEST

SWR9-11=0 TEST 1 CPS CRYSTAL CLOCK
SWR9-11=1 TEST 50 CPS CRYSTAL CLOCK
SWR9-11=2 TEST 50 CPS LINE CLOCK
SWR9-11=3 TEST 60 CPS LINE CLOCK
SWR9-11=4 TEST 500 CPS CRYSTAL CLOCK
SWR9-11=5 TEST 5000 CPS CRYSTAL CLOCK

MAINDEC-X8-DIQAB-A-D

DEC/X8 USERS GUIDE
MONITOR/BUILDER

THE FAMILY-OF-8 SYSTEMS EXERCISER (DEC/X8) IS A POWERFUL
AND ADAPTABLE MODULAR SOFTWARE SYSTEM DEDICATED TO THE PURPOSE
OF TESTING FAMILY-OF-8 HARDWARE IN A SYSTEMS ENVIRONMENT. THE
MODULAR STRUCTURE OF DEC/X8 ENABLES THE USER TO DESIGN AND
BUILD A UNIQUE OPERATIONAL EXERCISER CONSISTENT WITH HIS NEEDS
AND THE HARDWARE CONFUGURATION AT HAND.

MAINDEC-X8-DIPCA-A-D

DEC/X8 MODULE "HSRHSP"
HIGH SPEED READER/PUNCH EXERCISER

MODULE DESCRIPTION
"HSRHSP" IS A DEC/X8 SOFTWARE MODULE WHICH EXERCISES THE
STANDARD DEC HIGH SPEED READER AND/OR PUNCH OPTIONS.
THE READER AND PUNCH MAY BE RUN SEPARATELY OR SIMULTANEOUSLY
DEPENDENT ON MODULE INITIALIZATION. THE ONLY PATTERN USED IS
THE "SPECIAL BINARY COUNT PATTERN" WHICH CONSISTS OF A BINARY
COUNT PATTERN WITH EVERY SECOND FRAME EQUAL TO THE LOGICAL
COMPLEMENT OF THE PRECEEDING FRAME; E.G. 1,376, 2,375, 3,374, ETC.

REQUIREMENTS
PROCESSORS; PDP-8, 8/I, 8/L, 8/E, 8/M AND PDP-12.

OPTIONS: STANDARD DEC HIGH SPEED READER AND/OR PUNCH
TYPES "PR", "PP", AND "PC".
SPECIAL: IF NO PUNCH IS AVAILABLE, USE THE
"SPECIAL BINARY COUNT PATTERN" TEST TAPE
(MAINDEC-00-D2G4-PT).

RESTRICTIONS
THE PAPER TAPE BEING PUNCHED MUST NOT BE FED
DIRECTLY TO THE READER, TO RUN BOTH THE READER AND
PUNCH SIMULTANEOUSLY IT WILL BE NECESSARY TO
USE THE PUNCH ALONE TO PRE-PUNCH THE FIRST READER TAPE.

SPECIAL CONSIDERATIONS
IT IS LEGAL TO BUILD TWO OF THESE MODULES INTO
THE EXERCISER, ONE SHOULD BE SET UP FOR PUNCH ONLY,
THE OTHER FOR READER ONLY. THIS WILL ALLOW THE
READER TO BE USED MORE FREQUENTLY.

MAINDEC-X8-DIDFA-A-D

DEC/X8 MODULE "DF32DS"
DF32/DF32-D DECDISK SYSTEM EXERCISER

MODULE DESCRIPTION
"DF32DS" IS A DEC/X8 SOFTWARE MODULE WHICH EXERCISES A DF32/DF32-D
DECDISK SYSTEM WITH UP TO FOUR DISKS. THE MAIN CHARACTERISTICS
OF THIS MODULE ARE:

1. READ/WRITE TRANSFERS VARY RANDOMLY FROM 1 TO 1000(8) WORDS.

2. DISK ADDRESSES ARE SELECTED RANDOMLY BETWEEN ADDRESS
00000 OF THE LOWEST NUMBERED DISK SPECIFIED AND ADDRESS
77777 OF THE HIGHEST DISK SPECIFIED.

3. TRANSFERS WILL OCCUR ACROSS DISK BOUNDARIES AND IN THE CASE
OF 4 DISK SYSTEMS WILL WRAP AROUND TO DISK 0.

4. EACH PASS OF THE EXERCISER LOOP EXECUTES WRITE/READ/DATA CHECK
STARTING AT A RANDOMLY SELECTED DISK ADDRESS.

5. THREE READS ARE DONE IN THE CASE OF A PARITY ERROR.

REQUIREMENTS
PROCESSORS: PDP-8, 8/I, 8/L, 8/E, 8/M AND PDP-12,
OPTIONS: DF32 OR DF21-D DECDISK CONTROL WITH UP TO 4 DISKS.

RESTRICTIONS - THERE MUST BE AN EXISTENT DISK 0.

SPECIAL CONSIDERATIONS
THIS MODULE REQUIRES EXTERNAL BUFFERS.

MAINDEC-X8-DIKAC-A-D

DEC/X8 MODULE "OPRATE"
OPERATE INSTRUCTION TEST

MODULE DESCRIPTION
"OPRATE" IS A DEC/X8 SOFTWARE MODULE WHICH TESTS OPERATE
INSTRUCTIONS AND THEIR MICROPROGRAMS AS ARE LEGAL
IN SPECIFIED FAMILY-OF-8 PROCESSORS. THE
MODULE MAY BE "INITIALIZED" TO BYPASS THE ADDITIONAL
TESTS FOR ROTATE/IAC MICROPROGRAMS AND/OR SPECIAL
PDP-8/E AND 8/M OPERATES. THE METHODS USED ARE
OBVIOUS, HENCE ALL SPECIFICS MAY BE GAINED FROM
THE PROGRAM LISTING

REQUIREMENTS
PROCESSORS: PDP-8, 8/I, 8/L, 8/E, 8/M AND PDP-12.

SPECIAL CONSIDERATIONS
SR5 SHOULD BE SET TO Ø WHEN "OPRATE" IS SET UP TO TEST 8/E - 8/M MQ OPERATES.

MAINDEC-X8-DIKAB-A-D

DEC/X8 MODULE "RANMRI"
RANDOM MEMORY REFERENCE INSTRUCTION EXERCISER

MODULE DESCRIPTION
"RANMRI" IS A DEC/X8 SOFTWARE MODULE WHICH TESTS
RANDOMLY GENERATED AND, TAD, ISZ, DCA, JMS AND JMP
INSTRUCTIONS WHICH DO CURRENT PAGE DIRECT AND
INDIRECT MEMORY REFERENCES.

FIRST A RANDOM INSTRUCTION IS GENERATED AND
CHECKED FOR VALIDITY. THEN RANDOM DATA IS GENERATED.
FINALLY THE INSTRUCTION IS EXECUTED IN A
RANDOMLY SELECTED ADDRESS AND CHECKED 500(8)
TIMES. THEN THE PROCESS STARTS AGAIN.

REQUIREMENTS
PROCESSORS: PDP-8, 8/I, 8/L, 8/E, 8/M AND PDP-12.

MAINDEC-X8-DILPA-A-D

DEC/X8 MODULE "PRNTER"
PRINTER EXERCISER

MODULE DESCRIPTION

"PRNTER" IS A DEC/X8 SOFTWARE MODULE WHICH EXERCISES ANY HARDCOPY
OR CRT ASCII DRIVEN DEVICE WHICH IS TELETYPE OR LPØ8/LE8
PROGRAM COMPATIBLE. "PRNTER" APPLIES AT LEAST TO THE LPØ8
LE-8, VTØ5, VTØ6, LA3Ø, TTY AND FUTURE OPTIONS WHICH ARE
COMPATIBLE.

REQUIREMENTS
PROCESSORS: PDP-8,8/I,8/L,8/E,8/M AND PDP-12
OPTIONS: ANY HARDCOPY OR CRT ASCII DEVICE WHICH IS
TELETYPE OF LPØ8/LE8 PROGRAM COMPATIBLE.

MAINDEC-X8-DIKAD-A-D

DEC/X8 MODULE "NOTFUN"
NON-FUNCTIONAL IOT TEST

MODULE DESCRIPTION
"NOTFUN" IS A DEC/X8 SOFTWARE MODULE WHICH VERIFIES THAT ALL NON-FUNCTIONAL IOT'S WITHIN A GIVEN SYSTEM DO NOT AFFECT THAT SYSTEM WHEN EXECUTED.

THE METHOD USED IS TO EXECUTE ALL IOT'S NOT INCLUDED IN A USER SUPPLIED LIST OF FUNCTIONAL IOT'S AND VERIFYING DIRECTLY THAT THE AC IS UNEFFECTED AND THAT NO SKIP OCCURS. THE DEC/X8 MONITOR AND/OR OTHER EXERCISER MODULES SHOULD DETECT ANY MORE SUBTLE INTERACTIVE PROBLEMS

REQUIREMENTS
PROCESSORS: PDP-8,8/I,8/L,8/E,8/M AND PDP-12

MAINDEC-X8-DIKAA-A-D

DEC/X8 MODULE "MRIØ8A"
MEMORY REFERENCE INSTRUCTION TEST

MODULE DESCRIPTION
"MRIØ8A" IS A DEC/X8 SOFTWARE MODULE WHICH TESTS THE AND, TAD, ISZ AND JMS INSTRUCTIONS. THE METHODS USED ARE OBVIOUS, HENCE ALL SPECIFICS MAY BE GAINED FROM THE PROGRAM LISTING.

REQUIREMENTS
PROCESSORS: PDP-8, 8/I, 8/L, 8/E, 8/M AND PDP-12.

MAINDEC-X8-DITCA-A-D

DEC/X8 MODULE "TCØ1DT"
TCØ1/TCØ8 DECTAPE EXERCISER

MODULE DESCRIPTION
"TC01DT" IS A DEC/X8 SOFTWARE MODULE WHICH EXERCISES
A TC01/TC08 DECTAPE SYSTEM WITH UP TO EIGHT TRANSPORTS.
THE MAIN CHARACTERISTICS OF THIS MODULE ARE0

1. ALL READ/WRITE TRANSFERS CONSIST OF 777(8) WORDS
AND UTILIZE EXTERNAL BUFFERS. THE FIRST LOCATION
IN THE ASSIGNED BUFFER IS RESERVED FOR CURRENT BLOCK
BREAK IN DURING SEARCH.

2. SEARCH OPERATIONS ARE IN NORMAL MODE, BOTH DIRECTIONS.

3. READ/WRITE OPERATIONS ARE IN CONTINUOUS MODE,
BOTH DIRECTIONS.

4. ALL DRIVES WITHIN THE LIMITS OF THE LOWEST AND
HIGHEST NUMBERED DRIVES (DRIVE "8" = "0" IS LOW)
SPECIFIED ARE RANDOMLY UTILIZED.

5. ALL BLOCKS WITHIN THE LIMITS OF THE LOWEST-3
AND HIGHEST+3 BLOCKS SPECIFIED ARE
SEQUENTIALLY USED.

6. THE OPERATIONS AT EACH BLOCK CONSIST OF
WRITE/READ/CHECK FORWARD, THEN
WRITE/READ/CHECK REVERSE.

7. THREE READS ARE DONE IN THE CASE OF A PARITY ERROR.

REQUIREMENTS
PROCESSORS: PDP-8, 8/I, 8/L, 8/E, 8/M AND PDP-12(!).

OPTIONS: TC01 OR TC08 DECTAPE CONTROL WITH UP TO
EIGHT DRIVES (TU55 OR TU56)

SPECIAL: STANDARD PDP-8 FORMAT DECTAPES ARE
RECOMMENDED (2702 BLOCKS, 201 WORDS EACH).
NO GUARANTEE IS MADE FOR DECTAPES WITH ANY
OTHER FORMAT.

SPECIAL CONSIDERATIONS
THIS MODULE REQUIRES AND USES EXTERNAL BUFFERS.

MAINDEC-X8-DIKEA-A-D

DEC/X8 MODULE "EAEALL"
EAE EXERCISE OF MUY, DVI, SHL, LSR,
ASR AND NMI INSTRUCTIONS

MODULE DESCRIPTION
"EAEALL" IS A DEC/X8 SOFTWARE MODULE WHICH EXERCISES THE MUY,
DVI, SHL, ASR, LSR AND NMI INSTRUCTIONS IN ALL FAMILY-OF-8
EAE'S. IN THE KE8-E EAE BOTH MODES "A" AND "B" ARE UTILIZED.
REFER TO PARAGRAPH 4.3 FOR INITIALIZING INFORMATION.

"EAEALL" IS DIVIDED INTO FIVE TEST SECTIONS, TEST X000 THROUGH
X004.

SINCE TESTS X001 THROUGH X004 MAY CAUSE "DATA REQUEST LATE" OR "DATA RATE" ERRORS ON SOME HIGH SPEED DIRECT MEMORY ACCESS (DATA BREAK) DEVICES, THE USER HAS THE ABILITY TO BYPASS THESE TESTS AND RUN JUST TEST X000. HOWEVER, TEST X000 MAY ALSO CAUSE SIMILAR ERRORS TO OCCUR.

REQUIREMENTS
PROCESSORS: PDP-8, 8/I, 8/E, 8/M OR PDP-12.
OPTIONS: EXTENDED ARITHMETIC ELEMENT (EAE)

SPECIAL CONSIDERATIONS
THIS MODULE REQUIRES A NON-VOLATILE STEP COUNTER AND GT FLAG. SR5 SHOULD BE SET TO 0 WHEN THIS MODULE IS RUNNING SINCE THE MQ IS UTILIZED.

"DATA REQUEST LATE" OR DATA RATE" ERRORS MAY OCCUR IF THIS MODULE IS RUN WHILE EXERCISING A HIGH SPEED DIRECT MEMORY ACCESS (DATA BREAK) DEVICE.

MAINDEC-X8-DHKEA-A-D

DEC/X8 MODULE "EAEDP"
KE8-E EAE DOUBLE PRECISION AND
SAM INSTRUCTIONS EXERCISER

MODULE DESCRIPTION
"EAEDP" IS A DEC/X8 SOFTWARE MODULE WHICH EXERCISES THE DPSZ, DCM, DPIC, DAD, DST, AND SAM INSTRUCTIONS IN THE KE8-E EAE. ALL OPERATIONS ARE IN MODE "B"

"EAEDP" IS DIVIDED INTO FOUR TEST SECTIONS, TEST 4000 THROUGH 4003.

REQUIREMENTS
PROCESSORS: PDP-8/E OR PDP-8/M
OPTIONS: KE8-E EAE

SPECIAL CONSIDERATIONS
THIS MODULE REQUIRES A NON-VOLATILE GT FLAG. SR5 SHOULD BE SET TO 0 WHEN THIS MODULE IS RUNNING SINCE THE MQ IS UTILIZED.

MAINDEC-X8-DIRFA-A-D

DEC/X8 MODULE "RF08DS"
RF08 DISK SYSTEM EXERCISER

MODULE DESCRIPTION
"RF08DS" IS A DEC/X8 SOFTWARE MODULE WHICH EXERCISES AN RF08 DISK SYSTEM WITH UP TO FOUR DISKS. THE MAIN CHARACTERISTICS OF THIS MODULE ARE:

1. READ/WRITE TRANSFERS VARY RANDOMLY FROM 1 TO 1000(8) WORDS

2. DISK ADDRESSES ARE SELECTED RANDOMLY BETWEEN ADDRESSES 000000 OF THE LOWEST NUMBERED DISK SPECIFIED AND ADDRESS 777777 OF THE HIGHEST DISK

SPECIFIED.

3. TRANSFERS WILL OCCUR ACROSS DISK BOUNDARIES AND IN THE CASE OF 4 DISK SYSTEMS WILL WRAP AROUND TO DISK Ø.

4. EACH PASS OF THE EXERCISER LOOP EXECUTES WRITE/READ/DATA CHECK STARTING AT A RANDOMLY SELECTED DISK ADDRESS.

5. THREE READS ARE DONE IN THE CASE OF A PARITY ERROR.

REQUIREMENTS
PROCESSORS: PDP-8, 8/I, 8/L, 8/E, 8/M AND PDP-12
OPTIONS: RFØ8 DISK CONTROL WITH UP TO 4 DISKS.

SPECIAL CONSIDERATIONS
THIS MODULE REQUIRES EXTERNAL BUFFERS.

MAINDEC-X8-DIFPA-A-D

DEC/X8 MODULE "FPP12"

MODULE DESCRIPTION
"FPP12" IS A DEC/X8 SOFTWARE MODULE WHICH EXERCISES THE FLOATING POINT PROCESSOR OPTION. THE FPP12 IS A SUBPROCESSOR WITH SINGLE CYCLE DATA BREAK DIRECT MEMORY ACCESS. THIS MODULE OPERATES IN THE FOLLOWING WAY: ASSIGN A RANDOM BUFFER THEN MODIFY THE FPP12 INSTRUCTION SET AS TO THE MEMORY FIELD AND ADDRESS OF THE BUFFER. THEN LOAD THE "APT" TABLE INTO MEMORY AND LOAD THE FPP BUFFER FIELD AND STARTING ADDRESS POINTER REGISTERS AND START THE FPP12. WHEN AN INTERUUPT OCCURS (NORMALLY AFTER FIVE SECONDS) CHECK THE FPP ANSWER, INCREMENT THE MODULE COUNTER AND THEN RELEASE THE BUFFER JUST TESTED. THEN ASSIGN A NEW BUFFER AND REPEAT THIS CYCLE. THIS RESULTS IN TESING THE FPP12 CODE IN ALL EXISTING MEMORY FIELDS.

REQUIREMENTS
PROCESSORS: PDP-8,8/I,8/L,8/E,8/M AND PDP-12
OPTIONS: FPP12

SPECIAL CONSIDERATIONS - THIS MODULE REQUIRES EXTERNAL BUFFERS.

MAINDEC-X8-DITCB-A-D

DEC/X8 MODULE "TC58MT"
TC58 DECMAGTAPE EXERCISER

MODULE DESCRIPTION
"TC58MT" IS A DEC/X8 SOFTWARE MODULE WHICH EXERCISES A TC58 DECMAGTAPE SYSTEM WITH UP TO EIGHT TRANSPORTS. THE MAIND CHARACTERISTICS OF THIS MODULE ARE:

1. RECORD LENGTH VARIES RANDOMLY FROM 30 TO 1000 WORDS OCTAL.

2. FILE LENGTH VARIES RANDOMLY FROM 1 TO 200 RECORDS OCTAL. (EOF IS NOT WRITTEN.)

3. THE TAPE OPERATIONS PERFORMED ARE WRITE/READ-COMPARE/READ FOR EACH "FILE". SPACE REVERSE IS USED TO MOVE FROM THE END TO THE BEGINNING OF THE FILE. REWIND IS USED ONLY WHEN EOT IS SENSED.

4. ALL OPERATIONS ARE DONE AT 800 BPI, NORMAL GAP IN CORE DUMP MODE (9 TRACK TREATED AS 7 TRACK). GAP AND DENSITY MAY BE CHANGED BY THE USER AS INDICATED LATER; HOWEVER, NO PROVISIONS HAVE BEEN INCLUDED TO OPERATE IN STANDARD 9 TRACK COMPATIBLE MODE.

5. ALL DRIVES WITHIN THE LIMITS OF THE LOWEST AND HIGHEST DRIVES SPECIFIED ARE RANDOMLY UTILIZED.

6. UNLIKE MANY OTHER DECMAGTAPE EXERCISERS, THIS MODULE STARTS AT THE CURRENT TAPE POSITION. TAPE IS FORCED TO BOT ONLY WHEN EOT IS SENSED.

7. CONTINUE MODE IS UTILIZED WHENEVER POSSIBLE. IF ILLEGAL COMMAND OCCURS WHEN ATTEMPTING TO USE CONTINUE MODE, THE ERROR IS NOT REPORTED AND START/STOP OPERATION IS ATTEMPTED.

8. THE MODULE WILL HANG IF A SELECTED DRIVE IS OFF LINE OR OTHERWISE NOT READY.

REQUIREMENTS

OPTIONS: TC58 DECMAGTAPE CONTROL WITH UP TO EIGHT 7 AND/OR 9 TRACK TRANSPORTS (TU20,TU30,TU10 OR EQUIVALENTS).

SPECIAL: INDUSTRY CERTIFIED STANDARD MAGNETIC TAPE.

RESTRICTIONS

9 TRACK COMPATIBLE MODE MAY NOT BE USED. ALL 9 TRACK TRANSPORTS WILL BE OPERATED IN CORE DUMP MODE.

SPECIAL CONSIDERATIONS - THIS MODULE REQUIRES EXTERNAL BUFFERS.

MAINDEC-X8-DIDKA-A-D

DEC/X8 MODULE "TIMERA"
REAL TIME CLOCK ELAPSED TIME
REPORTER, JOB DEAD CHECKER AND
ROTATION RANDOMIZER

MODULE DESCRIPTION

"TIMERA" IS A DEC/X8 SOFTWARE MODULE WHICH CARRIES OUT THE FOLLOWING FUNCTIONS THROUGH THE USE OF A REAL TIME CLOCK.

1. REPORTS ELAPSED RUNTIME AT APPROXIMATELY 15 MINUTE INTERVALS (AFTER THE FIRST REPORT AT ELAPSED TIME 0 00 00);

2. REPORTS ANY INTERRUPT DRIVEN MODULE WHICH IS IN THE RUN STATE BUT WHOSE PASS COUNTER HAS NOT CHANGED WITHIN THE LAST 5 TO 10 MINUTES. A REPORT OF THIS TYPE INDICATES THAT THE SPECIFIED JOB IS MAKING TO PROGRESS, AND THAT PROBABLY THE DEVICE BEING EXERCISED BY TAHT JOB FAILED TO

GENERATE A PROGRAM INTERRUPT.

3. RANDOMIZE JOB SLOT ROTATION BY PERIODICALLY PLACING A RANDOM NUMBER IN THE DEC/X8 MONITOR LOCATION "ROTWRD" (00177); REFER TO THE "DEC/X8 USERS GUIDE", PARAGRAPH 4.33 FOR MORE INFORMATION ON "ROTWRD".

REQUIREMENTS
OPTIONS: REAL TIME CLOCKS TYPES:
DK8-EA, -EC, -EP
KW8/I[8/L]A, B, C, D, E, F
KW12-A

RESTRICTIONS
"TIMERA! DOES NOT RESPOND TO THE "KJFX" OR "AK" COMMANDS, IT MAY BE KILLED ONLY BY A RESTART AT 03000.

A MAXIMUM OF 4096 (DECIMAL) CLOCK TICKS PER SECOND ARE RECOGNIZED PROPERLY BY THE SOFTWARE.

SPECIAL CONSIDERATIONS
THIS MODULE REQUIRES EXTERNAL BUFFERS.

MAINDEC-X8-DIRKA-A-D

DEC/X8 MODULE "RK8DS"
RK8 DISK SYSTEM EXERCISER

MODULE DESCRIPTION
"RK8DS" IS A DEC/X8 SOFTWARE MODULE WHICH EXERCISES AN RK8 DISK SYSTEM WITH UP TO FOUR DRIVES. THE MAIN CHARACTERISTICS OF THIS MODULE ARE:

1. WRITE/READ TRANSFERS VARY RANDOMLY FROM 1 TO 1000(8) WORDS.

2. DISK ADDRESSES ARE SELECTED RANDOMLY BETWEEN ADDRESSES 0000 AND 6177 ON ALL DISKS BETWEEN THE SPECIFIED LOW AND HIGH DISK LIMITS.

3. TO ACHIEVE GREATER DATA BREAK THROUGHPUT, RANDOMLY FROM 1 TO 200(8) EXERCISER LOOP PASSES ARE MADE USING TWO ADJACENT TRACKS WITH RANDOM CHANGES TO THE SECTOR, SURFACE AND DRIVE SELECTION ENABLED.

4. THREE READS ARE DONE IN THE CASE OF A PARITY ERROR.

REQUIREMENTS
PROCESSORS: PDP-8, 8/I/8/L, 8/E, 8/M AND PDP-12.
OPTIONS: RK8 DISK SYSTEM WITH UP TO FOUR RK01 DRIVES.

SPECIAL CONSIDERATIONS
THIS MODULE REQUIRES EXTERNAL BUFFERS.

MAINDEC-X8-DDTCA-A-D

DEC/X8 MODULE "TC12LT"

TC12 LINCTAPE EXERCISER

MODULE DESCRIPTION

"TC12LT" IS A DEC/X8 SOFTWARE MODULE WHICH EXERCISES A TC12 LINCTAPE SYSTEM WITH UP TO EIGHT TRANSPORTS. THE MAIN CHARACTERISTICS OF THIS MODULE ARE:

1. ALL READ/WRITE TRANSFERS CONSIST OF 400(8) WORDS AND UTILIZE EXTERNAL BUFFERS.
2. ALL OPERATIONS PERFORMED ARE IN EXTENDED OPERATIONS MODE AND UTILIZE THE EXTENDED ADDRESSING MODE.
3. ALL DRIVES WITHIN THE LIMITS OF THE LOWEST AND HIGHEST NUMBERED DRIVES SPECIFIED ARE RANDOMLY UTILIZED.
4. ALL BLOCKS WITHIN THE LIMITS OF THE LOWEST AND HIGHEST BLOCKS SPECIFIED ARE SEQUENTIALLY USED.
5. THE OPERATIONS AT EACH BLOCK CONSIST OF WRITE/READ/CHECK.
6. THREE READS ARE DONE IN THE CASE OF A TRANSFER CHECK ERROR.
7. ALL OPERATIONS IN LINC MODE ARE DONE WITH THE INTERRUPT SYSTEM OFF.

REQUIREMENTS

PROCESSORS: PDP-12
OPTIONS: TC12 LINCTAPE PROCESSOR WITH UP TO EIGHT DRIVES (TU55 OR TU56).
SPECIAL: STANDARD PDP-12 FORMAT LINCTAPES ARE REQUIRED (1000 OR 1600 BLOCKS, 400 WORDS PER BLOCK).

SPECIAL CONSIDERATIONS

THIS MODULE REQUIRES EXTERNAL BUFFERS.

OPTION	MNEMONIC	CODE	FUNCTION
AA05/07	CLDA	6551	CLEAR DAC ADDRESS
	LDAD	6552	AC00 TO 05, TO DAC CHANNEL
	LDAR	6522	AC 0 TO 9, TO INPUT REGISTER
	UPDT	6524	UPDATE ALL CHANNELS(DOUBLE BUFFERS ONLY)
AA50	NONE: 6551 TO 56 - SELECTS, LOADS, STARTS CONVERSION ON DAC'S 0 TO 5 6561 TO 6566 SAME AS ABOVE - DAC'S 6 TO 11 6571 TO 6576 SAME AS ABOVE - DAC'S 12 TO 17		
AD01	ADSF	6531	SKIP ON FLAG
	ADRB	6532	READ BUFFER, CLEAR AC
	ADCV	6534	START CONVERT
	ADSC	6535	SET MUX., GAIN, START CONVERT
	ADRC	6536	READ BUFFER, START CONVERT
	ALL	6537	CHANNEL, GAIN, READ BUFFER, START CONVERT
AD08	ADSC	6543	SET MULTIPLEXER
	ADCC	6541	CLEAR MULTIPLEXER
	ADCV	6532	START CONVERT
	ADSF	6531	SKIP ON FLAG

	ADRB	6534	READ BUFFER
	ADIC	6544	INCREMENT MULTIPLEXER
AD8E	ADCL	6530	CLEAR ALL
	ADLM	6531	LOAD MULTIPLEXER
	ADST	6532	START CONVERSION
	ADRB	6533	READ A/D BUFFER
	ADSK	6534	SKIP ON A/D DONE
	ADSE	6535	SKIP ON TIMING ERROR
	ADLE	6536	LOAD ENABLE REGISTER
	ADRS	6537	READ STATUS REGISTER
AF01	ADSF	6531	SKIP ON FLAG
	ADCV	6532	CLEAR FLAG, START CONVERT
	ADRB	6534	READ BUFFER TO AC
	ADCC	6541	CLEAR MULTIPLEXER
	ADSC	6542	SET MULTIPLEXER FROM AC
	ADIC	6544	INCREMENT MULTIPLEXER
AF04	VSEL	6542	SELECT RANGE
	VCNV	6541	CONVERT
	VINX	6544	INDEX CHANNEL AND CONVERT
	VSDR	6561	SKIP ON DATA READY
	VSCC	6571	SAMPLE CURRENT CHANNEL
	VRD	6562	VIDAR READ
	VBA	6564	VIDAR BYTE ADVANCE
AFC-8	ADSF	6531	SKIP ON A/D FLAG SET
	ADCV	6532	START A/D CONVERSION
	ADRB	6534	READ A/D BUFFER
	READ	6541	READ DIAGNOSTIC REGISTER
	ADSG	6542	SET AMPLIFIER GAIN
	ADSC	6544	SELECT CHANNEL, START CONVERSION
AM08/AM03	ADCC	6541	READ CURRENT ADDRESS REGISTER
	ADSC	6542	CLEAR CA, FA REGISTERS AND EOS FLAG
	ADIC	6544	LOAD CA REGISTER AND CONVERT
		6571	SKIP ON END OF SCAN FLAG
		6572	INDEX CA REGISTER BY ONE AND CONVERT
		6574	LOAD FA REGISTER
AM8E	SEE AD8E		
AX08	630X	1-DXC-CLEARX; 2-DXL-LOAD X; 4-DIS-INTENSIFY POINT	
	631X	1-DYC-CLEARY; 2-DYL-LOAD Y; 4-DIS-INTENSIFY POINT	
	632X	1-SKXK-SKIP ON CRYSTAL CLOCK FLAG; 2-SKER-SKIP ON ADC TIMMING ERROR; 4-DSB-SET BRIGHTNESS	
	633X	1-XRIN-OR EXTERNAL SENSE REG. INTO AC; 2-SKAD-SKIP ON ADC DONE; 4-XRCL-CLEAR SENSE BIT WITH ONE IN AC	
	634X	1-SKRK-SKIP ON RC TIMMING CLOCK; 2-ZTEN-ZEROES IN AC CLEAR BITS IN ENABLE REG; 4-OTEN-ONE IN AC SET BITS IN EN	
ABLE REG.			
	635X	1-CLER-CLEAR ADC TIMMING ERROR FLAG; 2-CLKX-CLEAR CRYSTAL CLOCK FLAG; 4-CLRK-CLEAR RC CLOCK FLAG	
	636X	1-ICMX-INCREMENT MUX CHANNEL; 2-RADC-READ A/D BUFFER; 4-ADCV-START CONVERSION	
	637X	1-ACMX-SET MUX REG; 2-RADC-READ A/D BUFFER; 4-ADCV-START CONVERSION	
BM8L	CDF	62N1	CHANGE DATA FIELD TO N
	CIF	62N2	CHANGE INSTRUCTION FIELD TO N
	RDF	6214	READ DATA FIELD
	RIF	6224	READ INSTRUCTION FIELD
	RMF	6244	RESTORE MEMORY FIELD
	RIB	6234	READ INTERRUPT BUFFER
	CDI	62N3	CHANGE DATA FIELD AND INSTRUCTION FIELD TO N

CM8E	RCSF	6631	SKIP ON DATA FLAG
	RCRA	6632	READ ALPHA
	RCRB	6634	READ BINARY
	RCKC	6636	READ COMPRESSED
	RCSD	6671	SKIP ON CARD DONE FLAG
	RCSE	6672	START CARD MOTION AND SKIP IF READER READY
	RCRD	6174	CLEAR CARD DONE FLAG
	RCNO	6635	READ CONDITIONS OUT TO CARD READER
	RCNI	6637	READ CONDITIONS IN FROM CARD READER
	RCSI	6675	SKIP IF INTERRUPT BEING GENERATED
	RCTF	6677	CLEAR TRANSITION FLAGS

CM8F - SEE CM8E

CM8I	RCSF	6631	SKIP ON DATA FLAG
	RCRA	6632	READ ALPHA
	RCRB	6634	READ BINARY
	RCSD	6671	SKIP ON CARD DONE FLAG
	RCSE	6672	START CARD MOTION AND SKIP IF READER READY
	RCRD	6674	CLEAR CARD DONE FLAG,

CM8L - SEE CM8I

CR8E - SEE CM8E

CR8F - SEE CM8F

CR8I - SEE CM8I

CR8L - SEE CM8I

DB88	DBFI	6651	SKIP IF NO INTERRUPTING FLAG IS SET
	DBRS	6652	INCLUSIVE OR STATUS INTO AC,
	DBXS	6654	EXCLUSIVE OR AC INTO STATUS
	DBNB	6661	SKIP IF BUFFER NOT BUSY
	DBTL	6665	TRANSMIT LOOP
	DBRL	6666	RECEIVE LOOP
	DBTF	6662	SKIP IF TRAN FLAG IS UP
DB0BA	PBRS	6652	READ STATUS REGISTER
	PBXS	6654	XOR AC TO STATUS REGISTER
	PBLD	6665	LOAD DATA REGISTER
	PBRD	6666	READ DATA REGISTER
	PBNF	6661	SKIP IF NOT BUSY FLAG
	PBIF	6651	SKIP IF ANY FLAG
	PBTF	6662	SKIP IF TRANSMIT FLAG
DB8EA	DBRF	6501	SKIP IF RECEIVE FLAG SET
	DBRD	6502	READ DATA, CLEAR RECEIVE FLAG
	DBTF	6503	SKIP IF TRANSMIT FLAG IS SET
	DBDT	6504	TRANSMIT BUFFER TO AC, SET TRANS FLAG
	DBEI	6505	ENABLE INTERRUPT ENABLE
	DBDI	6506	DISABLE INTERRUPT ENABLE
	DBDC	6507	CLEAR DONE FLAG
DC02	MTSF	6121	SKIP ON RECEIVE FLAG
	MTCF	6122	CLEAR A.C. AND FLAG RECEIVER

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                MTPC            6124    READ SELECTED GROUP TRANSMIT FLAGS (Ø-7)
                MTLS            6126    READER BUFFER TO A.C.
                MKSF            6111    BIT 11 TO TTC INT. ON
                MKCC            6112    CLEAR A.C., READER BUFFER TO A.C. CLEAR FLAG
                MKRS            6114    SELECT STATIONS (Ø-7), SELECT GROUPS
                MKRB            6116    SKIP ON TRANSMITTER FLAG
                MTON            6117    CLEAR TRANSMITTER FLAG
                MTRS            6127    READ SELECTED GROUP RECEIVER FLAGS (Ø-7)
                MINT            6115    A.C. TO PRINTER BUFFER, PRINT
                MINS            6125    SKIP ON DCØ2 GROUP INTERRUPT
                MTPF            6113    A.C. TO PRINTER BUFFER, PRINT
                MTKF            6123    READ STATION SELECTED (Ø-7) AND
                                        INT. ON INTO BIT 11

DCØ2F           MKSF            6111    SKIP ON RECIVE FLAG
                MKCC            6112    CLEAR A.C. AND FLAG RECEIVER
                MTPF            6113    READ SELECTED GROUP TRANSMIT FLAGS (Ø-7)
                MKRS            6114    READ BUFFER TO A.C.
                MINT            6115    BIT 11 TO TTC INT. ON
                MKRB            6116    CLEAR A.C., READER BUFFER TO A.C. CLEAR FLAG
                MTON            6117    SELECT STATIONS (Ø-7), SELECT GROUPS

                MTSF            6121    SKIP ON TRANSMITTER FLAG
                MTCF            6122    CLEAR TRANSMITTER FLAG
                MTKF            6123    READ SELECTED GROUP RECEIVER FLAGS (Ø-7)
                MTPC            6124    A.C. TO PRINTER BUFFER, PRINT
                MINS            6125    SKIP ON DCØ2 GROUP INTERRUPT
                MTLS            6126    A.C. TO PRINTER BUFFER, PRINT, CLEAR FLAG
                MTRS            6127    READ STATION SELECTED (Ø-7) AND
                                        INT. ON INTO BIT 11

DCØ4            SWF             6151    SKIP ON WIRE FLAG
                RSS             6152    READ STATUS
                WIND            6153    WIRE INTERRUPT DISABLE
                RBF             6154    READ BUFFER, CLEAR FLAG
                WINE            6155    WIRE INTERRUPT ENABLE
                RSRB            6156    RSS AND RBF

DCØ8 A-E        TTCR            6471    CLEAR R REGISTER
                TTLR            6472    IOR AC7-11 IN R REGISTER
                TTRR            6464    READ R REGISTER INTO AC7-11
                TTRINC          6461    +1 TO R REGISTER
                TTCL            6411    CLEAR LINE SELECTION REGISTER
                TTLL            6412    LOAD LINE SEL REGISTER
                TTRL            6414    READ LINE SEL REGISTER
                TTO             6406    TRANSMIT AC11 & RAR
                TTI             6402    SCAN FOR INPUT
                TTINCR          6401    INCREMENT LSR

                CLEAR & ENABLE CLOCKS 1-4

                T1ON            6424
                T2ON            6434
                T3ON            6444
                T4ON            6454

                CLEAR & DISABLE CLOCKS 1-4

                T1OFF           6422
                T2OFF           6432
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	T3OFF	6442	
	T4OFF	6452	
	SKIP IF CLOCK FLAG IS SET		
	T1SKP	6421	
	T2SKP	6431	
	T3SKP	6441	
	T4SKP	6451	
DC08 F,N,J			
	CCF	6724	CLEAR CARRIER FLAG & START CARRIER SCANNER
	CCR	6752	CLEAR CALL REQUEST
	CDF	6741	CLEAR DIGIT FLAG
	CRF	6734	CLEAR RING FLAG & START RING SCANNER
	CRS	6722	CLEAR REQUEST TO SEND
	CSR	6755	CLEAR STATUS FLAG & READ STATUS
	CTR	6721	CLEAR TERMINAL-READY
	DDF	6712	DISABLE DC08-F INTERRUPTS
	EDF	6704	ENABLE DC08-F INTERRUPTS
	LAD	6757	LOAD A DIGIT
	LAU	6754	LOAD A UNIT
	RCD	6716	DISABLE DATASET; INCR. LINE NUMBER; & READ CARRIER STATUS
	RCS	6714	READ CARRIER SCANNER AND STATUS
	RRS	6702	READ RING SCANNER
	RTC	6756	SET CALL REQUEST (REQUEST TO CALL)
	SCF	6711	SKIP ON CARRIER FLAG
	SDF	6753	SKIP ON DIGIT FLAG
	SRF	6701	SKIP ON RING FLAG
	SRS	6732	SET REQUEST TO SEND
	SSF	6751	SKIP ON STATUS FLAG
	STR	6731	SET TERMINAL READY
	TTI	6402	TELETYPE INPUT
	TTLLD	6413	LOAD LINE REGISTER
	TTO	6404	TELETYPE OUTPUT
	TTRLD	6473	LOAD "R" REGISTER ("LOAD DISTRIBUTION COUNTER")
	TTCL	6411	
	TTCR	6471	
	TTLR	6472	
	TTXSKP	6411	SKIP ON CLOCK
	TXOF	6412	TURN OFF CLOCK
	TXON	6414	TURN ON CLOCK
	TTSL	6413	
	TTRIWG	6461	
DC14			
DF32	DCMA	6601	CLEAR DISK MEMORY ADDRESS REGISTER AND DISK FLAGS
	DMAR	6603	LOAD DISK MEMORY ADDRESS REGISTER AND READ
	DMAW	6605	LOAD DISK MEMORY ADDRESS REGISTER AND WRITE
	DCEA	6611	CLEAR DISK EXTENDED ADDRESS, REGISTER AND MEMORY ADDRESS EXTENSION
	DSAC	6612	SKIP ON ADDRESS CONFIRMED FLAG
	DEAL	6615	LOAD DISK EXTENDED ADDRESS AND MEMORY ADDRESS EXTENSION
	DEAC	6616	READ DISK EXTENDED ADDRESS REGISTER
	DFSE	6621	SKIP ON ZERO ERROR FLAG
	DFSC	6622	SKIP ON DATA COMPLETION FLAG
	DMAC	6626	READ DISK MEMORY ADDRESS REGISTER

DF32D	DCMA	6601	CLEAR DISK MEMORY ADDRESS REGISTER AND DISK FLAGS
	DMAR	6603	LOAD DISK MEMORY ADDRESS REGISTER AND READ
	DMAW	6605	LOAD DISK MEMORY ADDRESS REGISTER AND WRITE
	DCEA	6611	CLEAR DISK EXTENDED ADDRESS REGISTER AND MEMORY ADDRESS EXTENSION
	DSAC	6612	SKIP ON ADDRESS CONFIRMED FLAG
	DEAL	6615	LOAD DISK EXTENDED ADDRESS AND MEMORY ADDRESS EXTENSION
	DEAC	6616	READ DISK EXTENDED ADDRESS REGISTER
	DFSE	6621	SKIP ON ZERO ERROR FLAG
	DFSC	6622	SKIP ON DATA COMPLETION FLAG
	DMAC	6626	READ DISK MEMORY ADDRESS REGISTER

DF32E - SEE DF32D

DK8E	EA CLSK	6133	SKIP ON CLOCK FLAG
	OR CLEI	6131	ENABLE CLOCK INTERRUPT
	EC CLED	6132	DISABLE CLOCK INTERRUPT
	CLZE	6130	CLEAR CLOCK ENABLE WITH ONES IN AC
	CLSK	6131	SKIP ON INTERRUPT
	CLOE	6132	AC TO CLOCK ENABLE
	CLAB	6133	AC TO CLOCK BUFFER REGISTER
	CLEN	6134	CLOCK ENABLE REGISTER TO A,C.
	CLSA	6135	CLOCK STATUS TO A,C.
	CLBA	6136	CLOCK BUFFER REGISTER TO A,C.
	CLCA	6137	CLOCK COUNTER REGISTER TO A,C.

DM01 - NONE

DM04 - NONE

DP01A	TAC	6X01	TRANSMIT A CHARACTER
	CTF	6X02	CLEAR TRANSMIT FLAG AND SKIP IF TRANSMIT ACTIVE UP
	CIM	6X04	CLEAR IDLE MODE
	STF	6X11	SKIP TRANSMIT FLAG DOWN
	RRB	6X12	READ RECEIVE BUFFER
	SIM	6X14	SET IDLE MODE
	SEF	6X21	SKP IF RECEIVE END
	CEF	6X22	CLEAR RECEIVE END FLAG
	SRE	6X24	SET RING ENABLE
	SRI	6X31	SKP IF RING FLAG DOWN
	CRF	6X32	CLEAR RING FLAG
	STR	6X34	SET TERMINAL READY
	SSR	6X41	SKP ON TERMINAL READY
	CTR	6X42	CLEAR TERMINAL READY
	CRE	6X44	CLEAR RING ENABLE
	SRF	6X51	SKP RECEIVE FLAG DOWN
	CRA	6X52	CLEAR RECEIVE ACTIVE
	TME	6X54	TIME PULSE
	COB	6X61	CLEAR OR BUFFER
	RCB	6X62	READ OR BUFFER
	IOR	6X64	INCLUSIVE OR
	XOR	6X54	EXCLUSIVE OR

DR8E	DBDI	65X0	DISABLE DATA BUFFER INTERRUPT
	DBEI	65X1	ENABLE DATA BUFFER INTERRUPT
	DBSK	65X2	SKIP ON DATA BUFFER INPUT FLAG
	DBCI	65X3	0'S TO INPUT REGISTER CORRESPONDING TO 1'S IN AC

	DBRI	65X4	INPUT REGISTER TO A,C.
	DBCO	65X5	0'S TO OUTPUT REG, CORRESPONDING TO 1'S IN AC,C
	DBSO	65X6	1'S TO OUTPUT REG, CORRESPONDING TO 1'S IN AC,C.
	DBRO	65X7	JAM XFER OUTPUT REG TO A,C.
DS32 - SEE DF32			
FPP12	FPINT	6551	SKIP WHEN INTP, REQ, FLAG SET
	FPHLT	6554	FORCE EXIT, DUMP STATUS IN APT AND SET INTP, REQ, FLAG
	FPCOM	6553	LOAD AC TO COMMAND REG, IF NOT IN RUN AND INTP, FLAG NOT SET,
	FPICL	6552	UNCONDITIONALLY RESET FPP12 AND ALL FLAGS,
	FPST	6555	TWELVE LSB OF APT ARE SET TO AC AND FPP IS STARTED,
	FPRST	6556	READ STATUS TO AC,
	FPIST	6557	SKIP IF INTP, FLAG IS SET,
		6561	ENTER MAINTENANCE MODE OR MAINTENCE STEP,
		6562	READ STATES
		6563	READ OMSW
		6564	READ OLSW
		6565	READ APT
		6566	READ MQLSW
		6567	LOAD SHIFT COUNTER
KL8E A-G			
	KCR	6030	CLEAR KBRD FLAG BUT DO NOT SET RDR RUN
	KSF	6031	SKIP IF KEYBOARD/READER FLAG = 1,
	KCC	6032	CLEAR AC AND KBRD/READER FLAG, SET READER RUN
	KRS	6034	READ KEYBOARD/READER BUFFER STATIS
	KIE	6035	ENABLE TTY INTERRUPT WHEN AC11 EQUALS 1
	KRB	6036	CLEAR AC, READ KEYBOARD BUFFER, CLEAR KEYBOARD FLAGS
	SPF	6040	SET PRINTER FLAG
	TSF	6041	SKIP IF TELEPRINTER/PUNCH FLAG = 1
	TCF	6042	CLEAR TELEPRINTER/PUNCH FLAG
	TPC	6044	LOAD TELEPRINTER/PUNCH BUFFER SELECT AND PRINT
	SPI	6045	SKIP IF TTY INTERRUPT
	TLS	6046	LOAD TELEPRINTER/PUNCH BUFFER SELECT AND PRINT AND CLEAR TELEPRINTER/PUNCH FLAG
KE8-E	MQL	7421	LOAD MQ
	MQA	7501	INCLUSIVE OR MQ WITH AC
	NOPM	7401	EAE NOP
	CLAM	7601	EAE CLA
	NMI	7411	NORMALIZE
	SHL	7413	SHIFT LEFT
	ASR	7415	ARITHMETIC SHIFT RIGHT
	LSR	7417	LOGICAL SHIFT RIGHT
	SWP	7521	SWAP AC AND MQ
	CAM	7621	CLEAR AC AND MQ
	ACL	CLAM MQA	LOAD AC FROM MQ
	SCA	7441	STEP COUNTER TO AC
	SWAB	7431	SWITCH FROM MODE "A" TO "B",
	SWBA	7447	SWITCH FROM MODE "B" TO "A",
	SCL	7403	STEP COUNTER LOAD FROM MEMORY
	ACS	7403	ACCUMULATOR TO STEP COUNTER
	SAM	7457	SUBTRACT AC FROM MQ
	DAD	7443	DOUBLE PRECISION ADD
	DST	7445	DOUBLE PRECISION STORE
	DPIC	7573	DOUBLE PRECISION INCREMENT

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                DCM             7575    DOUBLE PRECISION COMPLEMENT
                DPSZ            7451    DOUBLE PRECISION SKIP IF ZERO,
                DLD         DAD CAM     DOUBLE PRECISION LOAD
                DDZ         DST CACM    DOUBLE PRECISION DEPOSIT ZERO

KE8I            DVI             7407    DIVIDE
                NMI             7411    NORMALIZE
                SHL             7413    SHIFT LEFT
                ASR             7415    ARITHMETIC SHIFT RIGHT
                LSR             7417    LOGICAL SHIFT RIGHT
                MQL             7421    LOAD AC INTO MQ, CLEAR AC
                MUY             7405    MULTIPLY
                MQA             7501    INCLUSIVE OR, MQ WITH AC
                CAM             7621    CLEAR AC AND MQ
                SCA             7441    READ SC INTO AC
                CLA             7601    CLEAR AC
                SCL             7403    LOAD THE STEP COUNTER

KL8 - SEE KL8-E

KL8F - SEE KL8-E

KM8E            CDF             62N1    CHANGE TO DATA FIELD N
                CIF             62N2    CHANGE TO INSTRUCTION FIELD N
                CDI             62N3    CHANGE TO DATA FIELD AND INSTRUCTION FIELD N
                RDF             6214    READ DATA FIELD
                RIF             6224    READ INSTRUCTION FIELD
                RMF             6244    RESTORE MEMORY FIELD

KP8E            SPL             6102    SKIP ON LOW POWER

KP8I - SEE KP8E

KP8L - SEE KP8E

KT8I            CDF             62N1    CHANGE TO DATA FIELD N
                CIF             62N2    CHANGE TO INSTRUCTION FIELD N
                CDI             62N3    CHANGE TO DATA FIELD AND INSTRUCTION FIELD N
                CINT            6204    CLEAR USER INTERRUPT
                RDF             6214    READ DATA FIELD
                RIF             6224    READ INSTRUCTION FIELD
                RIB             6234    READ INTERRUPT BUFFER
                RMF             6244    RESTORE MEMORY FIELD
                SINT            6254    SKIP ON USER INTERRUPT
                CUF             6264    CLEAR USER FLAG
                SUF             6274    SET USER FLAG
                TTI             6402
                TTO             6404
                TTINCR          6401
                TTCL            6411
                TTRL            6414

KV8I            SNC             6051    SKIP NEXT INST IF NO CURSOR FLAG INTERRUPT
                CCF             6052    CLEAR CURSOR FLAG
                SAC             6062    SELECT ANALOG COMPARATOR
                LDF             6063    LOAD FORMAT
                LDX             6064    LOAD X REGISTER
                LDY             6065    LOAD Y REGISTER
                EXC             6066    EXECUTE INST. ACCORDING TO AC WORD
                SRF             6071    SKIP IF READY SET
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                CRF             6072    CLEAR READY FLAG
                SDA             6073    SKIP WHEN D/A OUTPUT IS GREATER THAN SELECTED SOURCE
                LDA             6074    LOAD D/A

KW08-S
                CLSF            6301    SKIP ON CLOCK OVERFLOW FLAG
                CLCB            6302    TURN OFF CLOCK, CLEAR OVERFLOW FLAG CLEAR CLOCK BUFFER
                CLIB            6304    INCLUSIVE OR INTO CLOCK BUFFER FROM AC
                CLLB            6306    CLEAR AND LOAD CLOCK BUFFER
                CLAC            6311    CLEAR AC
                CLAB            6312    INCLUSVIE OR CLOCK BUFFER INTO AC
                CLRB            6313    READ CLOCK BUFFER
                CLON            6314    ENABLE (TURN ON) CLOCK

KW8-I           CCF             6312    CLEAR ALL CONTROL FLIP-FLOPS
                SCF             6133    SKIP AND CLEAR FLAG
                RCL             6134    READ CLOCK
                RCLA            6135    READ CLOCK
                CFC             6136    CLEAR ALL CONTROL FLIP-FLOPS AND ENABLE CLOCKS
                CLI             6137    CLEAR ALL CONTROL FLIP-FLOPS ENABLE CHECK & INTERRUPT

KW8L - SEE KW8I

LC8E

LE8             LSR             6663    SKIP ON NOT READY
                LSF             6661    SKIP ON CHARACTER FLAG SET
                LSP             6665    SET PROGRAM INTERRUPT
                LCP             6667    CLEAR PROGRAM INTERRUPT
                LLC             6664    TRANSMIT CHARACTER TO PRINTER
                LCF             6662    CLEAR CHARACTER FLAG
                LPC             6666    TRANSMIT CHARACTER AND CLEAR FLAG

LPC-8           SLF             6631    SKIP ON DONE FLAG
                CFDB            6632    CLEAR FLAG AND DATA BUFFER
                LDB             6634    LOAD DATA BUFFER
                STF             6671    SKIP ON TESTER FLAG
                RTDB            6672    READ TESTER DATA BUFFER,
                ET              6674    ENABLE TESTER

LP08 - SEE LE8

LT08            /SKIP ON KEYBOARD FLAG
                KSFLT1          6401    LINE 1
                KSFLT2          6421    2
                KSFLT3          6441    3
                KSFLT4          6461    4
                KSFLT5          6111

                /CLEAR KEYBOARD FLAG
                KCCLT1          6402    LINE 1
                KCCLT2          6422    2
                KCCLT3          6442    3
                KCCLT4          6462    4
                KCCLT5          6112    5

                /READ KEYBOARD STATIC

                KRSLT1          6404    LINE 1
                KRSLT2          6424    2
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KRSLT3          6444    3
KRSLT4          6464    4
KRSLT5          6114    5

/READ KEYBOARD DYNAMIC

KRRLT1          6406    LINE 1
KRRLT2          6426    2
KRRLT3          6446    3
KRRLT4          6466    4
KRRLT5          6116    5

/SKIP ON TLEPRINTER FLAGS

TSFLT1          6411
TSFLT2          6431
TSFLT3          6451
TSLFT4          6471
TLSFLT5         6121

/CLEAR TELEPRINTER FLAGS

TCFLT1          6412
TCFLT2          6432
TCFLT3          6452
TCFLT4          6472
TCFLT5          6122

/LOAD TELEPRINTERS AND PRINT

TPCLT1          6414
TPCLT2          6434
TPCLT3          6454
TPCLT4          6474
TPCL5           6124

/LOAD TELEPRINTER SEQUENCES

TLSLT1          6416
TLSLT2          6436
TLSLT3          6456
TLSLT4          6476
TLSLT5          6126

LT33    KSF     6031    SKIP IF KEYBOARD/READER FLAG=1
        KCC     6032    CLEAR AC AND KEYBOARD/READER FLAG
        KRS     6034    READ KEYBOARD/READER BUFFER, STATIC
        KRB     6036    CLEAR AC, READ KEYBOARD BUFFER
                        CLEAR KEYBOARD FLAG

                TELETYPE TELEPRINTER/PUNCH

        TSF     6041    SKIP IF TELEPRINTER/PUNCH FLAG=1
        TCF     6042    CLEAR TELEPRINTER/PUNCH FLAG
        TPC     6044    LOAD TELEPRINTER/PUNCH BUFFER, SELECT
                        AND PRINT
        TLS     6046    LOAD TELEPRINTER/PUNCH BUFFER, SELECT AND PRINT,
                        AND CLEAR TELEPRINTER/PUNCH FLAG

LT35 = SEE LT33
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MC8E            CDF             62N1    CHANGE TO DATA FIELD N
                CIF             62N2    CHANGE TO INSTRUCTION FIELD N
                CDI             62N3    CHANGE TO DATA FIELD AND
                                        INSTRUCTION FIELD N
                CINT            6204    CLEAR USER INTERRUPT
                RDF             6214    READ DATA FIELD
                RIF             6224    READ INSTRUCTION FIELD

ML8I            CDF             62N1    CHANGE TO DATA FIELD N
                CIF             62N2    CHANGE TO INSTRUCTION FIELD N
                RDF             6214    READ DATA FIELD INTO AC 8
                RIF             6224    READ INSTRUCTION FIELD INTO AC 8
                RMF             6244    RESTORE MEMORY FIELD
                RIB             6234    READ INTERRUPT BUFFER

MC8L - SEE MC8I

MI8E - NONE

MM8E - SEE MC8E

MM8EJ - SEE MC8E

MM8I - SEE MC8I

MM8L - SEE MC8I

MP8I -          CMP             6104
                SNPE            6101

MP8L - SEE MP8I

MP8E            DPI             6100    DISABLE PARITY INTERRUPT
                SMP             6101    SKIP IF NO PARITY ERROR
                EPI             6103    ENABLE PARITY INTERRUPT
                CMP             6104    CLEAR PARITY ERROR FLAG
                CEP             6106    CHECK FOR EVEN PARITY
                SPO             6107    SKIP ON PARITY OPTION

MR8E - NONE

PA60            RSF             6011    SKIP IF READER FLAG SET
                RRB             6012    READ READER BUFFER AND CLEAR FLAG
                RFC             6014    FETCH CHARACTER FROM TAPE TO READER BUFFER, SET FLAG
                PSF             6021    SKIP IF PUCH FLAG SET
                PCF             6022    CLEAR PUNCH FLAG AND BUFFER
                PPC             6024    LOAD PUNCH BUFFER AND PUNCH CHARACTER
                SKPNA           6311    SKIP IF PUNCH NOT AVAILABLE
                RSC             6312    LOAD READER SELECTION BUFFER FROM AC.
                PSC             6314    LOAD PUNCH SELECTION BUFFER FROM AC.

PA61 - SEE PA60

PA63 - SEE PA60

PA68 - SEE PA60

PC01            HIGH SPEED PERFORATED TAPE READER
                RSF             6011    SKIP IF READER FLAG=1
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                RRB             6012    READ READER BUFFER; AND CLEAR FLAG
                RFC             6014    CLEAR FLAG AND BUFFER AND FETCH CHARACRACTER

                HIGH SPEED PERFORATED TAPE PUNCH
                PSF             6021    SKIP IF PUNCH FLAG=1
                PCF             6022    CLEAR FLAG AND BUFFER
                PPC             6024    LOAD BUFFER AND PUNCH CHARACTER
                PLS             6026    CLEAR FLAG AND BUFFER; LOAD AND PUNCH

PC02            HIGH SPEED PERFORATED TAPE READER
                RSF             6011    SKIP IF READER FLAG=1
                RRB             6012    READ READER BUFFER; AND CLEAR FLAG
                RFC             6014    CLEAR FLAG AND BUFFER AND FETCH CHARACTER

PC03            HIGH SPEED PERFORATED TAPE PUNCH
                PSF             6021    SKIP IF PUNCH FLAG=1
                PCF             6022    CLEAR FLAG AND BUFFER
                PPC             6024    LOAD BUFFER AND PUNCH CHARACTER
                PLS             6026    CLEAR FLAG AND BUFFER; LOAD AND PUNCH

PC04 - SEE PC01

PC8E            HIGH SPEED PERFORATED TAPE PUNCH - TyPE
                RPE             6010    SET INTERRUPT ENABLE FOR READER AND PUNCH
                PCE             6020    CLEAR INTERRUPT ENABLE FOR READER AND PUNCH
                PSF             6021    SKIP IF PUNCH FLAG=1
                PCF             6022    CLEAR FLAG AND BUFFER
                PPC             6024    LOAD BUFFER AND PUNCH CHARACTER
                PLS             6026    CLEAR FLAG AND BUFFER, LOAD BUFFER AND
                                        PUNCH CHARACTER

                HIGH SPEED PERFORATED TAPE READER-TYPE F
                RPE             6010    SET INTERRUPT ENABLE FOR READER AND PUNCH
                RSF             6011    SKIP IF READER FLAG=1
                RRB             6012    READ READER BUFFER AND CLEAR FLAG
                RCF             6014    CLEAR FLAG AND BUFFER AND FETCH CHARACTER
                RCC             6016    READ READER BUFFER; CLEAR FLAG AND BUFFER,
                                        AND FETCH CHARACTER
                PCE             6020    CLEAR INTERRUPT ENABLE FOR READER AND PUNCH
```

PC8J - SEE PC04

PC8L - SEE PC04

PP8E - SEE PC8E

PP8I - SEE PC03

PP8L - SEE PC03

PP67 - SEE PA60

PR68 - SEE PA60

PR8E - SEE PC8E

PR8I - SEE PC02

PR8L - SEE PC02

PT08C - SEE LT08

PT08F - SEE LT08

RF08/RB01

	DCMA	6601	CLEAR FLAGS
	DMAR	6603	READ
	DMAW	6605	WRITE
	DCIM	6611	CLEAR DISK INTERRUPT ENABLES
	DSAC	6612	SKIP ON ADC
	DIML	6615	LOAD INTERRUPT ENABLE
	DIMA	6616	LOAD AC WITH STATUS REGISTER
	DFSE	6621	SKIP ON ERROR
	DFSC	6622	SKIP ON COMPLETION FLAG SET
	DMAC	6626	LOAD AC WITH DISK MEMORY ADDRESS
	DMMT	6646	MAINTENANCE
	DCXA	6641	CLEAR DISK EXT ADDRESS
	DXAL	6643	LOAD DISK EXT ADDRESS
	DXAC	6645	LOAD AC WITH DISK EXT ADDRESS
	DISK	6623	SKIP ON DISK FLAG
RK8	DLDA	6731	AC TO TRACK, SURFACE, AND SECTOR REGISTERS
	DLDC	6732	AC TO COMMAND REGISTER
	DLDR	6733	AC TO TRACK ADDRESS REGISTER AND -READ-
	DRDA	6734	TRACK ADDRESS COUNTER TO AC
	DLDW	6735	AC TO TRACK ADDRESS AND -WRITE-
	DRDC	6736	COMMAND REGISTER TO AC
	DCHP	6737	AC TO TRACK ADDRESS REGISTER AND -CHECK PARITY-
	DRDS	6741	STATUS REGISTER TO AC
	DCLS	6742	CLEAR STATUS REGISTER
	DMNT	6743	AC TO MAINTENANCE REGISTER AND EXECUTE
	DSKD	6745	SKIP IF CONTROL DONE F/F (XFER DONE AND/OR TRACK FOUND) = 1
	DSKE	6747	SKIP IF ERROR FLAG F/F = 1
	DCLA	6751	FORCE SELECTED DISK TO TRACK Ø AND CLEAR ALL REGISTERS EXCEPT DA
	DRWC	6752	WORD COUNT REGISTER TO AC
	DLWC	6753	AC TO WORD COUNT REGISTER
	DLCA	6755	AC TO CURRENT ADDRESS REGISTER
	DRCA	6757	CURRENT ADDRESS REGISTER TO AC
RK8E	DSKP	6741	SKIP ON DISK DONE OR ERROR
	DCLR	6742	CLEAR ALL
	DLAG	6743	LOAD ADDRESS AND GO,
	DLCA	6744	LOAD CURRENT ADDRESS.
	DRST	6745	READ STATUS
	DLDC	6746	LOAD COMMAND REGISTER.
	DMAN	6747	MAINTENANCE IOT.
RM08	DCW	6605	
	DCR	6603	
	DTS	6615	
	DFS	6624	
	DSC	6622	

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                DSE             6621
                DES             6612

TC01            DTRA            6761    READ STATUS REGISTER A
                DTCA            6762    CLEAR STATUS REGISTER A
                DTXA            6764    LOAD STATUS REGISTER A
                DTSF            6771    SKIP ON FLAGS
                DTRB            6772    READ STATUS REGISTER B
                DTLB            6774    LOAD STATUS REGISTER B

TC08 - SEE TC01

TC58            MTSF            6701    SKIP ON MAGTAPE FLAG
                MTCR            6711    SKIP ON CONTROL READY
                MTTR            6721    SKIP ON TRANSPORT READY
                MTAF            6712    MAGTAPE CLEAR FLAGS
                MTRC            6724    READ COMMAND
                LCM             6714    LOAD COMMAND NO CLEAR
                MTLC            6716    CLEAR AND LOAD COMMAND
                MTRS            6706    READ STATUS
                MTGO            6722    TAPE GO
                MCAF            6732    POWER CLEAR MTF
                SDF             6731    SET DATA FLAG

TD8E            SDSS            6771    SKIP ON SINGLE LINE FLAG
                SDST            6772    SKIP ON TIMING ERROR
                SDSQ            6773    SKIP ON QUADRUPLE LINE FLAG
                SDLC            6774    LOAD COMMAND REGISTER
                SDLD            6775    LOAD DATA REGISTER, CLEAR FLAGS
                SDRC            6776    READ COMMAND REGISTER AND MARK TRACK, CLEAR FLAGS
                SDRD            6777    READ DATA REGISTER; CLEAR FLAGS

UDC8            UDSS            6351    SKIP ON SCAN NOT BUSY
                UDSC            6353    START SCAN
                UDRA            6356    READ ADDRESS
                UDLS            6357    READ COSGATES
                UDRS            6355    SKIP ON DEFFERRED INTERRUPT
                UDSF            6361    SKIP ON IMMEDIATE INTERRUPT
                UDLA            6363    LOAD ADDRESS
                UDEI            6364    ENABLE UDC INTERRUPT
                UDDI            6365    DISABLE UDC INTERRUPT
                UDRD            6366    READ DATA
                UDLD            6367    LOAD DATA

VC8E            DICL            6050    CLEARS ENABLES, FLAGS
                DICD            6051    CLEARS DONE FLAG
                DISD            6052    SKIP ON DISPLAY DONE FLAG (NO CIR)
                DILX            6053    LOAD X REGISTER
                DILY            6054    LOAD Y REGISTER
                DIXY            6055    INTENSIFY
                DILE            6056    LOAD ENABLE FROM AC, CLEAR AC
                DIRE            6057    ENABLE TO AC

VC8I            DXC             6051    CLEAR X DEFLECTION REGISTER
                DXL             6053    LOAD X DEFLECTION REGISTER
                DIS             6054    DISPLAY (INTENSIFY)
                DYC             6061    CLEAR Y DEFLECTION REGISTER
                DYL             6063    LOAD Y DEFLECTION REGISTER
                DSI             6064    DISPLAY (INTENSIFY)
                DSF             6071    SKIP ON LITE PEN FLAG
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	DCF	6072	CLEAR LITE PEN FLAG
	DIR	6074	SET INTENSITY REGISTER

VC8L - SEE VC8I

VP8I	PLSF	6501	SKIP IF FLAG IS SET
	PLCF	6502	CLEAR FLAG
	PLPU	6504	OPEN UP
	PLPP	6511	OPEN RIGHT
	PLDD	6512	DRUM UP
	DUPR	6513	DRUM UP; PEN RIGHT
	PLUD	6514	DRUM DOWN
	DDPR	6515	DRUM DOWN; PEN RIGHT
	PLPL	6521	PEN LEFT
	PLUD	6522	DRUM UP
	DUPL	6523	DRUM UP; PEN LEFT
	PLPD	6524	PEN DOWN

VP8L - SEE UP8I

VT05 - NONE

VT06 - NONE

VW02 - NONE

XY8E	PLCE	6500	CLEAR INTERRUPT ENABLE
	PLSF	6501	SKIP IF PLOT FLAG=1
	PLCF	6502	CLEAR PLOT FLAG
	PLPU	6503	PEN UP (500 SERIES ONLY)
	PLCR	6504	LOAD OR SET FLAG
	PLPD	6505	PEN DOWN (500 SERIES ONLY)
	CFLR	6506	CLEAR FLAG, LOAD DR, SET FLAG
	PLSE	6507	SET INTERRUPT ENABLE

TR05/TR06 - SEE TC58

TR02	IRS	6701	SKIP ON READ DONE
	ISR	6702	READ STATUS REGISTER
	IWS	6703	SKIP ON WRITE DONE
	IMC	6704	MOVE COMMAND
	IGS	6705	SKIP ON GAP DETECT
	IWR	6706	WRITE AC INTO TAPE BUFFER
	IRD	6707	READ BUFFER INTO AC

THOSE NOT DONE - IOT

AF06
DP8E
KG8E
LC8L
LC8E
RC8/RS64
RK8E/RK08
TM8-E