Mnemonic	Code	Function	Time (μsec.)
		EXTENDED MEMORY MC12	
CDF	62n1	change to data field n	follow by JMP F
CIF	62n2	change to instruction field n	
RDF	6214	read data field into AC bits 6-8	
RIF	6224	read instruction field into AC bits 6-8	
RMF	6244	restore memory field	
RIB	6234	read interrupt buffer	
		INTERRUPT CONTROL	
ION	6001	turn interrupt on	
IOF	6002	turn interrupt off	
		REAL TIME CLOCK KW12	4.25 if executed from 8-mode. 5.9 if executed from LINC-mode.
CLSK	6131	skip on clock interrupt	
CLLR	6132	AC → clock control register	
CLAB	6133	AC → clock preset register	
CLEN	6134	AC → clock enable register	
CLSA	6135	clock status register → AC	
CLBA	6136	clock preset register → AC	
CLCA	6137	counter → AC	
		MODE CHANGE	
LINC	6141	change to LINC mode	
		POWER FAILURE/RESTART KP12	
SPL	6102	skip on power too low	
		8-MODE MULTIPLY/DIVIDE KE12	
**SCL	7403	load the step counter	3.2
**MUY	7405	multiply	8.0
**DVI	7407	divide	4.0-9.0
**NMI	7411	normalize	1.6 + 0.3n
**SHL	7413	shift left	1.6 + 0.3n
**ASR	7415	arithmetic shift right	1.6 + 0.3n
**LSR	7417	logical shift right	1.6 + 0.3n
**MQL	7421	load AC into MQ, clear AC	1.6
**SCA	7441	read SC into AC	1.6
**MQA	7501	inclusive OR, MQ with AC	1.6
**CLA	7601	clear AC	1.6
**CAM	7621	clear AC and MQ	1.6
		HIGH SPEED PERFORATED TAPE READER TYPE PR8/I	4.25 if executed from 8-mode. 5.9 if executed from LINC-mode.
RSF	6011	skip if reader flag=1	
RRB	6012	read reader buffer, and clear flag	
RFC	6014	clear flag and buffer and fetch character	
		HIGH SPEED PERFORATED TAPE PUNCH TYPE PR8/I	
PSF	6021	skip if punch flag=1	
PCF	6022	clear flag and buffer	
PPC	6024	load buffer and punch character	
PLS	6026	clear flag and buffer; load and punch	

SPECIAL REGISTER BIT ASSIGNMENTS

0	1	2	3	4	5	6	7	8	9	10	11

Bit	Special Function Register	Tape Extended Operations Register
0	not used	extended memory address bits
1	not used	extended memory address bits
2	trap enable	extended memory address bits
3	tape trap enable	not used
4	half-size characters	tape mark enable
5	fast sample enable	tape interrupt enable
6	disable TTY interrupt	maintenance mode
7	generate I/O power clear	extended addressing mode
8	not used	no pause operation
9	not used	hold current transport motion
10	not used	additional transports
11	not used	additional transports

INDEX CLASS ADDRESSING

I=0	$\beta \neq 0$	operand address is in β register
I=0	$\beta = 0$	operand address is in next location
I=1	$\beta = 0$	operand address is in next location
I=1	$\beta \neq 0$	operand address—1 in β register, β register is incremented by 1 during instruction execution

HALF-WORD CLASS ADDRESSING

I=0	$\beta = 0$	operand address* is in p+1
I=0	$\beta \neq 0$	operand address* is in β register
I=1	$\beta = 0$	operand is left half of p+1
I=1	$\beta \neq 0$	operand address*—4000 in β register, β register incremented by 4000 during instruction execution

*Except in the case I=1, β=0, the 12-bit operand address is computed as follows: the 11 low-order bits specify a memory address. The high order bit (bit 0) selects a half-word as follows:
bit 0=0—left half-word
bit 0=1—right half-word